

# Compal Confidential

## DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

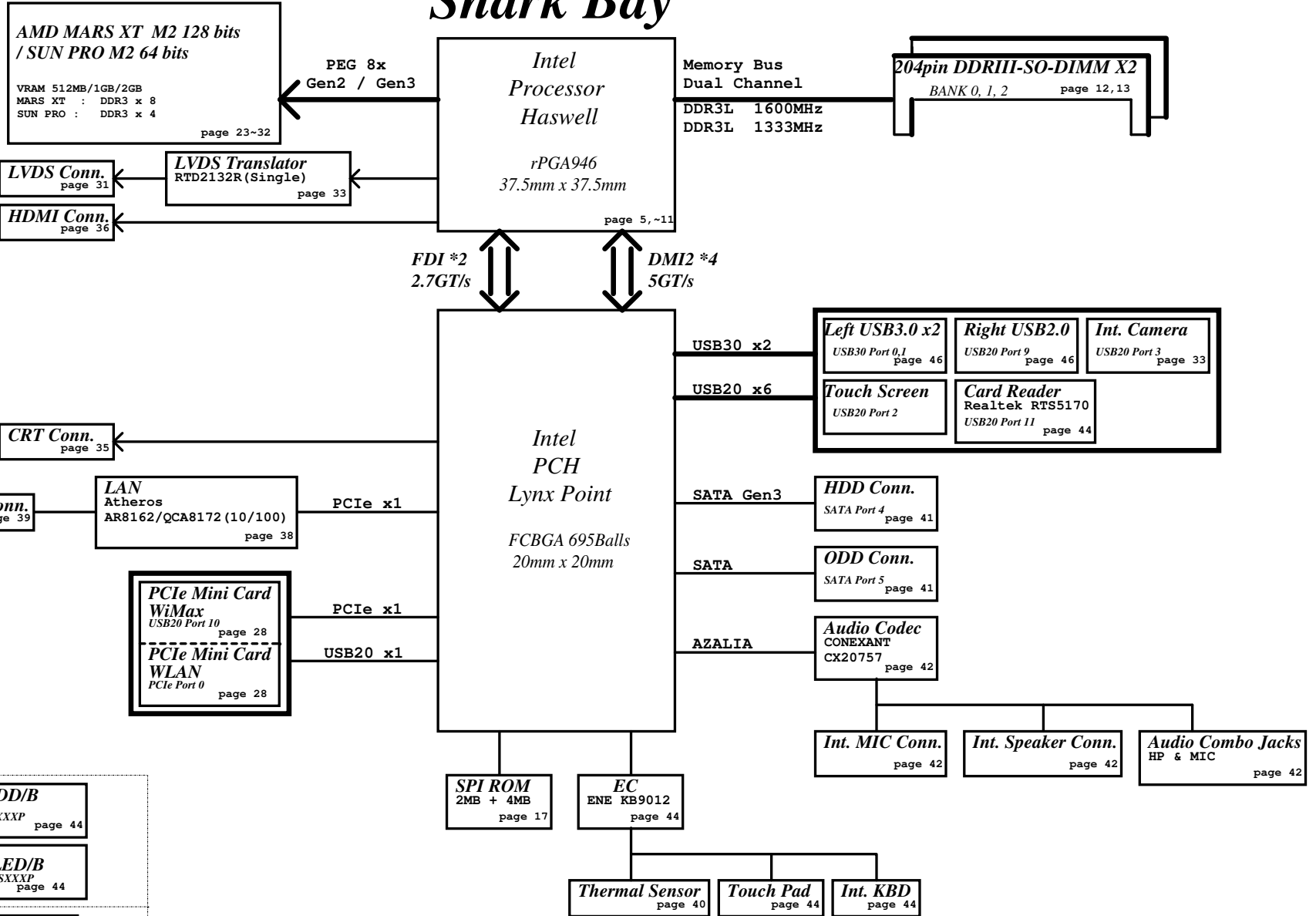
2012-08-06

LA-9641P

REV: 0.1

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# Shark Bay



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### Voltage Rails

power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS
				+VCC_CORE +VGA_CORE  +1.5VS +0.675VS +1.05VS
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor	1001_100xb

### PCH SM Bus address

### AMD-GPU SM Bus address

Device	Address	Device	Address
DDR DIMM0	1001 000Xb	Internal thermal sensor	1000_001xb
DDR DIMM2	1001 010Xb		

Device	Address
RTD2132R	1101 010Xb

### SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X
SMB_EC_DA1									
SMB_EC_CK2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS	V +3VS
SMB_EC_DA2									
SMBCLK	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X	X
SMBDATA									
SML0CLK	PCH +3VALW	X	X	X	X	X	X	X	X
SML0DATA									
SML1CLK	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X	V +3VS
SML1DATA									

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

### Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Project	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

### USB Port Table

	USB 2.0 Port	3 External USB Port
EHCI1	UHCI0	0 Left USB3.0
		1 Left USB3.0
	UHCI1	2 Touch screen
		3 Camera
	UHCI2	4
EHCI2	UHCI3	5
		6
	UHCI4	7
		8
	UHCI5	9 Right USB2.0
		10 WLAN
	UHCI6	11 Card reader
	12	
	13	

### BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Camera	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
GREEN CLOCK	GCLK@
DIS GREEN CLOCK	GCLK304@
UMA GREEN CLOCK	GCLK244@
NO GREEN CLOCK	NOGCLK@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

VRAM BOM STRUCTURE Refer P4. VGA NOTE

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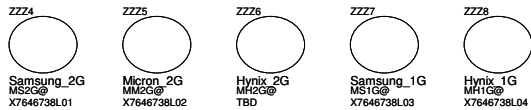
### Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

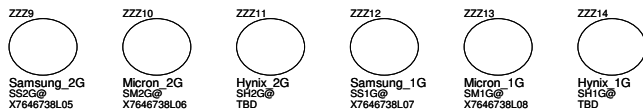
#### Mars XT VRAM STRAP

		X76@			X76@		
		Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
2GBytes	ZZZ4 MS2G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
	ZZZ5 MM2G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
1GBytes	ZZZ6 MH2G@	Hynix 2048Mbits TBD H5TQ2G63DFR-N0C	0	1	0	4.53K	2K
	ZZZ7 MS1G@	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
	ZZZ8 MH1G@	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC



#### Sun PRO VRAM STRAP

		X76@			X76@		
		Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
2GBytes	ZZZ9 SS2G@	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
	ZZZ10 SM2G@	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-109G:E	0	0	1	8.45K	2K
1GBytes	ZZZ11 SH2G@	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
	ZZZ12 SS1G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
	ZZZ13 SM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
	ZZZ14 SH1G@	Hynix 2048Mbits TBD H5TQ2G63DFR-N0C	1	1	1	4.75K	NC



VDDR3(3.3VGS)

PCIE\_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD\_CT(1.8V)

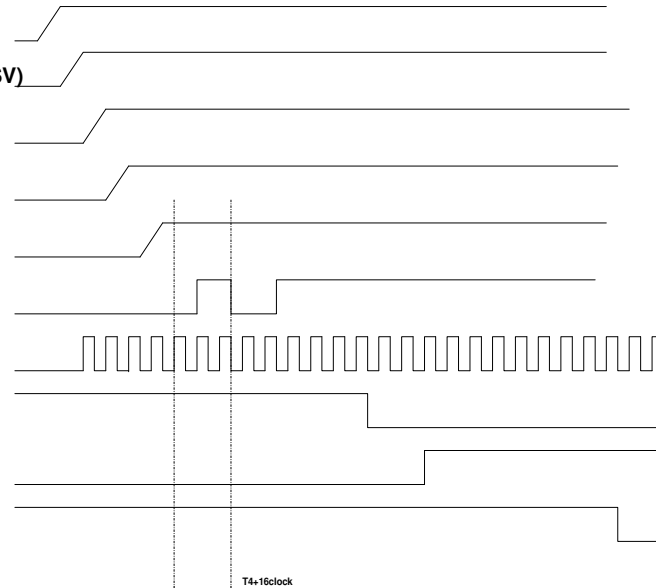
PERSTb

REFCLK

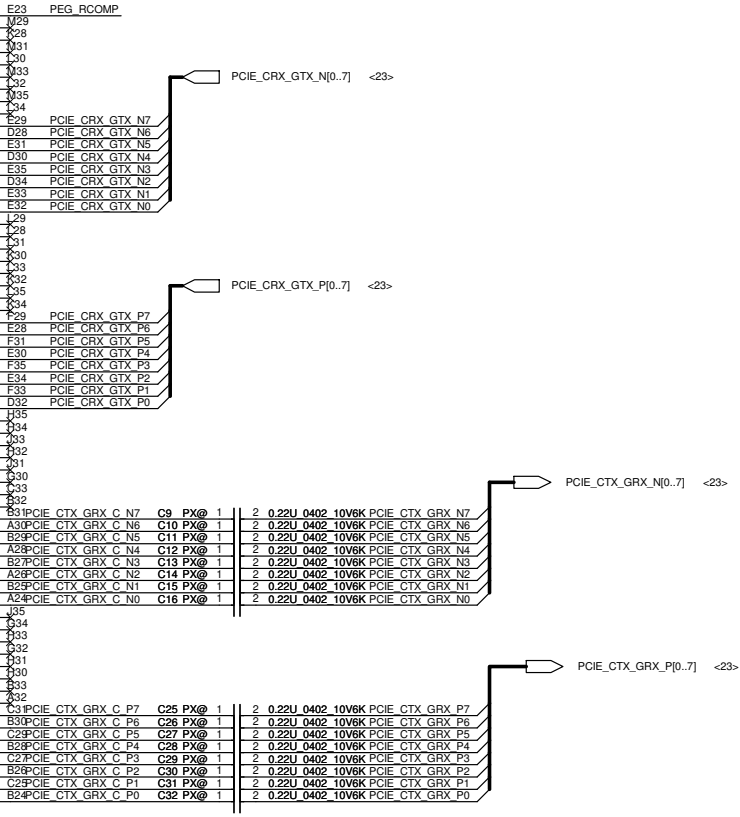
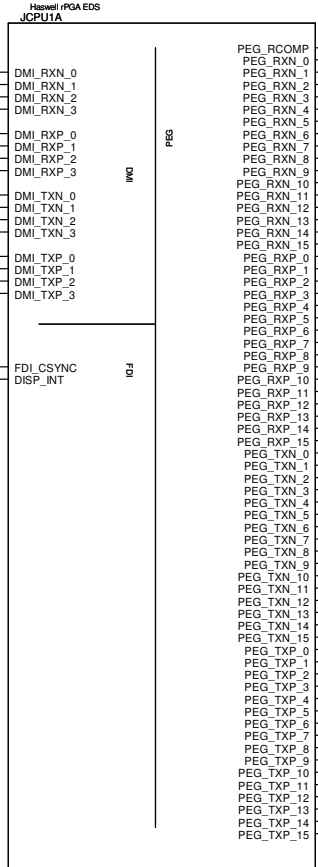
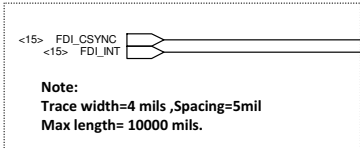
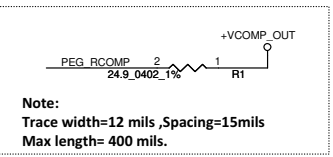
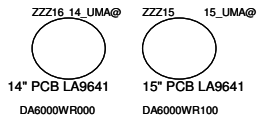
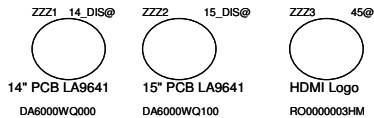
Straps Reset

Straps Valid

Global ASIC Reset

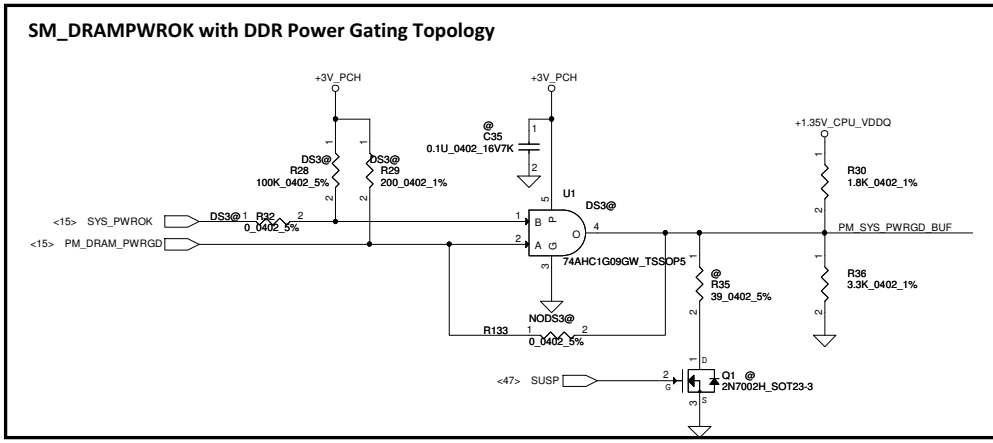
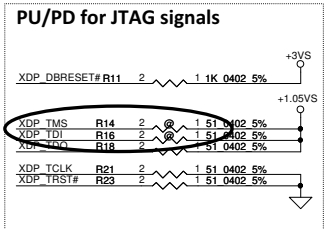
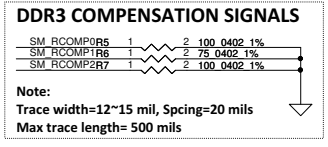
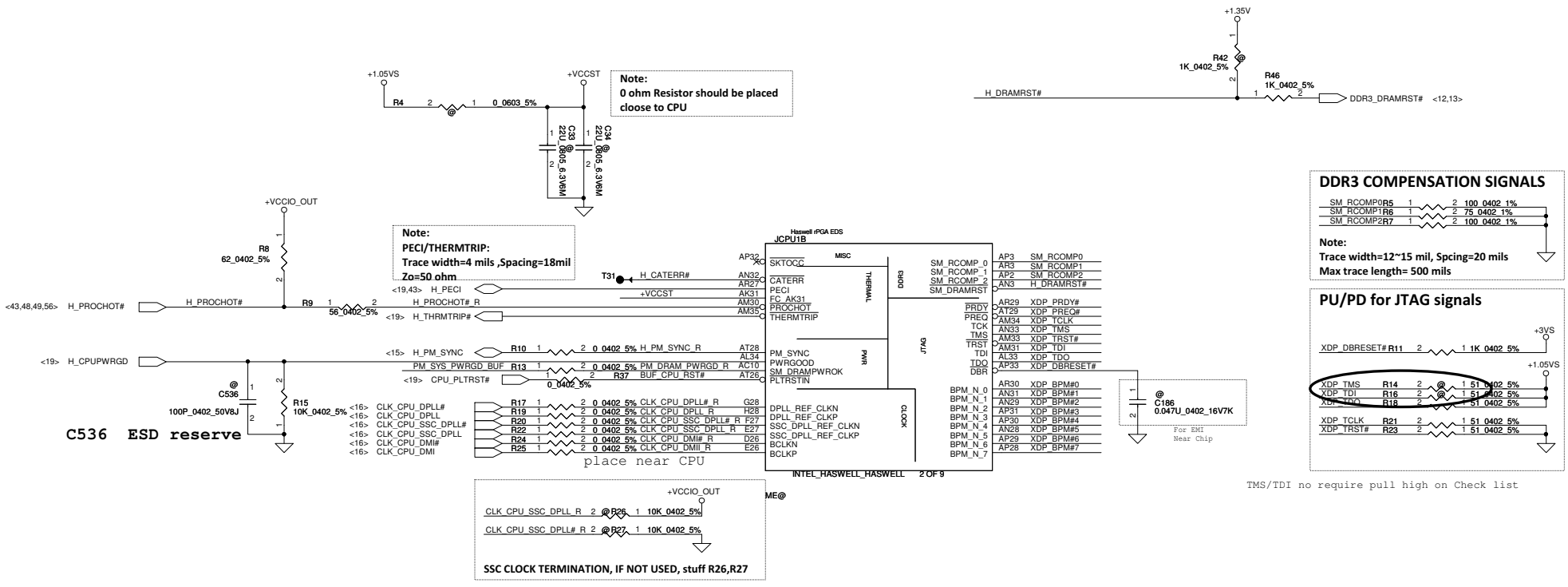


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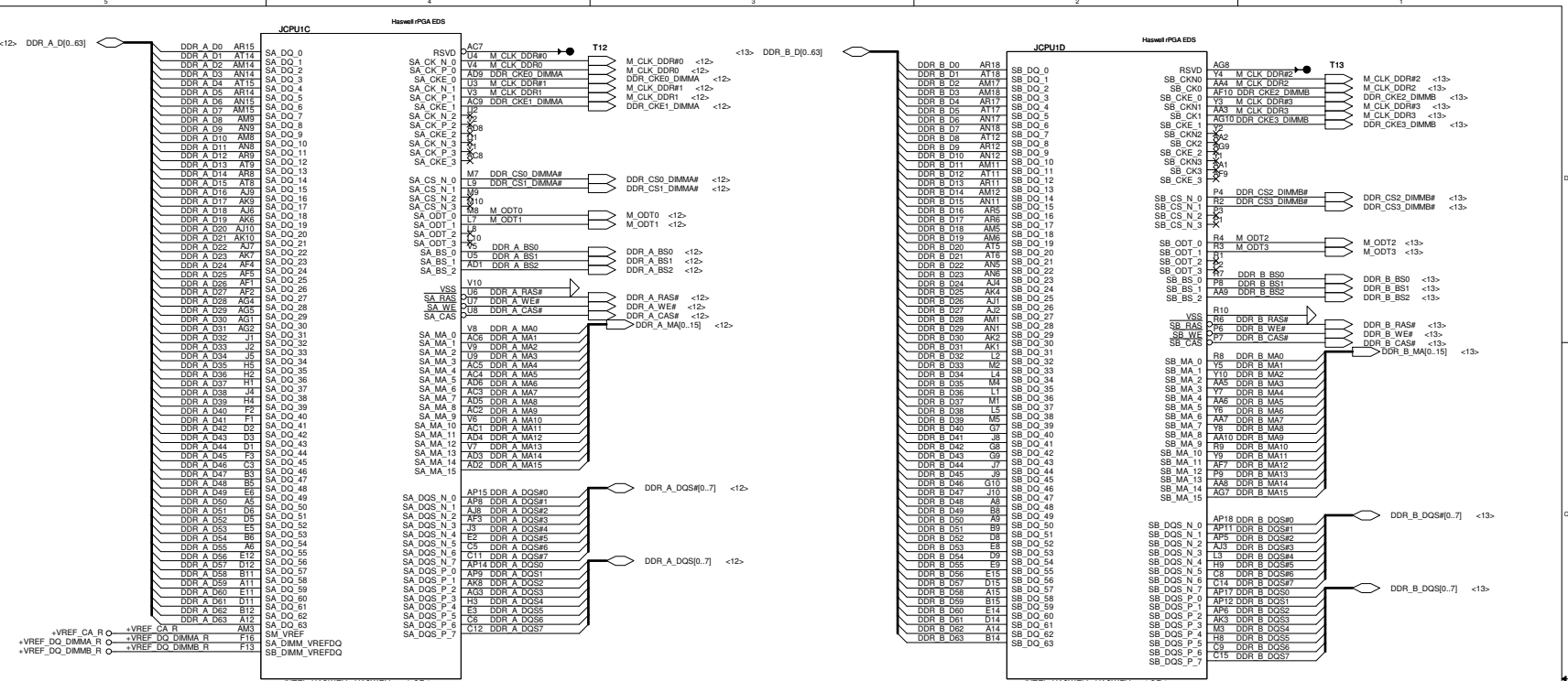


INTEL\_HASWELL\_HASWELL 1 OF 9  
ME@

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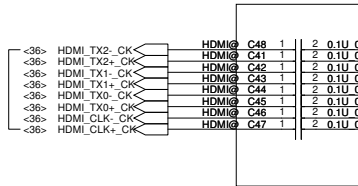
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CPI DRIVER VREF PATH IS DEFAULT

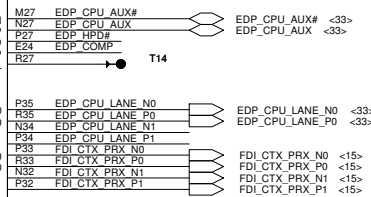
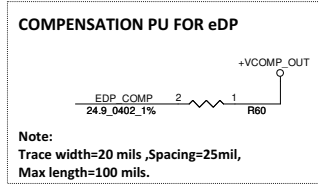
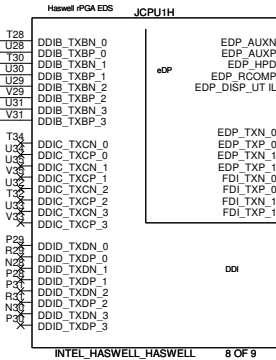
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HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

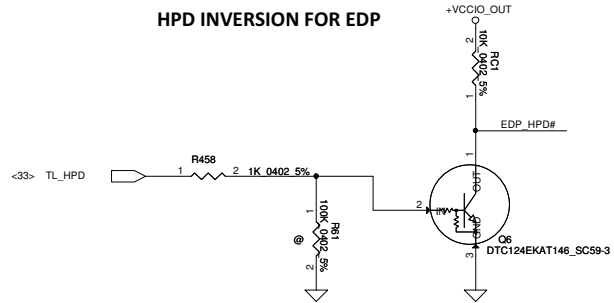
HDMI



Place on connector side



**HPD INVERSION FOR EDP**

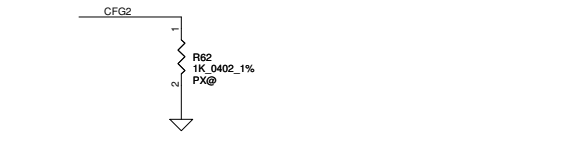
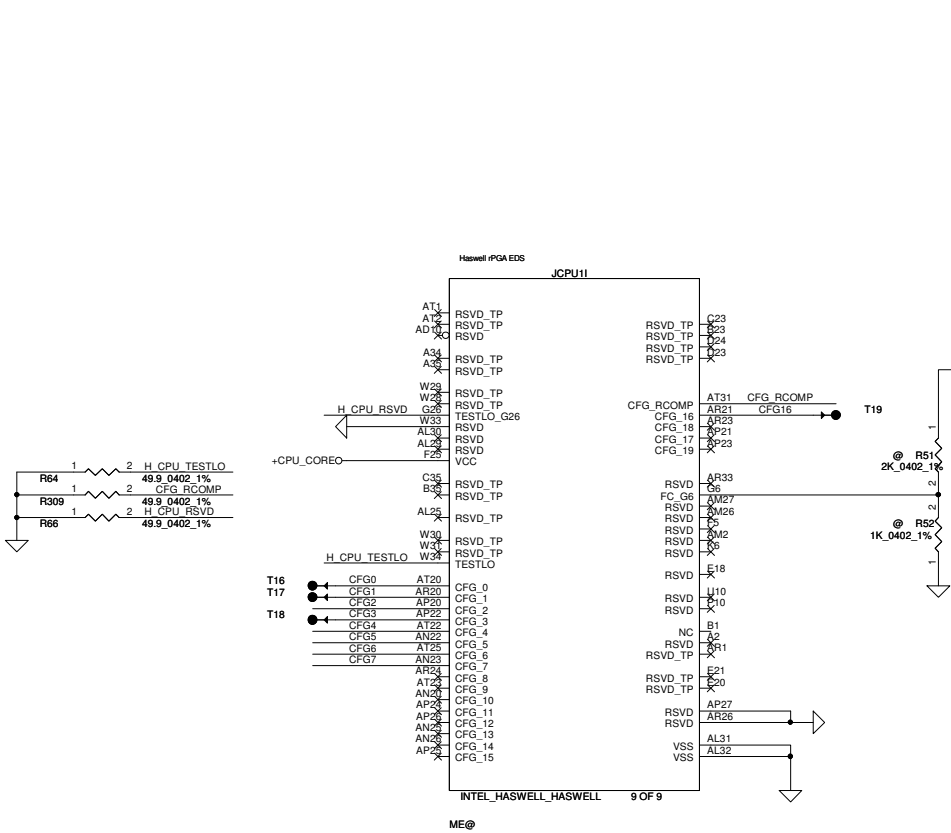


HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

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# CFG Straps for Processor



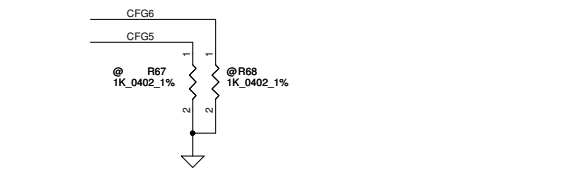
**PEG Static Lane Reversal - CFG2 is for the 16x**

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	* 0: Lane Reversed



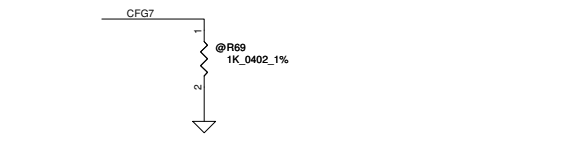
**Embedded Display Port Presence Strap**

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	* 0: Enabled; An external Display Port device is connected to the Embedded Display Port



**PCIe Port Bifurcation Straps**

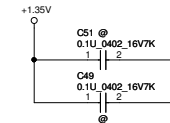
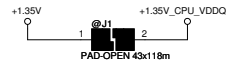
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
	00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



**PEG DEFER TRAINING**

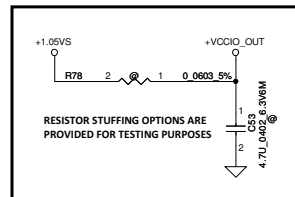
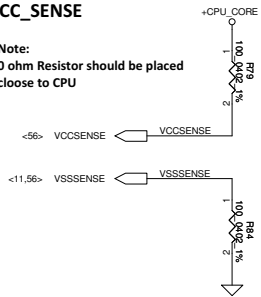
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

### +1.35V\_CPU\_VDDQ Source

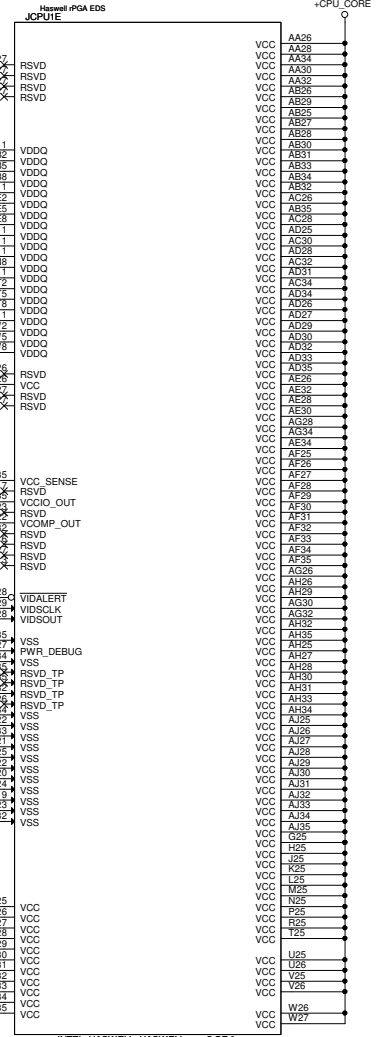
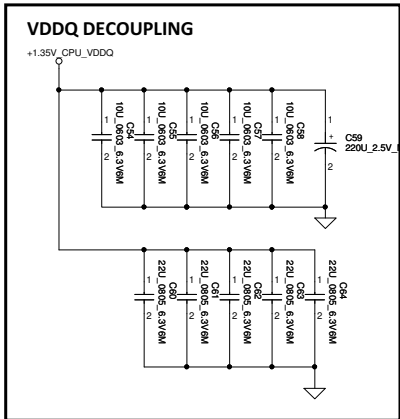
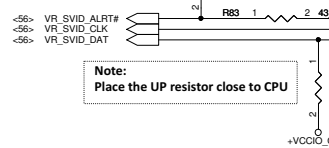


### VCC\_SENSE

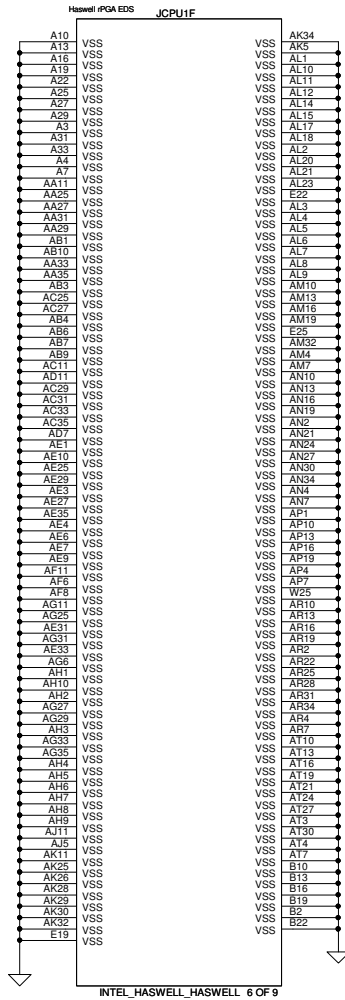
Note:  
0 ohm Resistor should be placed close to CPU



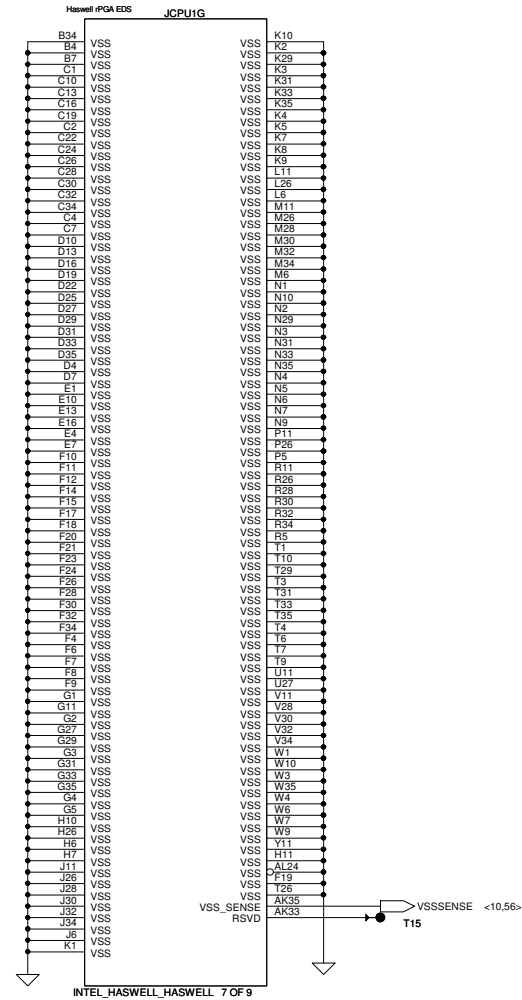
Note:  
Place the UP resistor close to CPU



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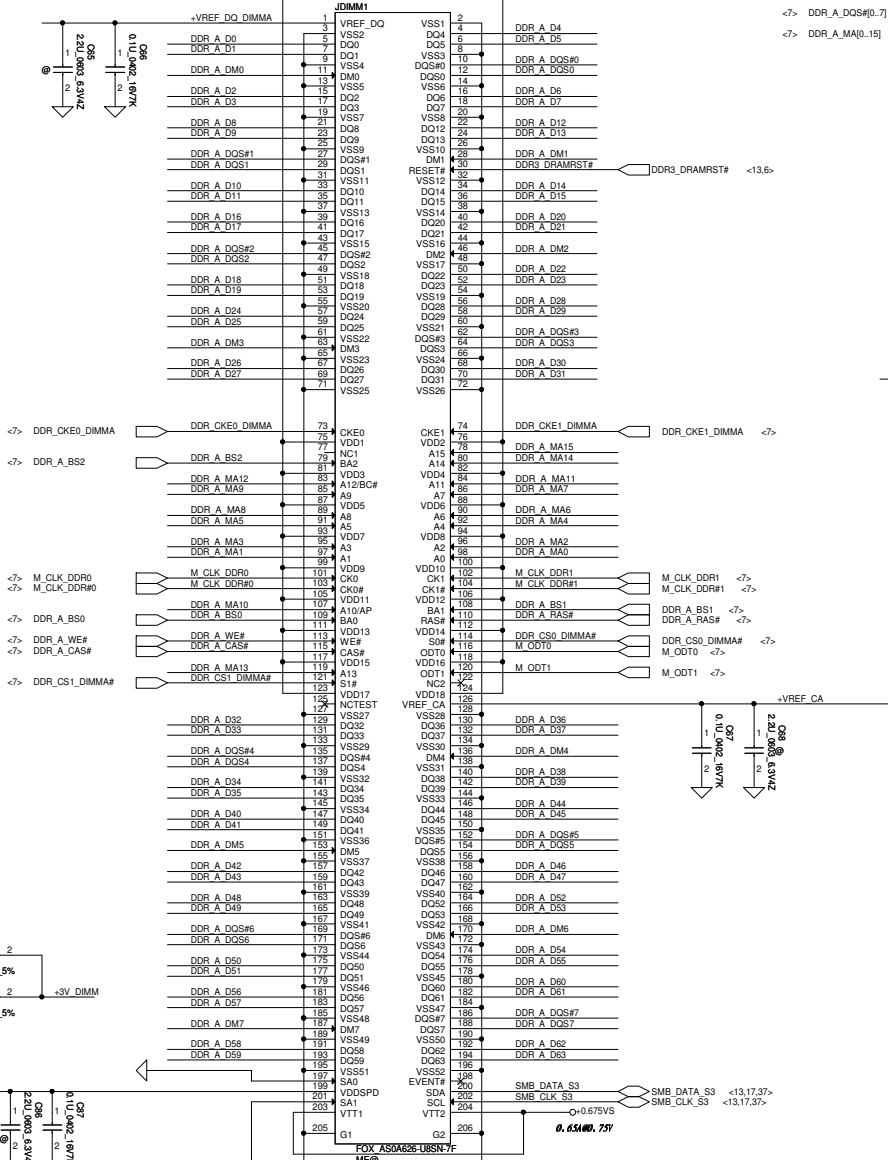
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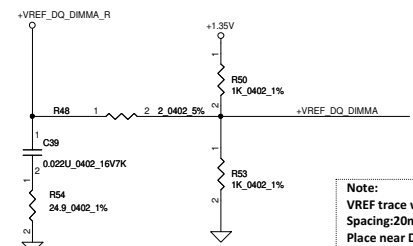
**PROCESSOR(7/7) VSS**

**LA-9641P**

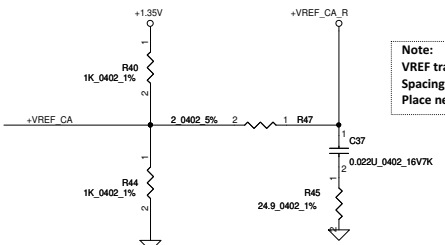
# DDR3 SO-DIMM A



- <7> DDR\_A\_D0[0..68]
- <7> DDR\_A\_DQS[0..7]
- <7> DDR\_A\_DQS#0..7]
- <7> DDR\_A\_MA0..15]

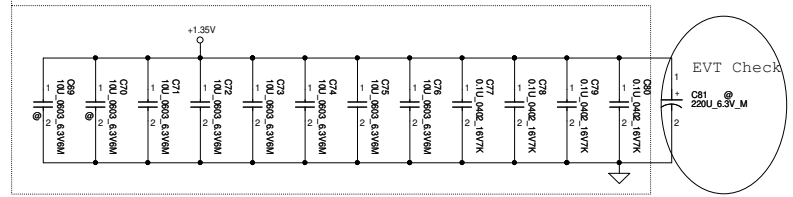


Note:  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes  
Place near DIMM socket

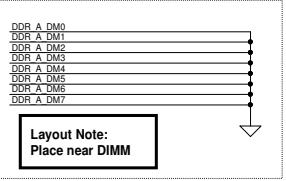
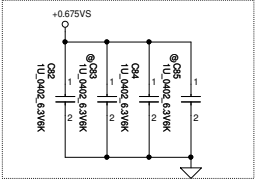


Note:  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes  
Place near DIMM socket

Layout Note:  
Place near DIMM

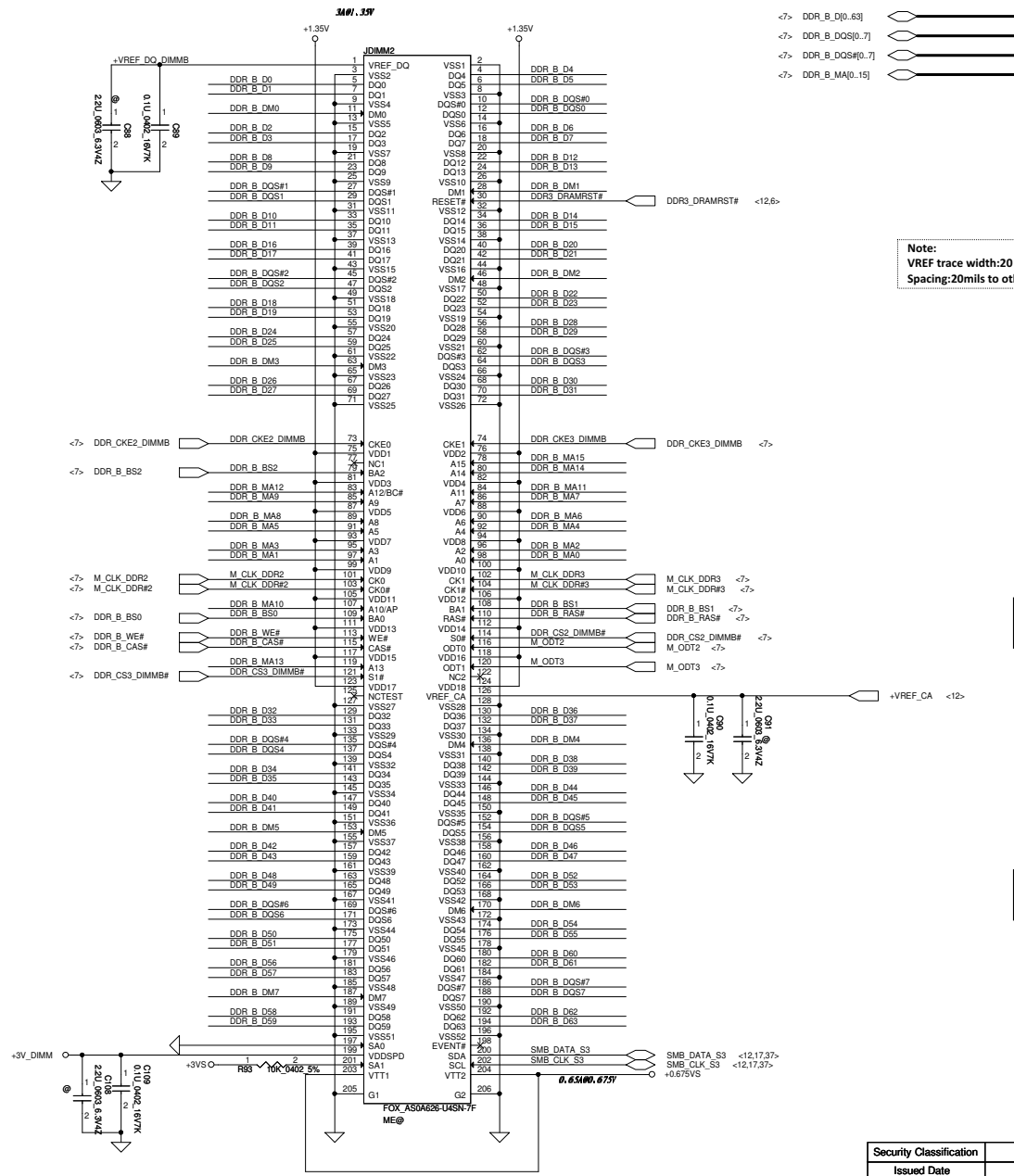


Layout Note:  
Place near DIMM



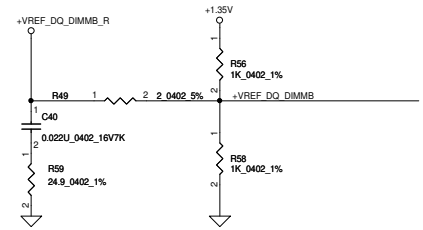
Layout Note:  
Place near DIMM

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Size Custom	Document Number	Rev	2.0		
Date:	Thursday, October 11, 2012	Sheet	12	of 60	

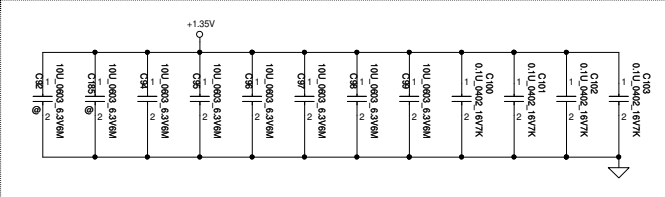


- <-> DDR\_B\_D[0..63]
- <-> DDR\_B\_DQS[0..7]
- <-> DDR\_B\_DQS#[0..7]
- <-> DDR\_B\_MA[0..15]

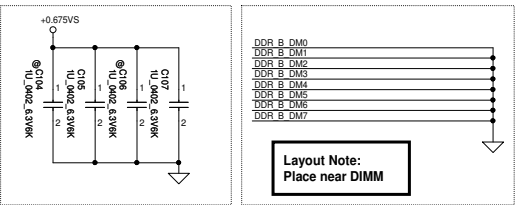
Note:  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes



Layout Note:  
Place near DIMM

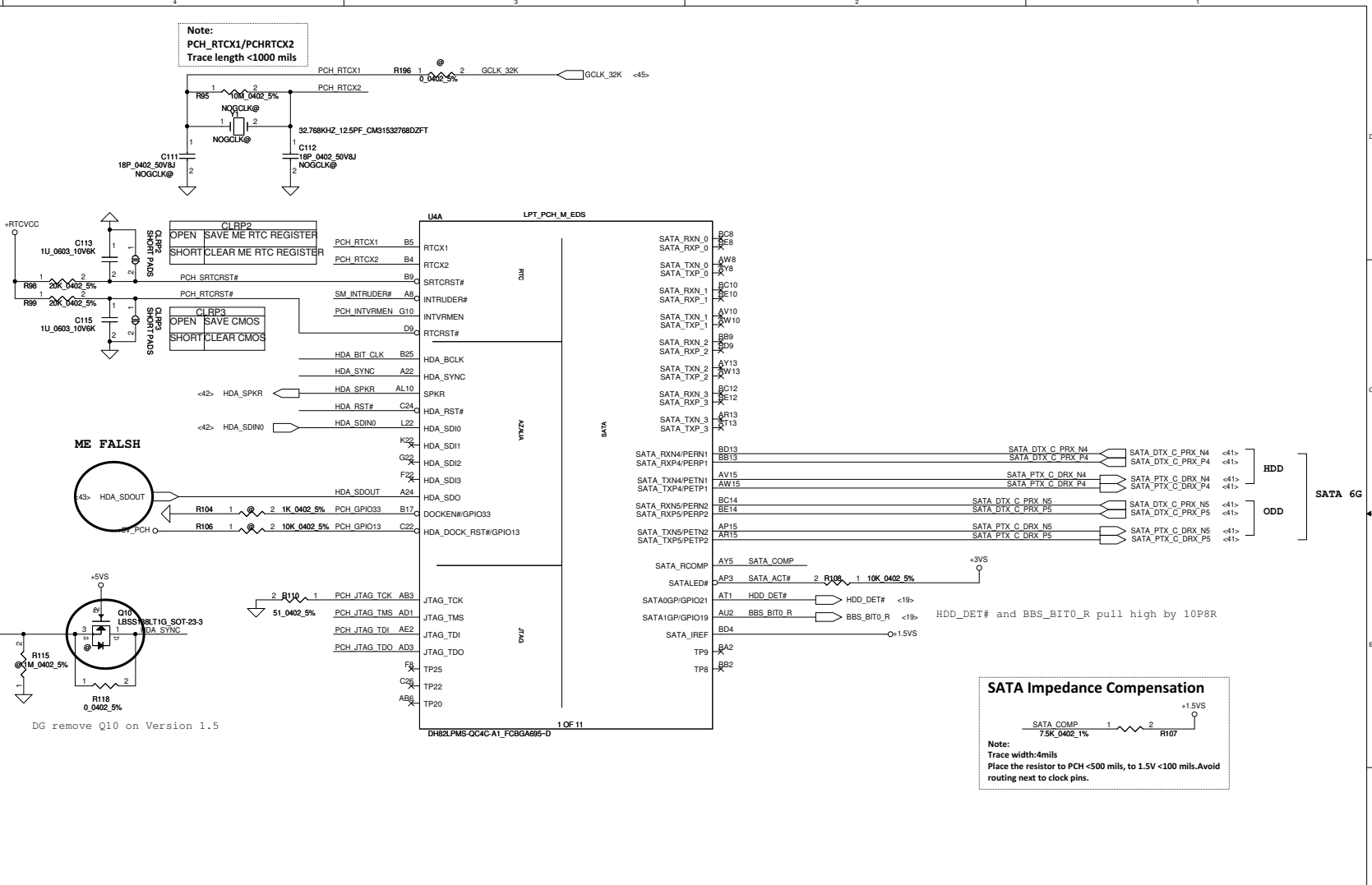
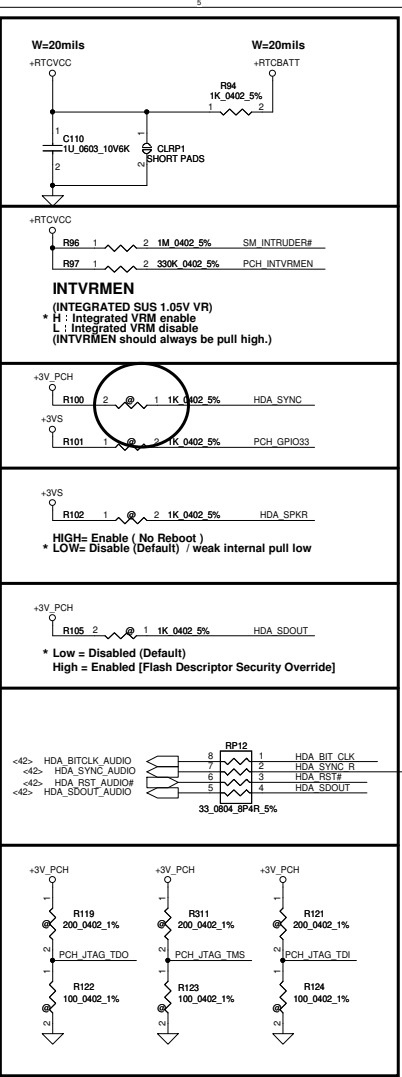


Layout Note:  
Place near DIMM

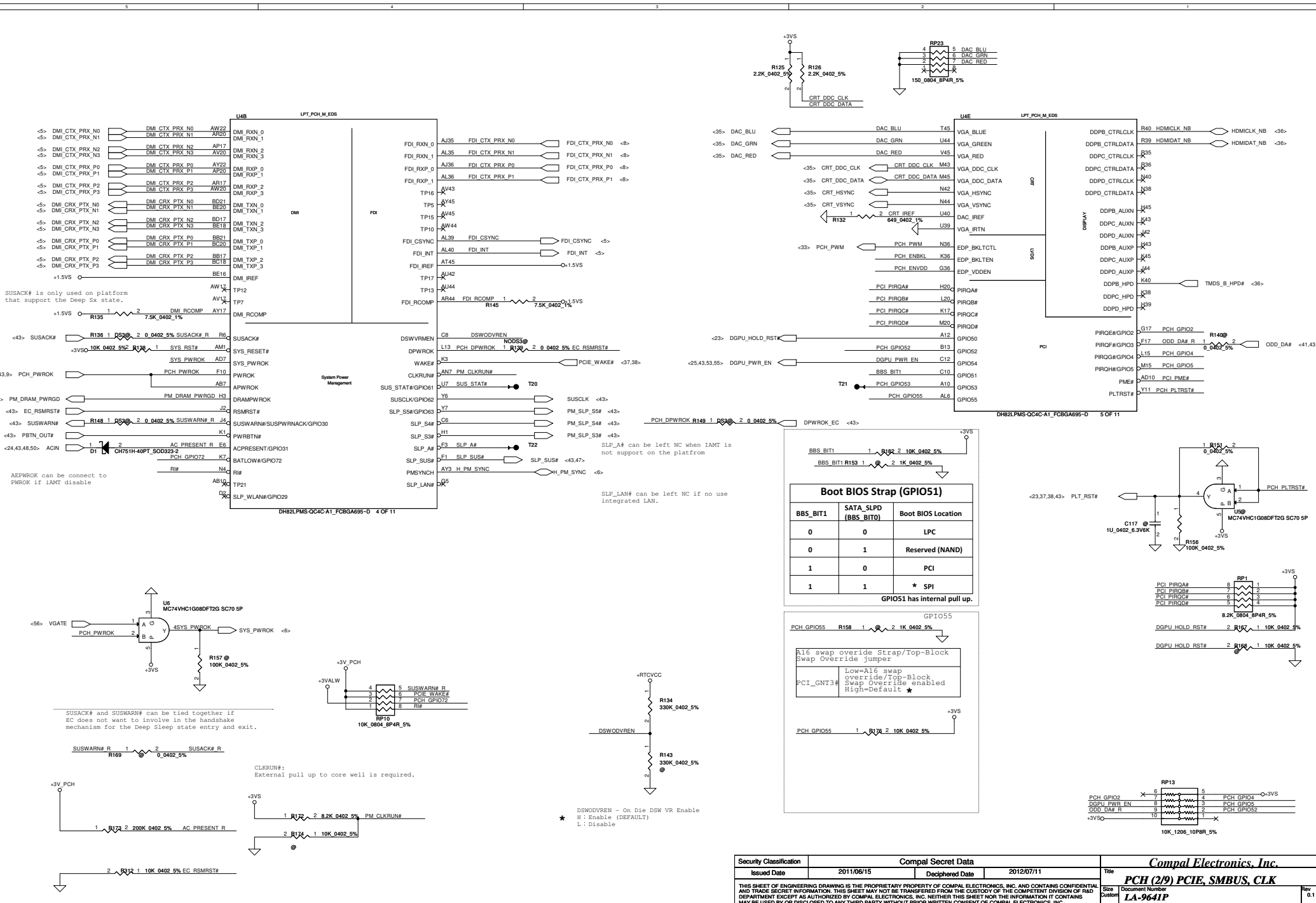


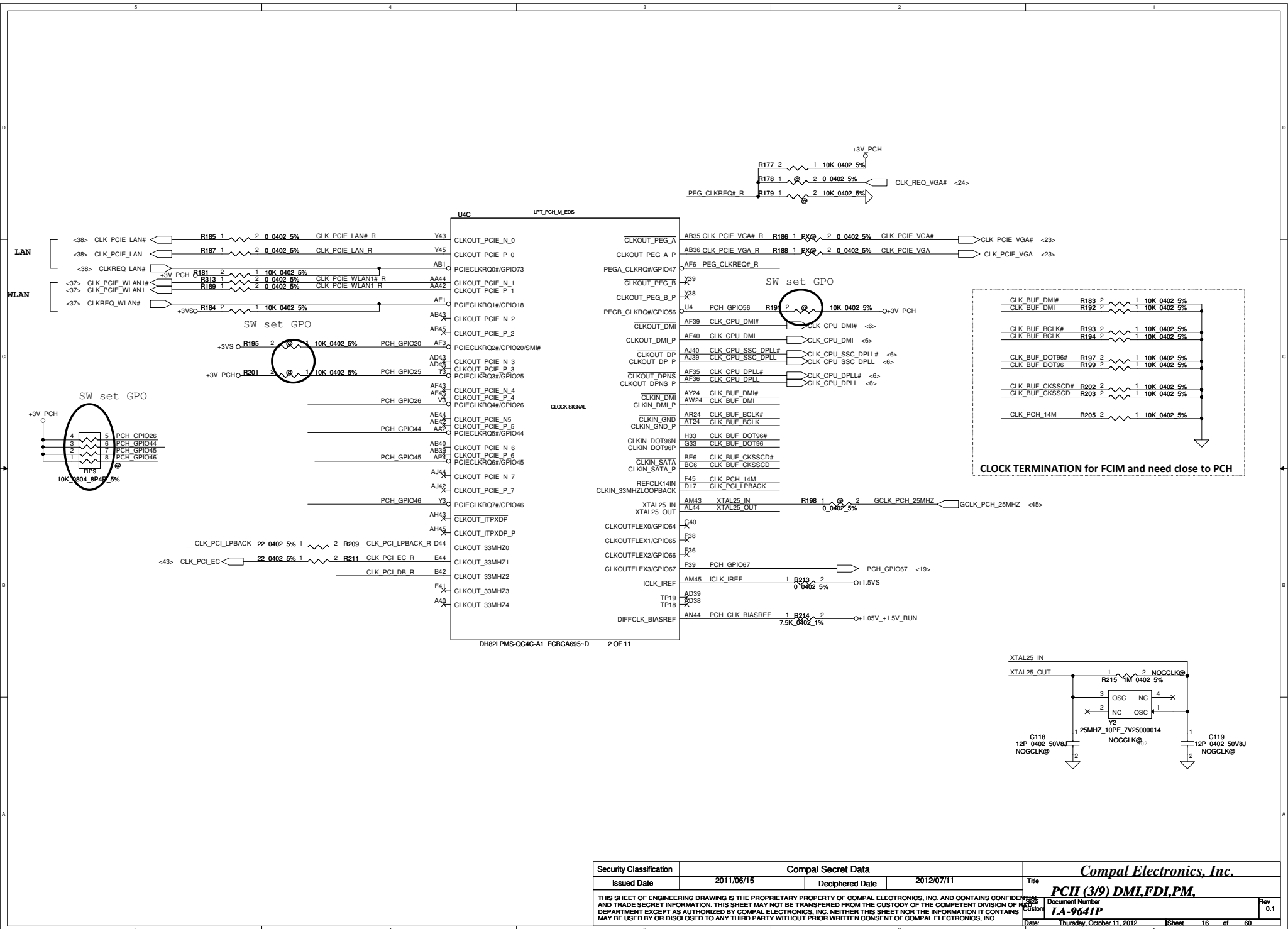
Layout Note:  
Place near DIMM

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				DDRIII-SODIMM SLOT2
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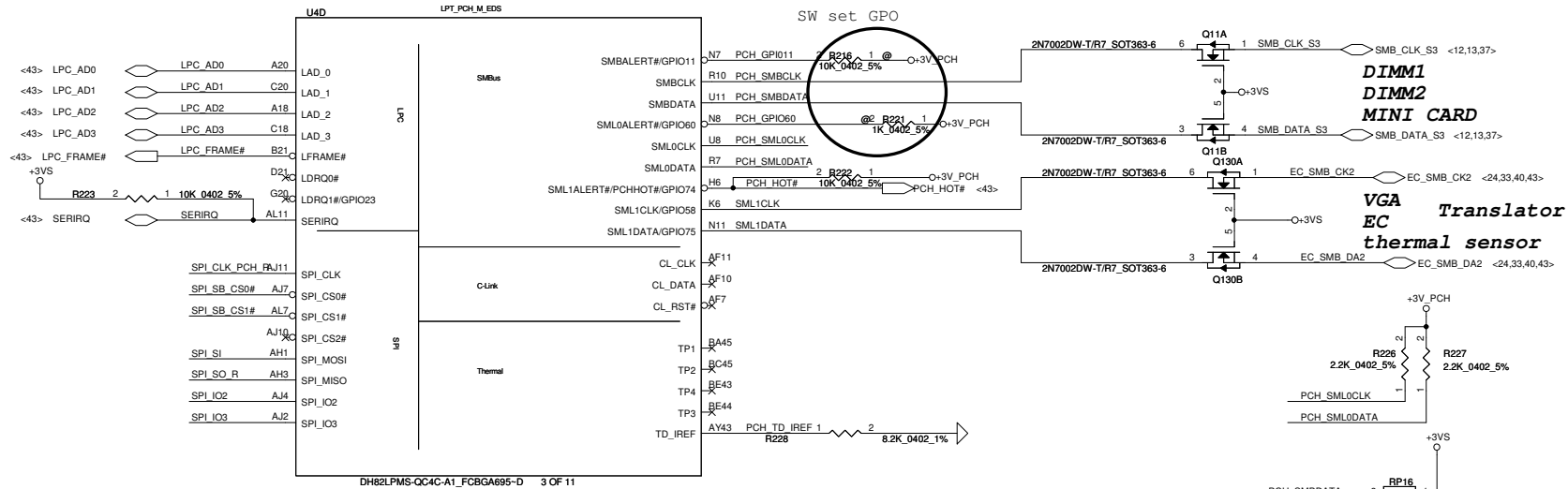
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Size	Document Number
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Customer	LA-9641P		Rev	0.1	
Date:	Thursday, October 11, 2012	Sheet	14	of 60	



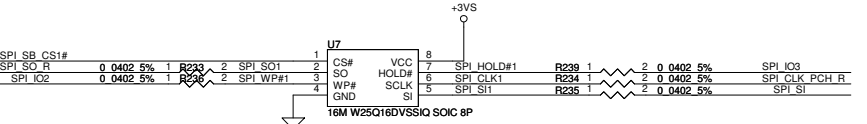
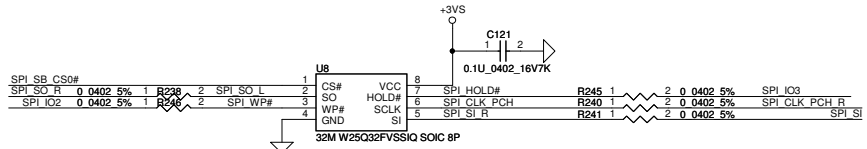
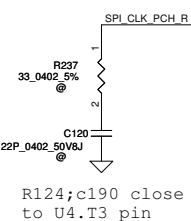
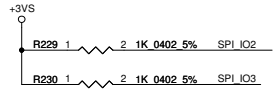


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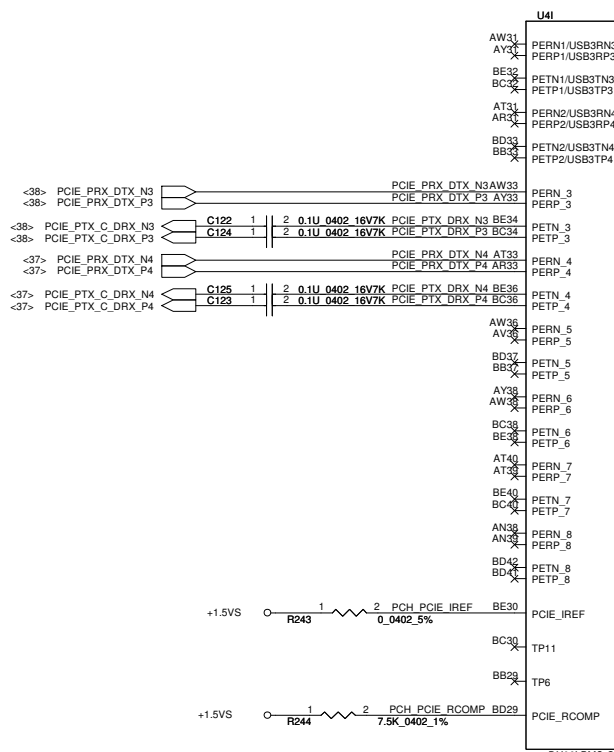


**8MB SPI ROM FOR ME & Non-share ROM.**

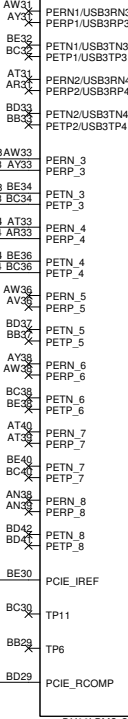


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Issued Date	2011/06/15		Deciphered Date	2012/07/11		Title		<b>PCH (A9) LVDS,CRT,DP,HDMI</b>	
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								<b>LA-9641P</b>	0.1
Date: Thursday, October 11, 2012								Sheet	17 of 60

LAN  
WLAN

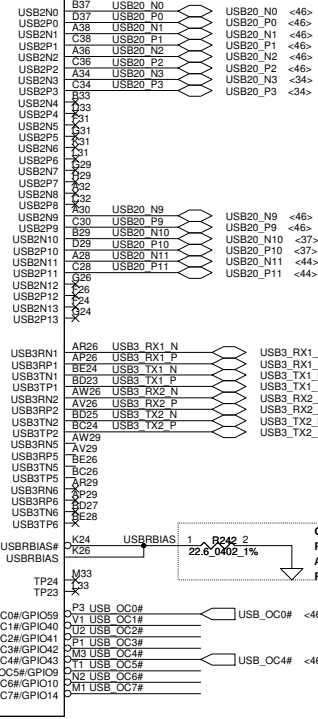


U41 LPT\_PCH\_M\_EDS



DH82LPM5-QC4C-A1\_FCBGA695-D 9 OF 11

USB DEBUG=PORT1 AND PORT9

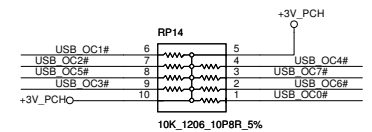


LEFT USB (USB 3.0)  
LEFT USB  
Touch panel  
USB Camera

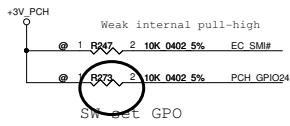
RIGHT USB  
WLAN  
CARD READER

EHCI 1  
EHCI 2

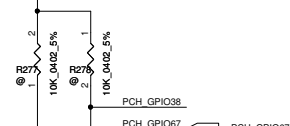
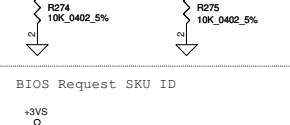
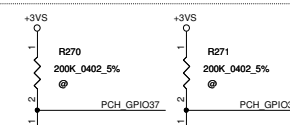
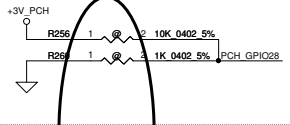
CAD NOTE:  
Route single-end 50-ohms and max 500-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils.



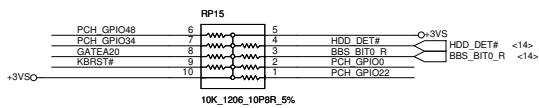
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			Date:	Thursday, October 11, 2012	Sheet 18 of 60



Remove strap description  
inform SW set GPO



PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	UMA
1	1	DIS

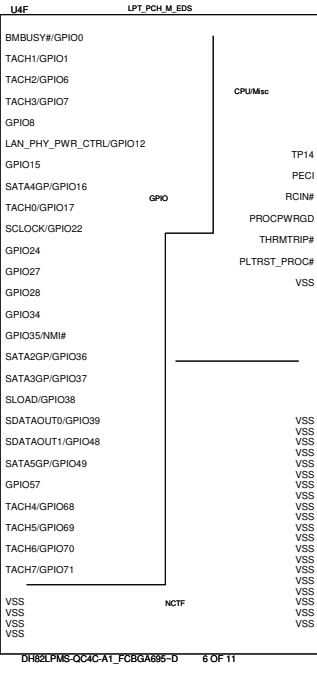
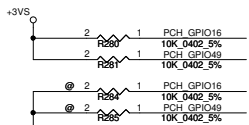


SW set GPO

Check Behavior

SW set GPO

<43> EC\_LID\_OUT#  
<55> DGPU\_PWROK  
PU on power side



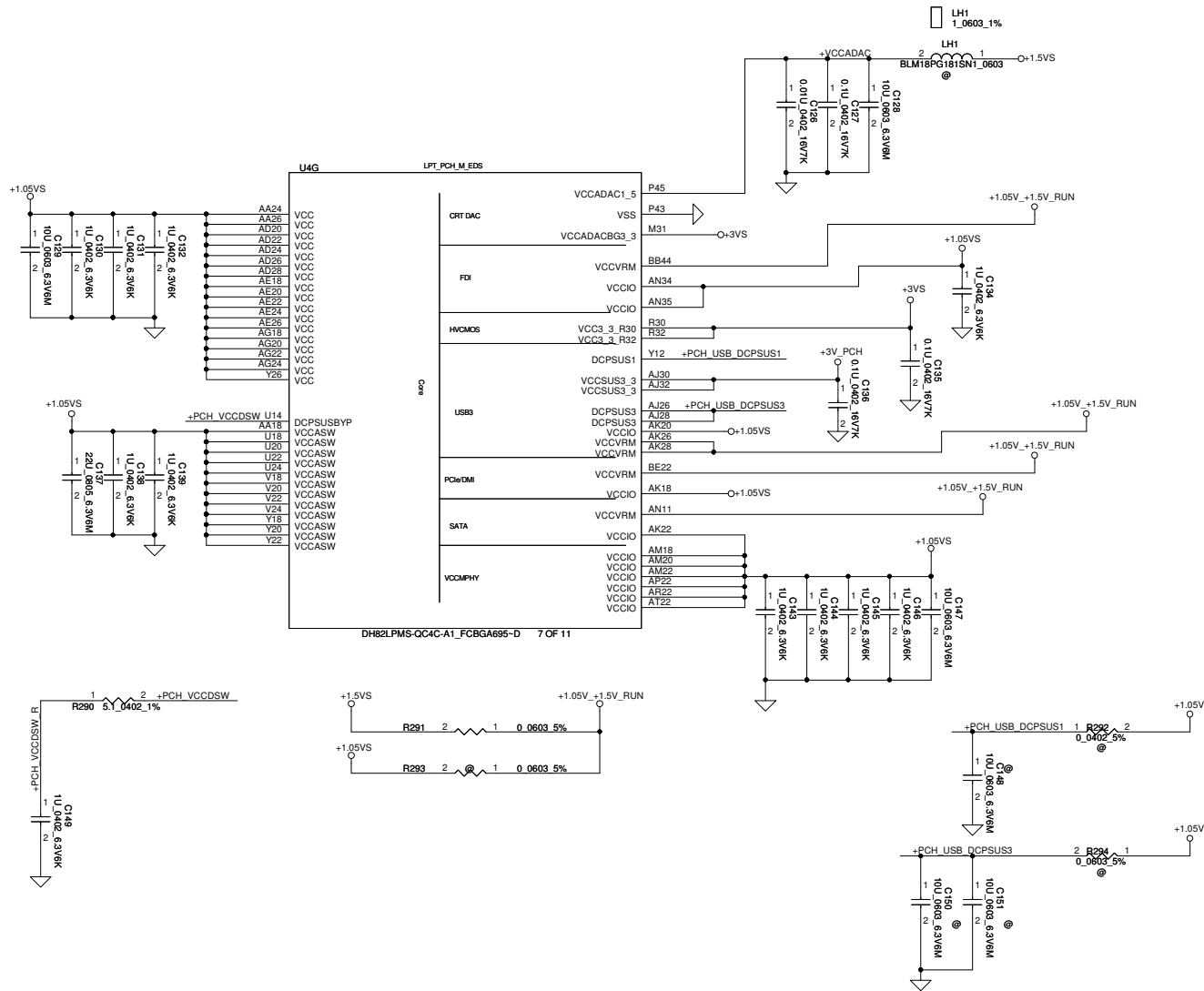
Config	GPIO16 & 49
USB3.0 x4, PCIE x8, SATA x6	11
USB3.0 x6, PCIE x8, SATA x4	01

Fixed Signals	Mixed Signals	Fixed Signals	Mixed Signals	Fixed Signals

Need Update

PCH_GPIO69	Function
0	
1	

PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	SUN PRO
1	Mars XT

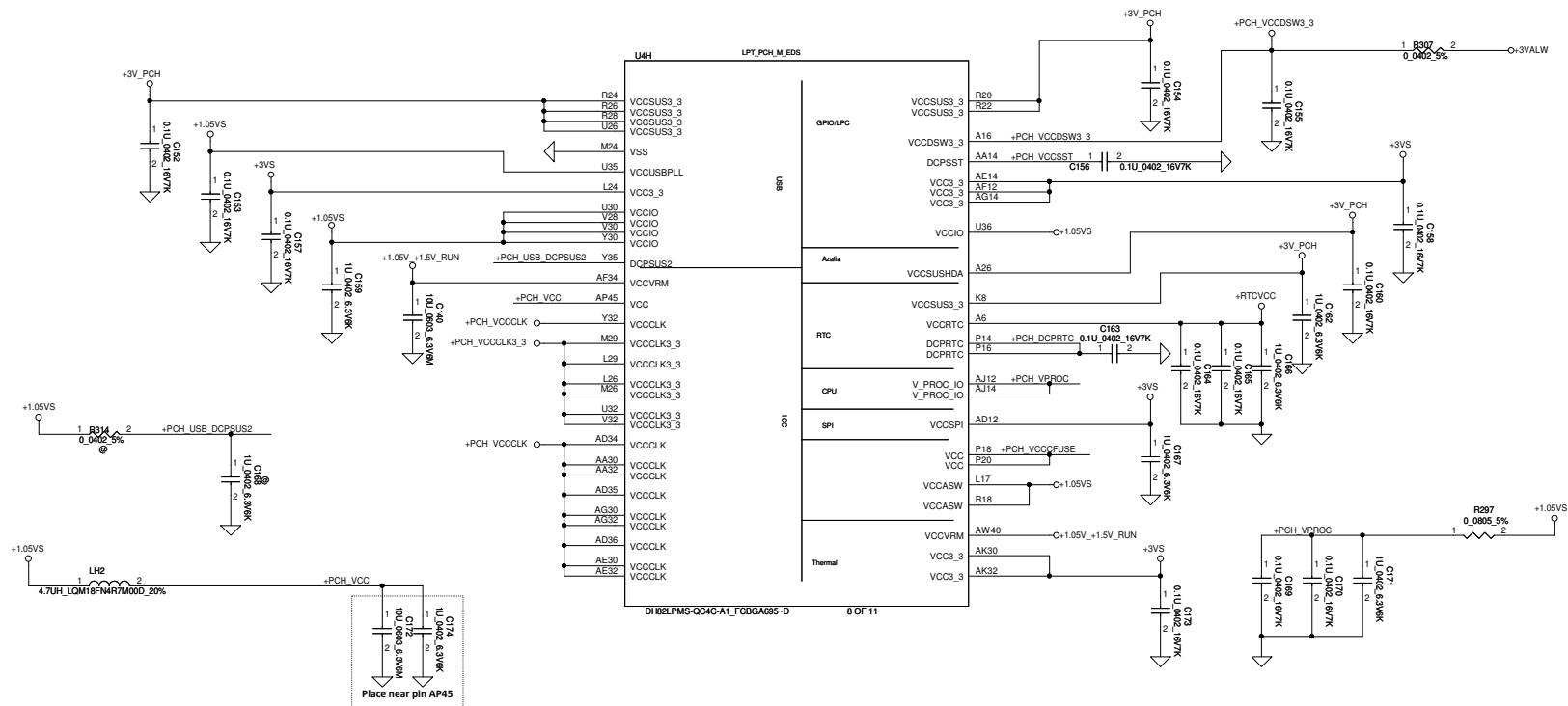


PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

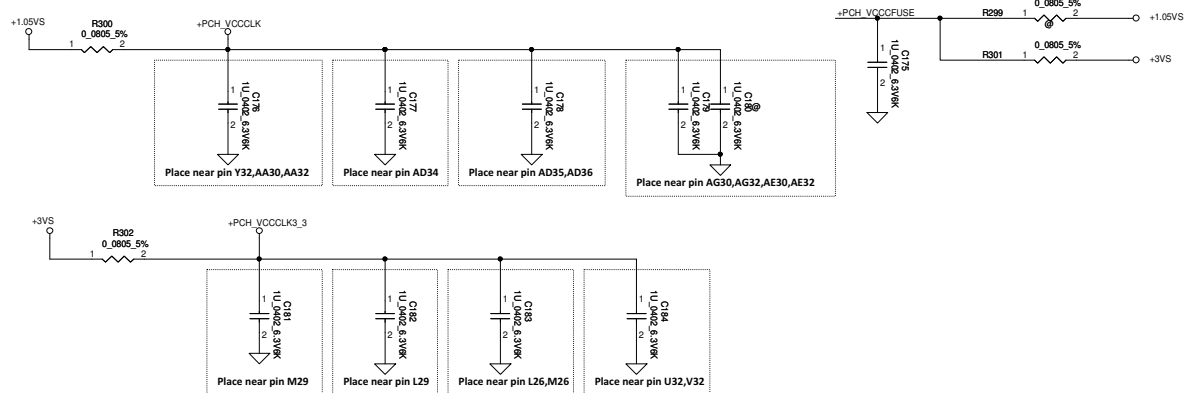
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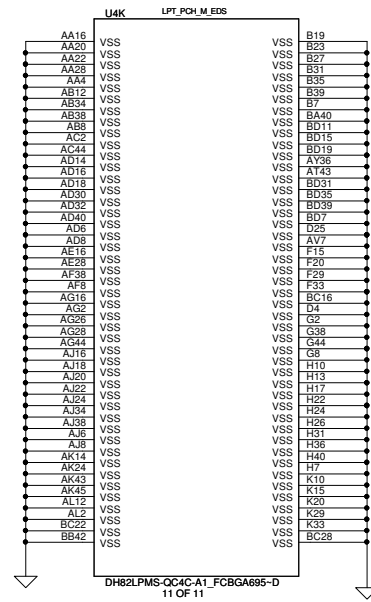
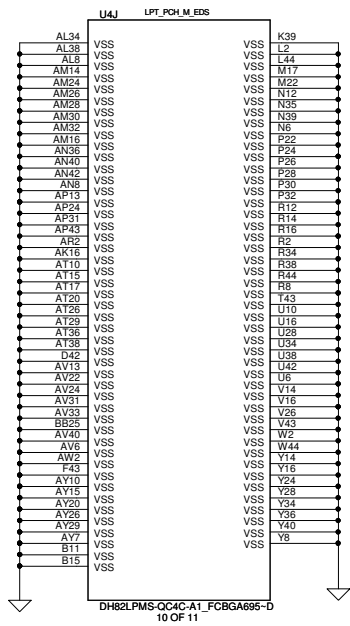
Compal Electronics, Inc.	
Title	<b>PCH (7/9) PWR</b>
Document Number	<b>LA-9641P</b>
Date	Thursday, October 11, 2012
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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



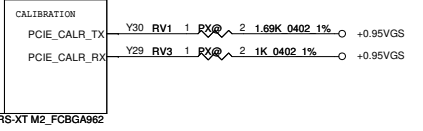
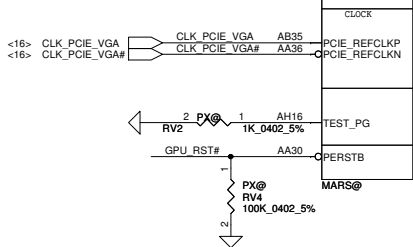
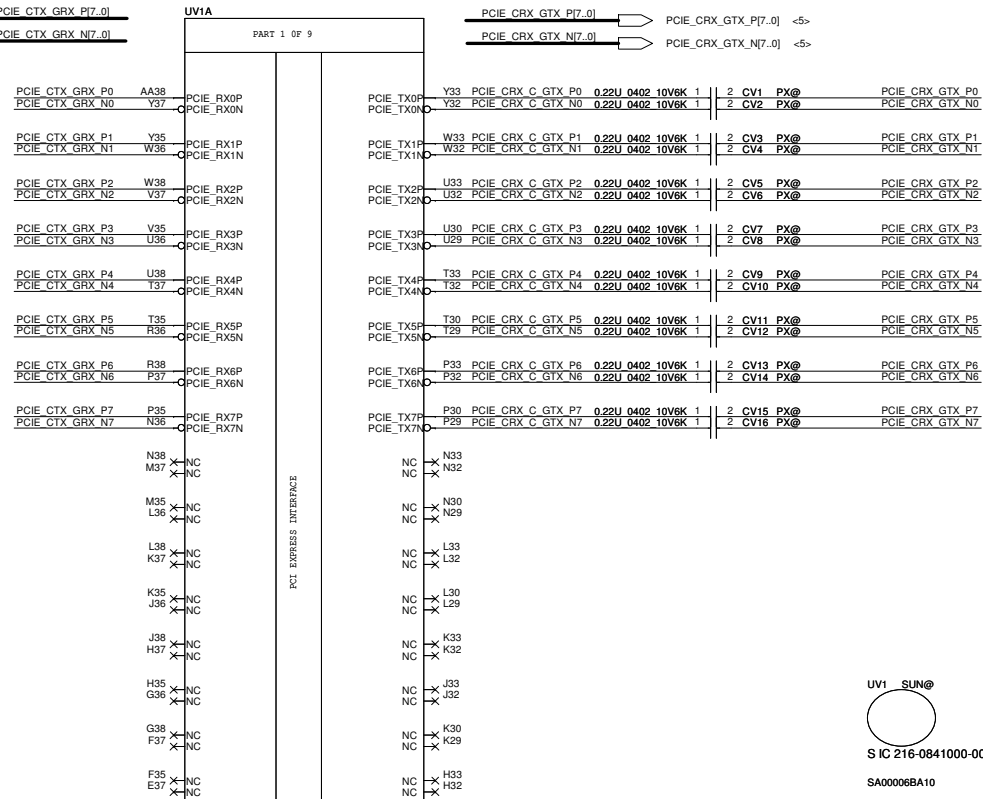
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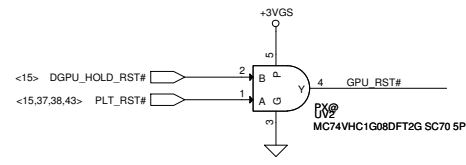
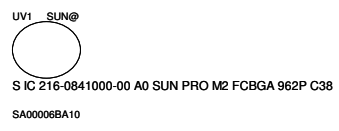
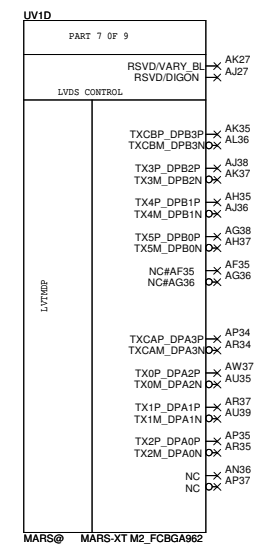
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<5> PCIE\_CTX\_GRX\_P[7..0] PCIE\_CTX\_GRX\_P[7..0]  
 <5> PCIE\_CTX\_GRX\_N[7..0] PCIE\_CTX\_GRX\_N[7..0]

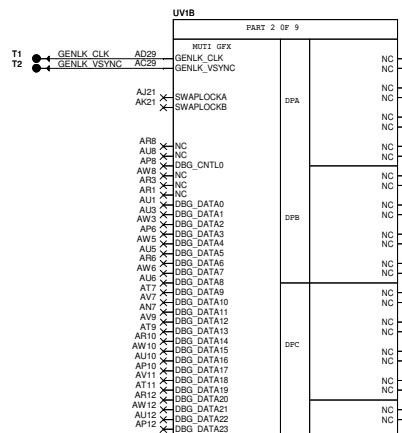
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 PCIE\_CRX\_GTX\_N[7..0] PCIE\_CRX\_GTX\_N[7..0] <5>



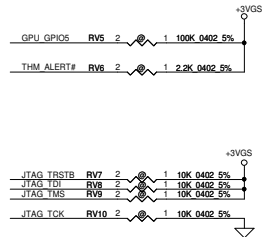
### LVDS Interface



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### STRAPS



AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

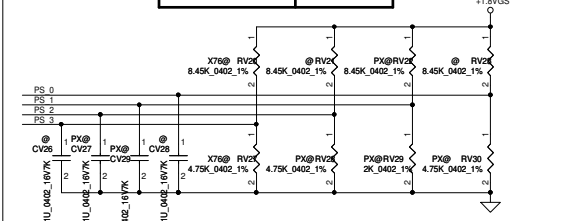
VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0.50% Tx output swing 1.Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0.7x de-emphasis disabled 1.Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE RESERVED FOR Thames/Seymour and should be strapped to 0)	1
BIF_VGA_DIS	PS_2[4]	VGA control 0.VGA controller capacity enabled (for multi-GPU) 1.VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3:1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 101 - 5120x M2SP5A (ST) 101 - 1Mbit M2SP10A (ST) 101 - 2Mbit M2SP20 (ST) 101 - 4Mbit M2SP40 (ST) 101 - 8Mbit M2SP80 (ST) 100 - 5120x Pm2SLV010 (Chingis) 101 - 1Mbit Pm2SLV010 (Chingis)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0.Disabled 1.Enabled	0
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI  HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whisper/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

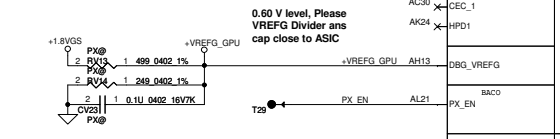
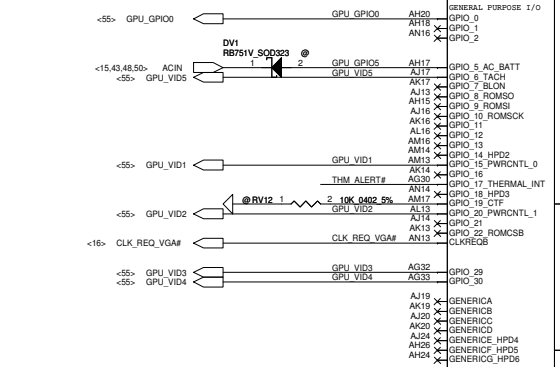
### MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_1[5:1]	0 1	0 0 1	82 nF	8.45K	2K
PS_2[5:1]	1 0	0 0 0	10 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 4

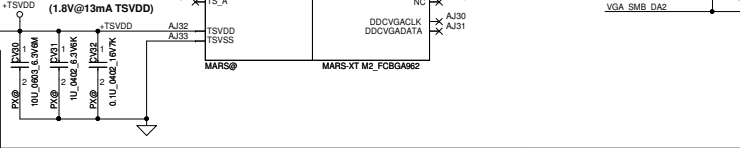


Place CLOSE VGA CHIP



GPIO 28_FDO	MLPS
H	Disable
L	Enable

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



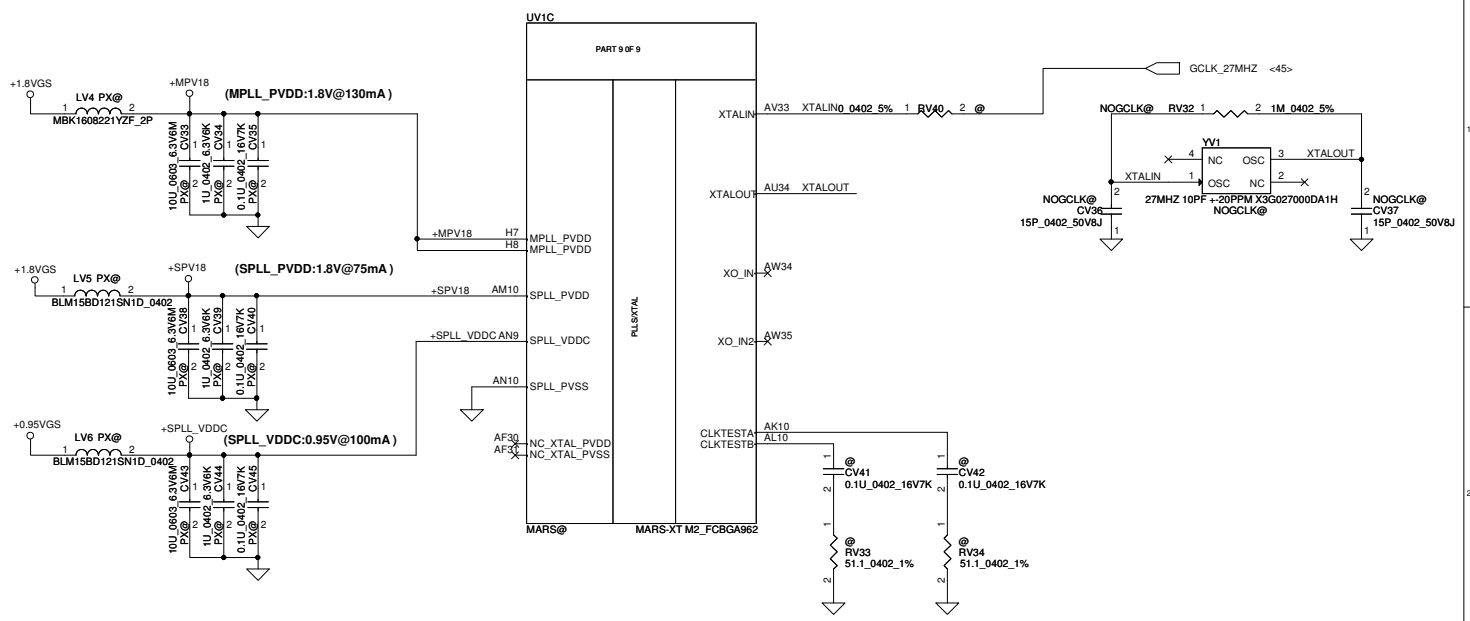
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Compal Electronics, Inc.			ATI MarsXTX M2 Main MSIC	
Size C	Document Number	LA8642P M/B		Rev 0.1
Date:	Thursday, October 11, 2012	Sheet	24	of 60



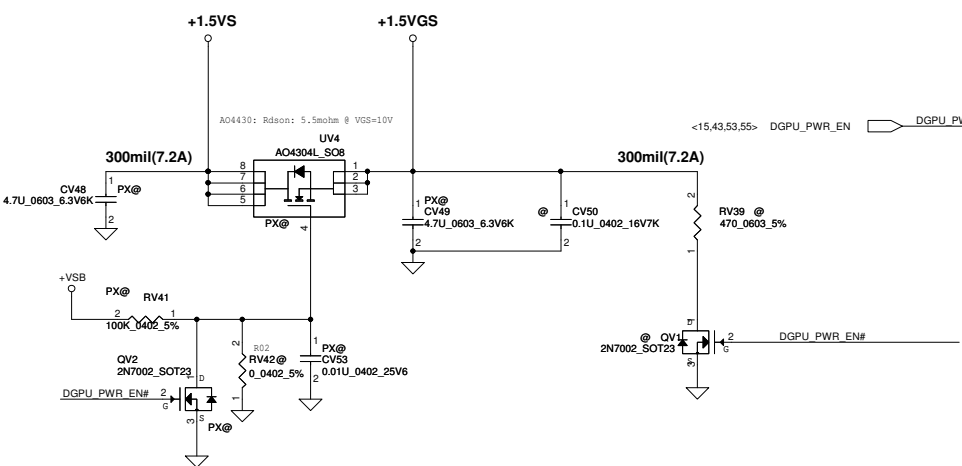
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

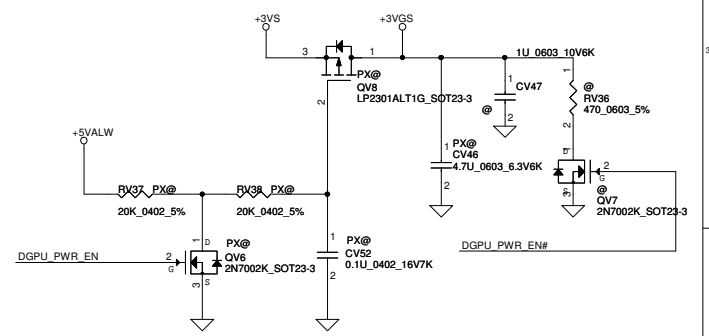
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



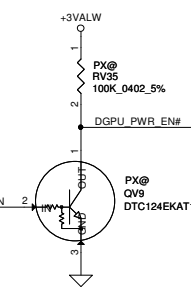
**+1.5VS to +1.5VGS Transfer**



**<+3VS TO +3VGS>**

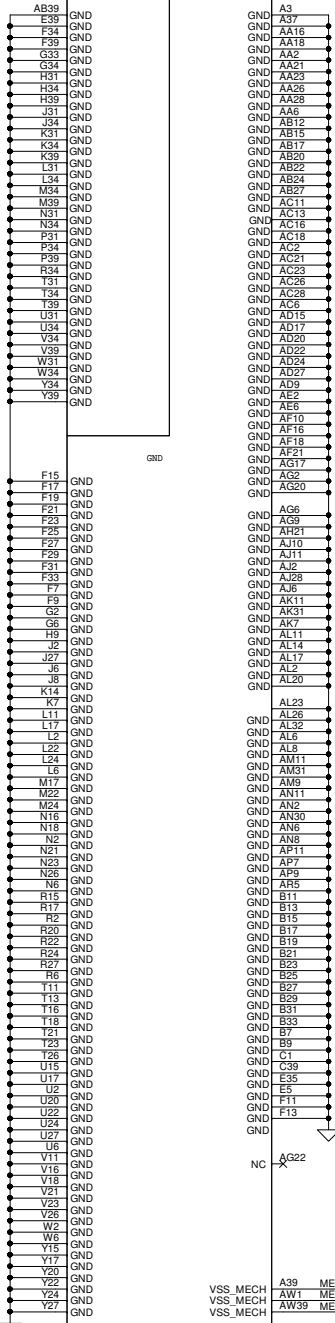


**Need OPEN**

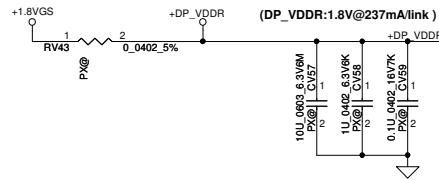


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Date: Thursday, October 11, 2012				Sheet 25 of 60

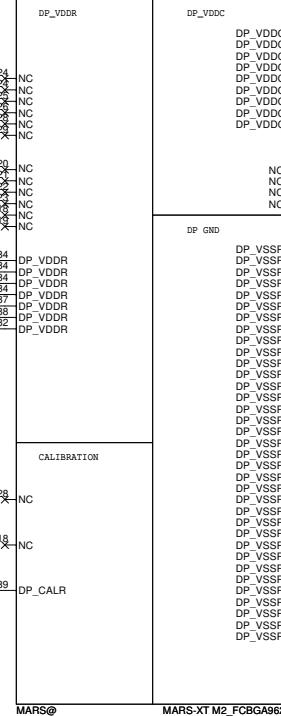
UVIG PART 6 OF 9



DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

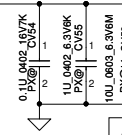


UVIF PART 8 OF 9

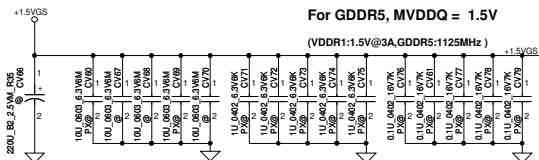


(DP\_VDDC:0.95V@280mA/link)

DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1



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Date: Thursday, October 11, 2012				Sheet 26 of 60

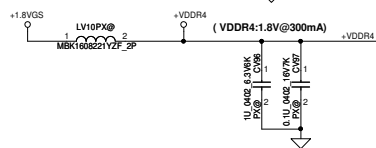
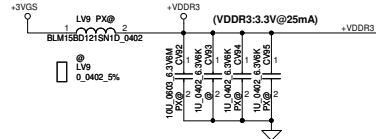
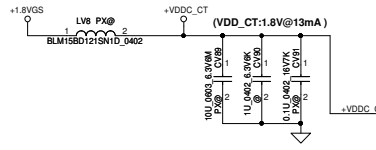


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

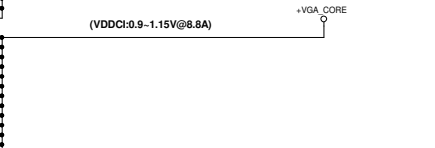
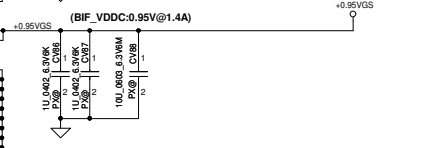
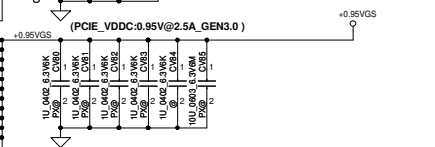
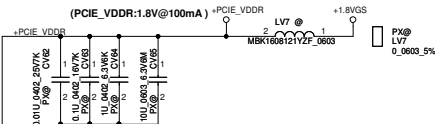
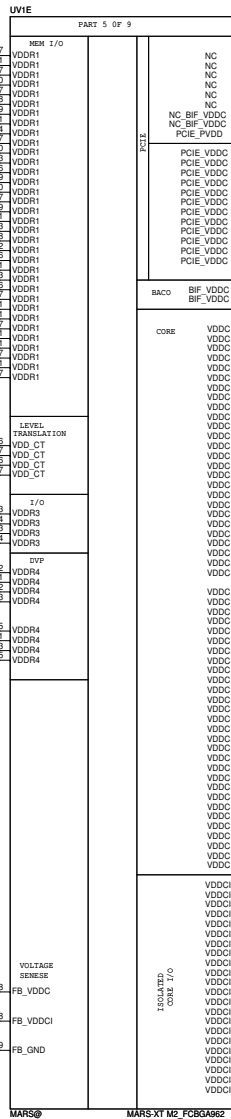
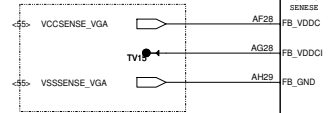
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



Route as differential pair

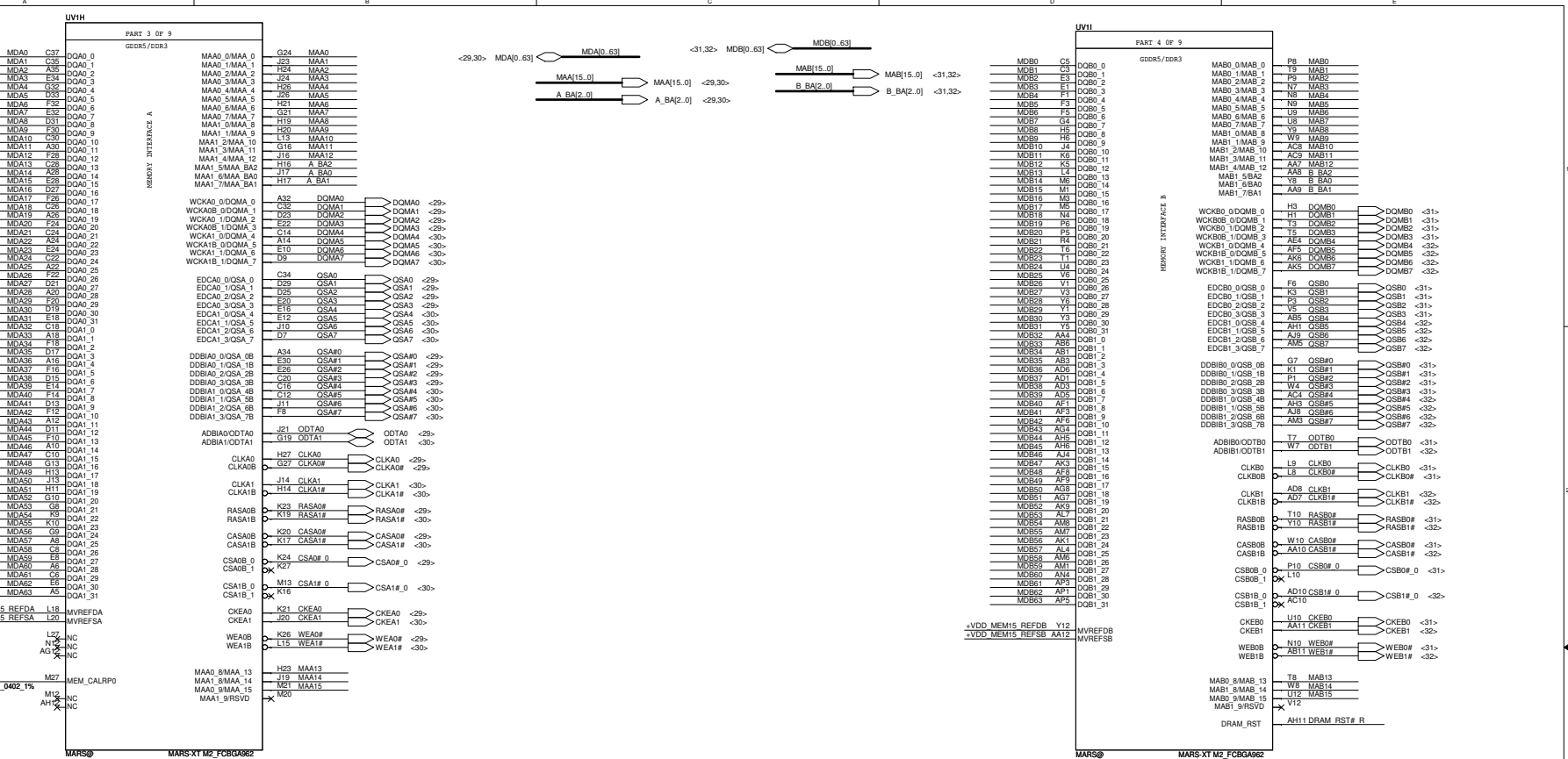


PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

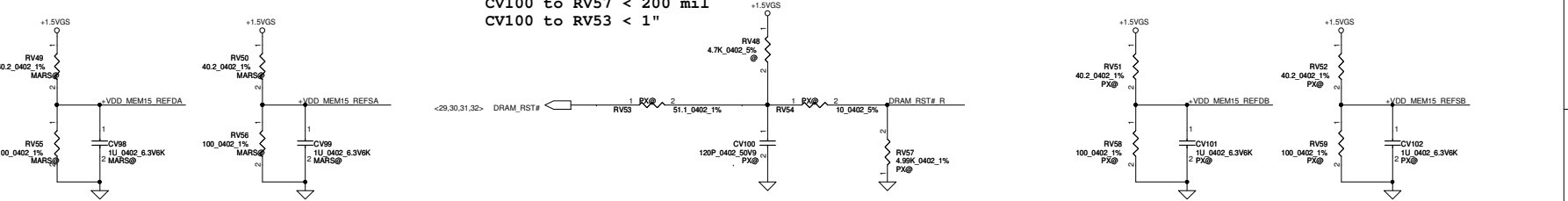
PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VGA\_CORE Cap in power side sheet

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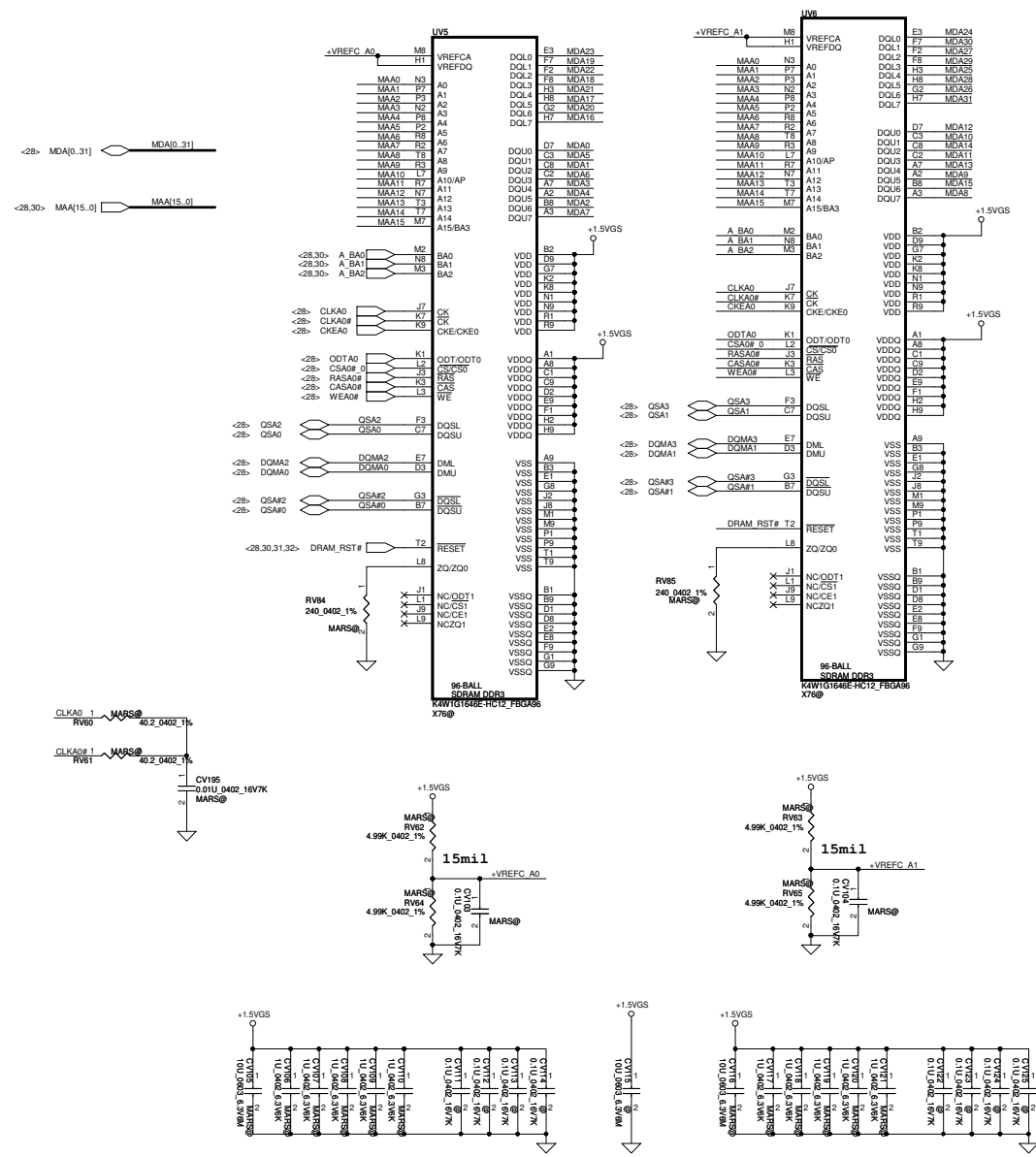
Ball to RV57 < 1"  
 CV100 to RV57 < 200 mil  
 CV100 to RV53 < 1"

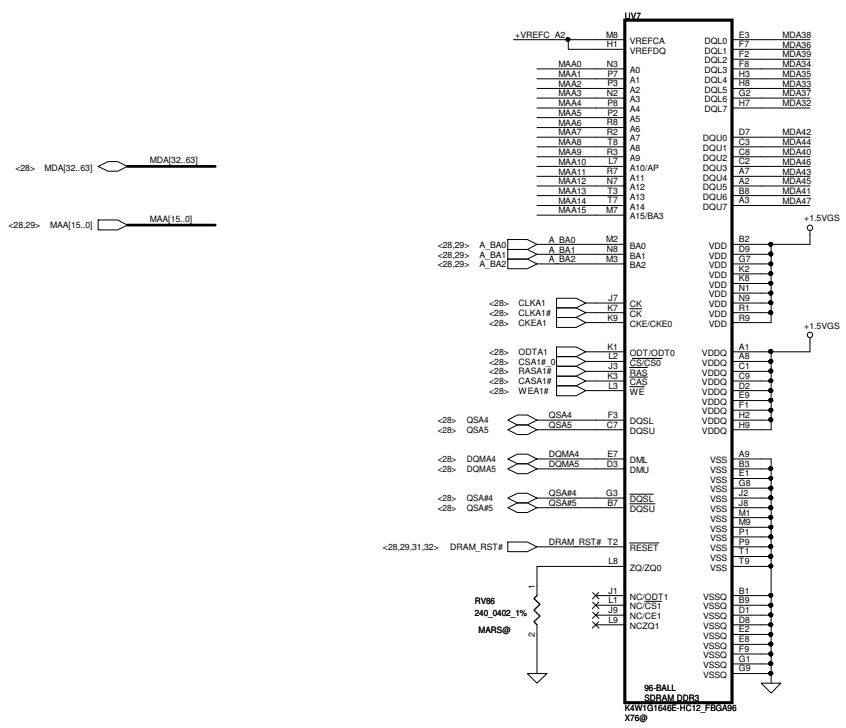


**DRAM\_RST is a daisy-chain net that connects to all VRAM**

This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and U cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

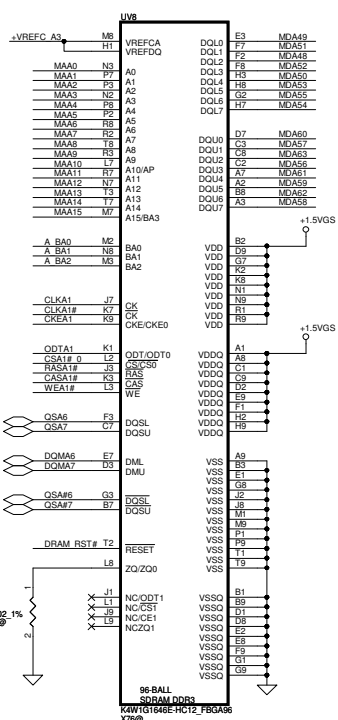
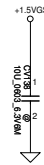
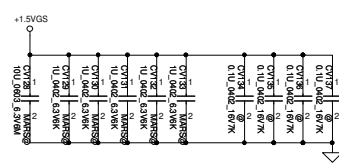
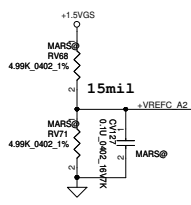
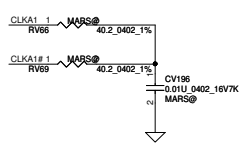
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Size	C	Document Number	LA8642P/M/B	Rev	0.1
Date:	Thursday, October 11, 2012	Sheet	28	of	60





<28> MDA[32..63]

<28,29> MAA[15..0]



<28> OSA6

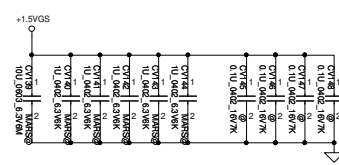
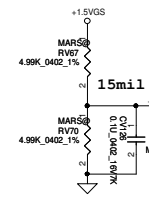
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<28> DQMA6

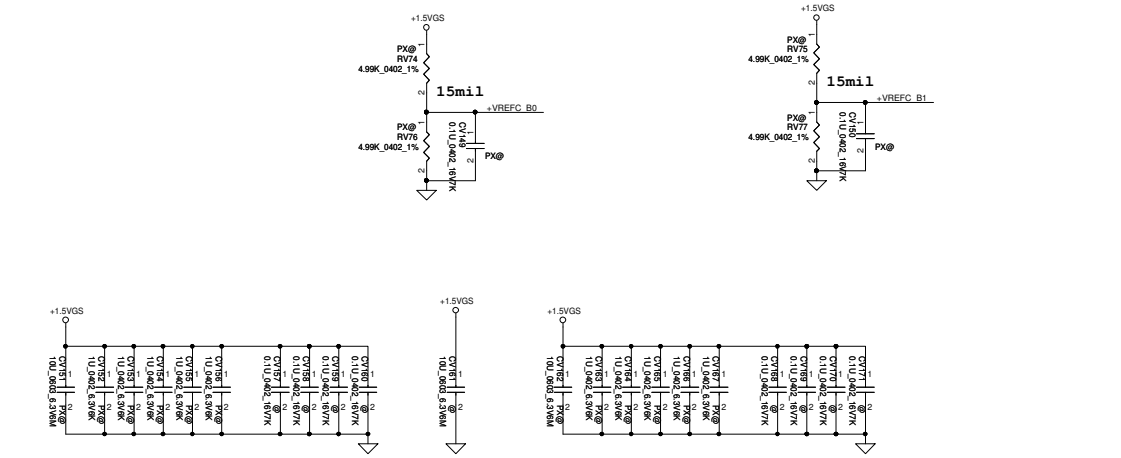
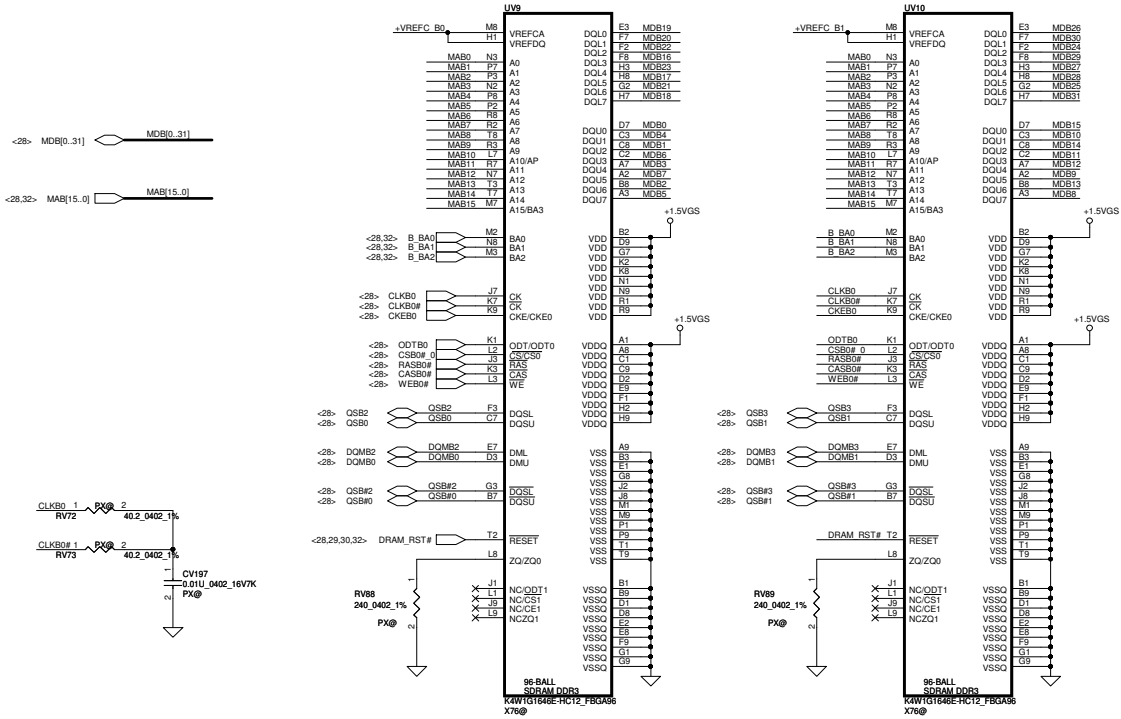
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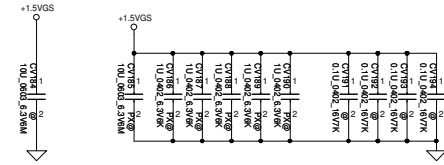
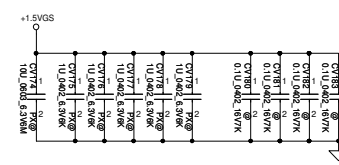
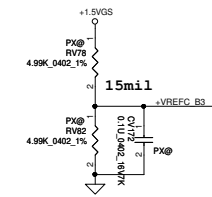
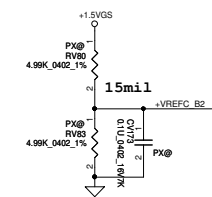
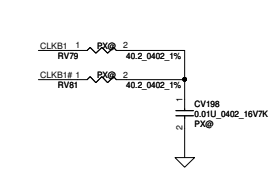
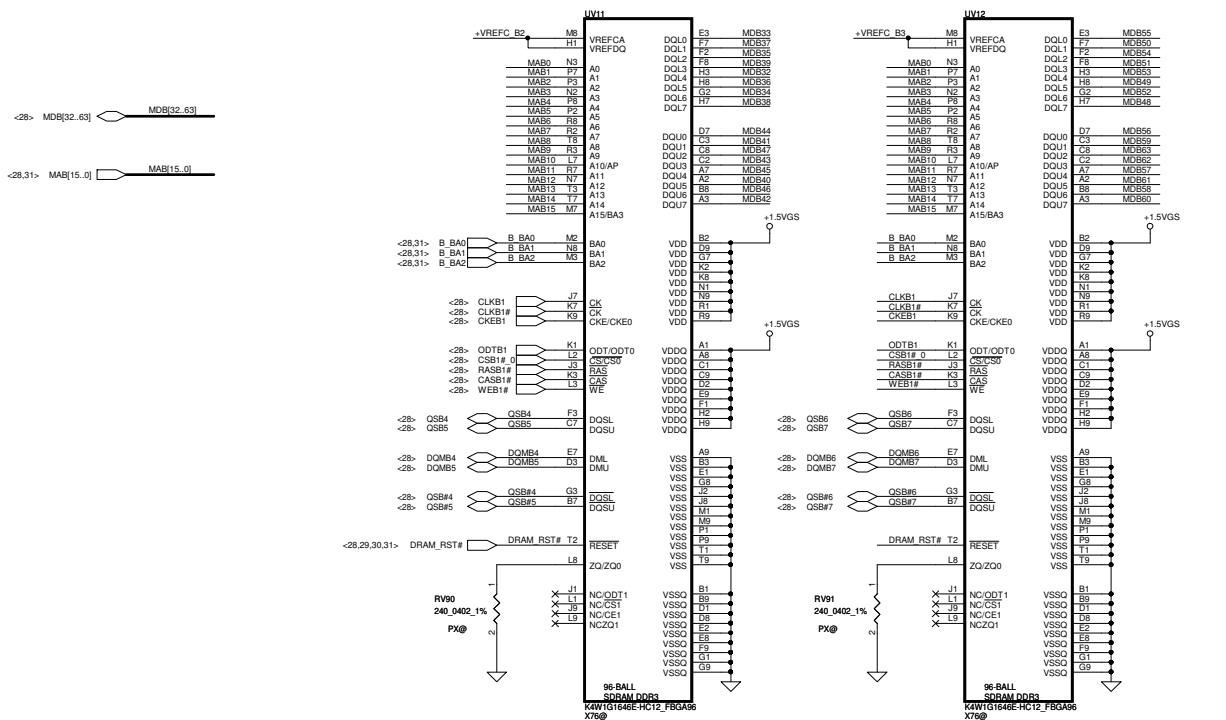
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<28> OSA7



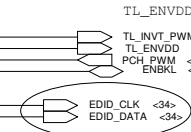
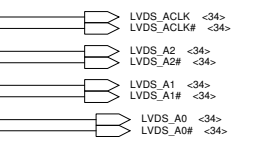
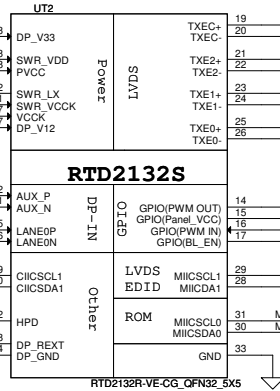
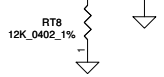
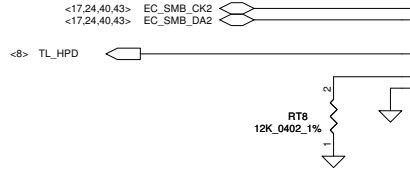
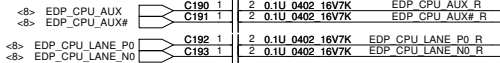
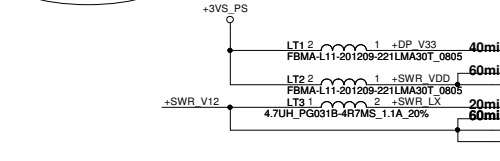
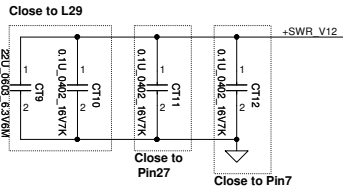
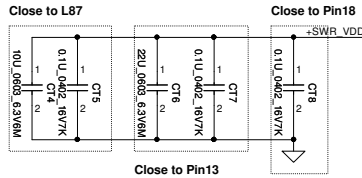
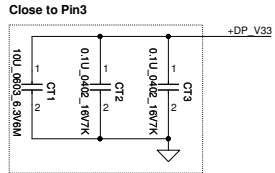
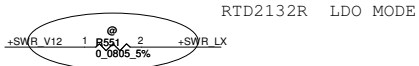
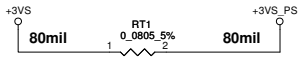
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Size	C	Document Number	QIQY2.LA6884P	Rev
Date	Thursday, October 11, 2012	Sheet	30	of 60





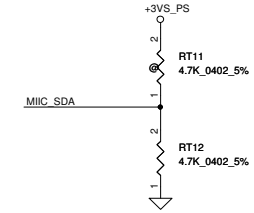
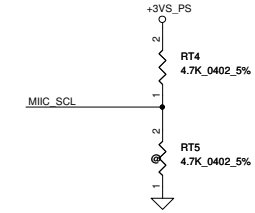
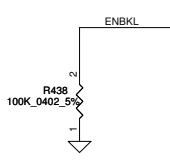
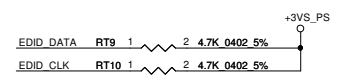
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Size	C	Document Number	QIQY2 LA6884P	Rev
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TL\_ENVDD need 60 mil if use for LVDS power on R version

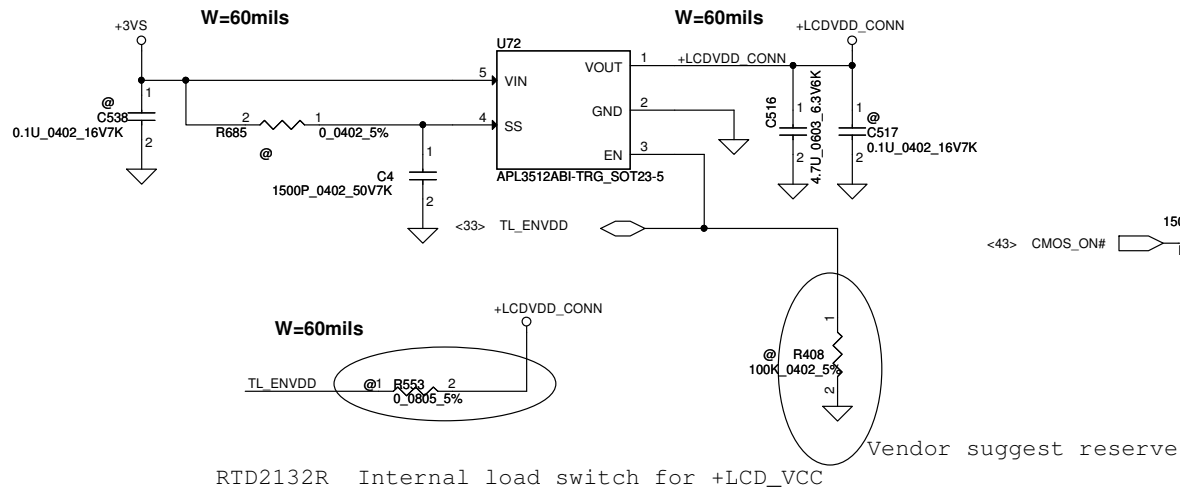
ADD TP on trace or via



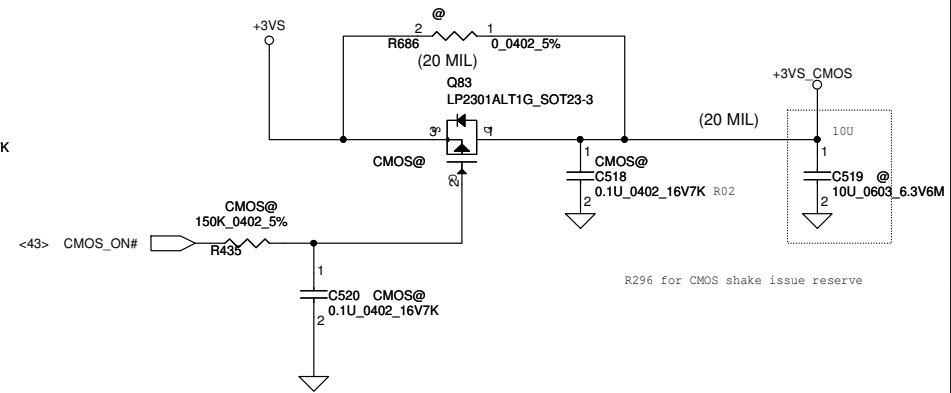
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MIIC_SCL	0	X	EC CODE
1	Internal ROM		EEPROM

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				LA-9641P
				Rev 1.0
				Date: Thursday, October 11, 2012 Sheet 33 of 60

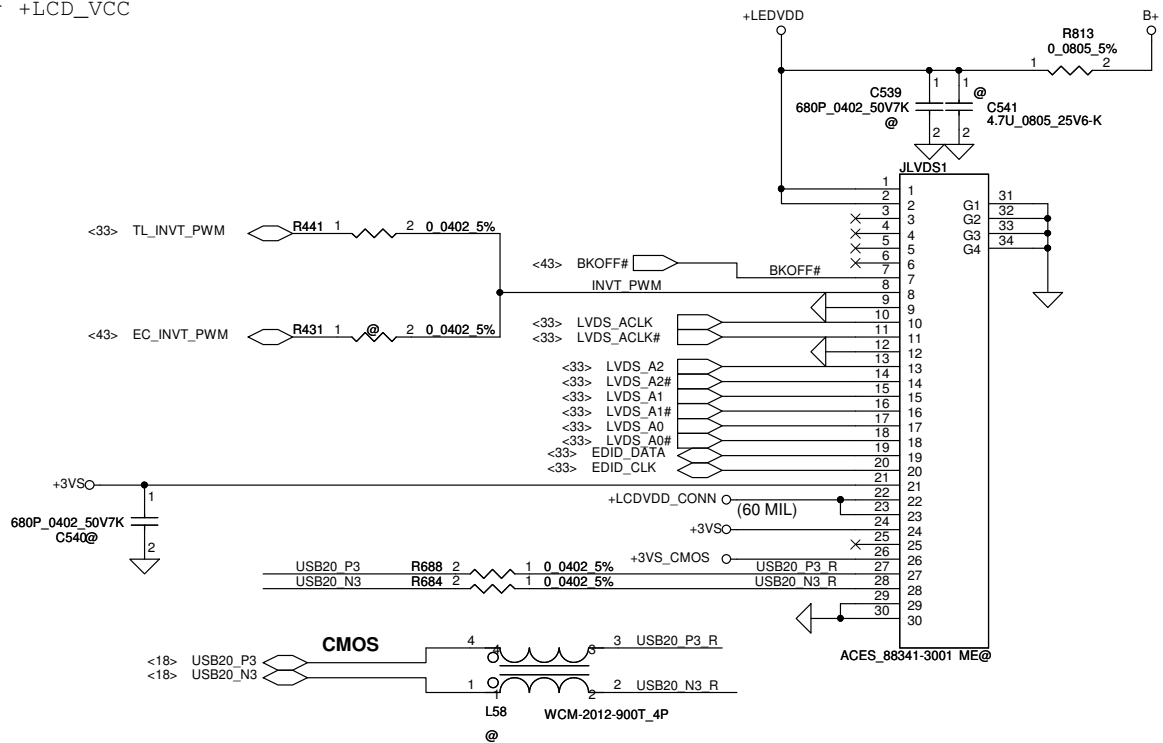
# LCD POWER CIRCUIT



# CMOS Camera

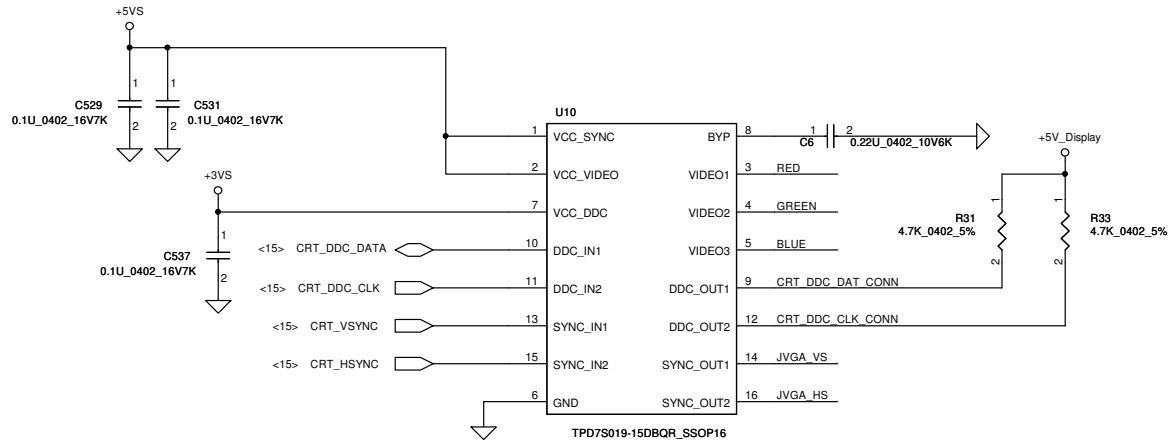
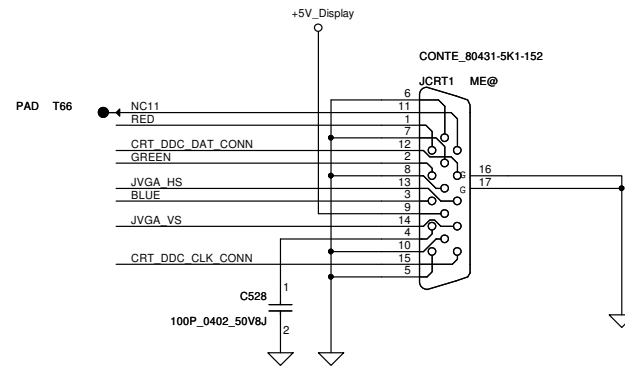
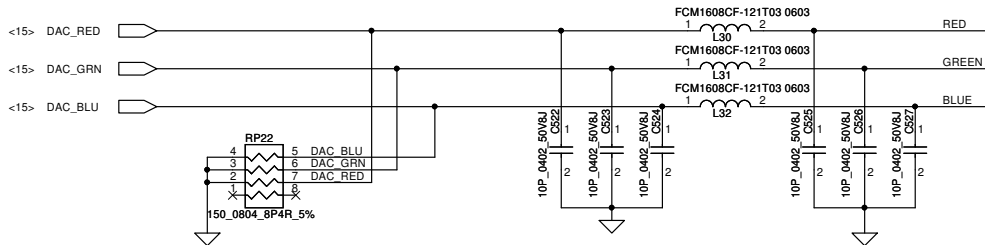


# VGA LCD/PANEL BD. Conn.

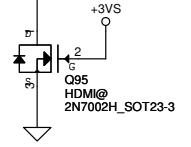
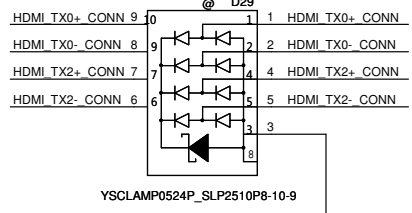
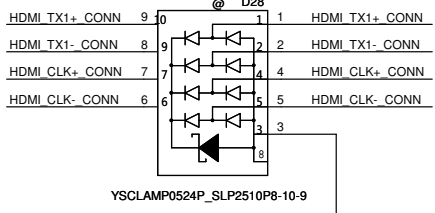
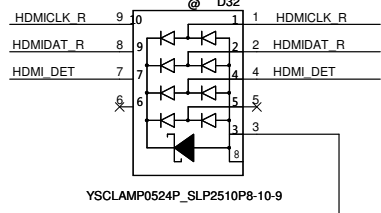
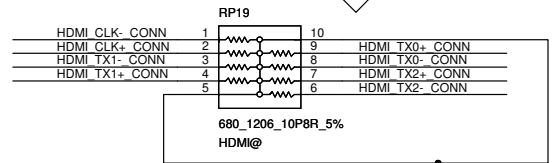
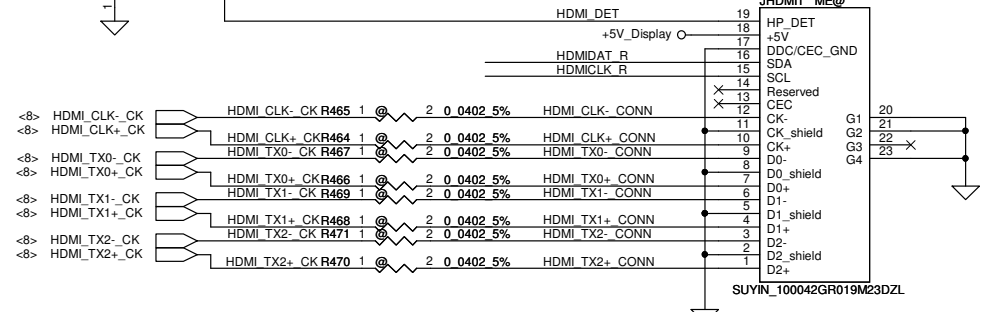
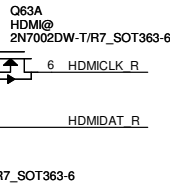
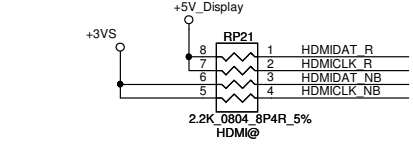
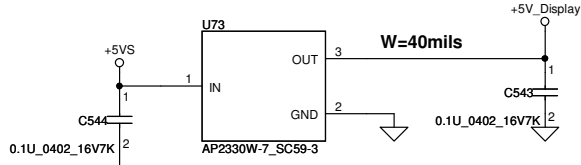
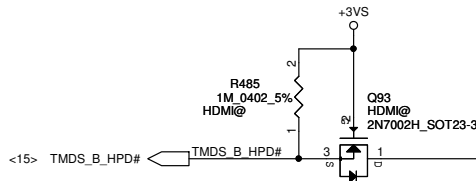
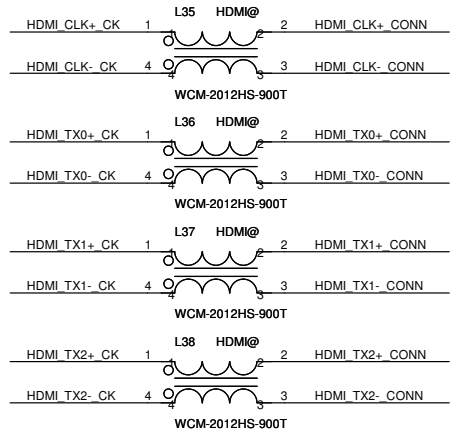


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				Document Number <b>LA-9641P</b>
				Rev 2.0
Date: Thursday, October 11, 2012				Sheet 34 of 60

# CRT Connector

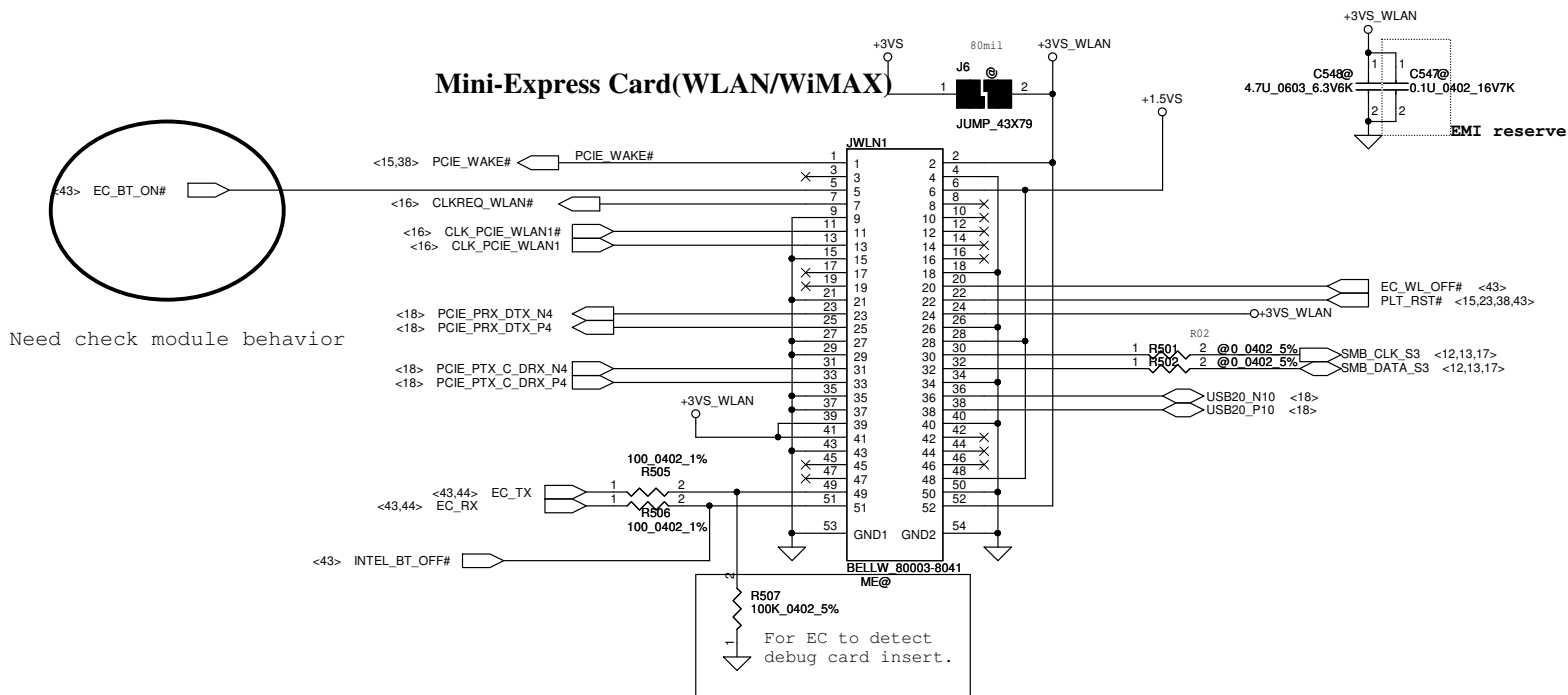


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Size	Custom	Document Number	<b>LA-9641P</b>		Rev
Date:	Thursday, October 11, 2012	Sheet	35	of	60

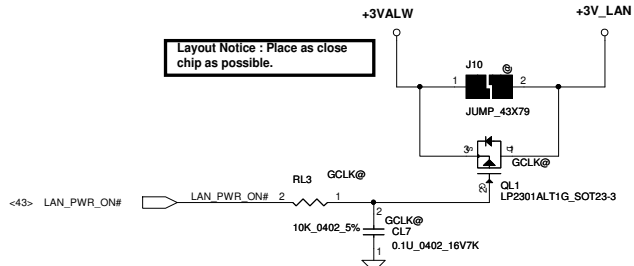


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Issued Date	2011/06/15	Deciphered Date	2012/07/11				Title	<b>HDMI CONN</b>
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						3	<b>LA-9641P</b>	2.0
						Date: Thursday, October 11, 2012	Sheet	36 of 60

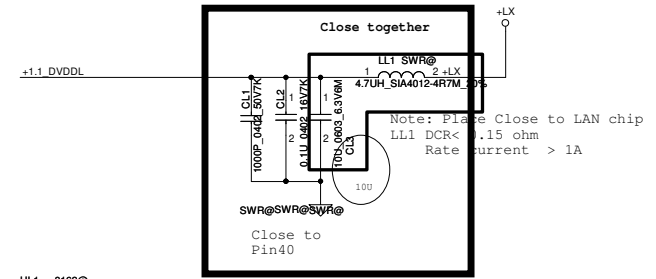
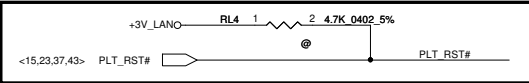
# Mini-Express Card for WLAN/WiMAX(Half)



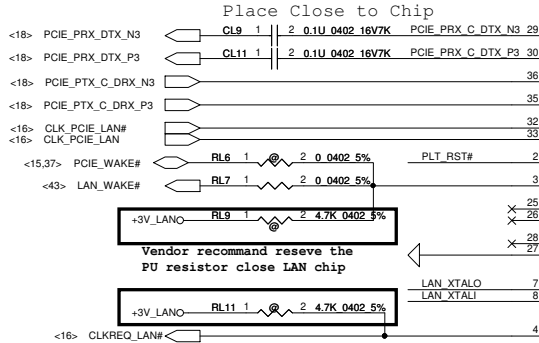
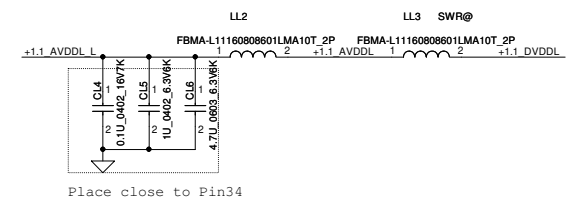
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>Mini-Card/NEW Card/SIM</b> <b>LA-9641P</b>								
Issued Date	2011/06/15	Deciphered Date	2012/07/11				Title	Size	Document Number	Rev		
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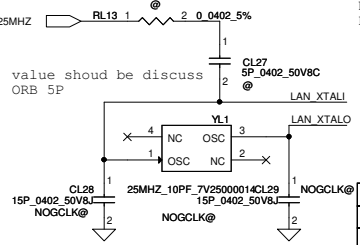
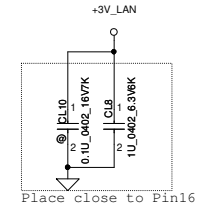
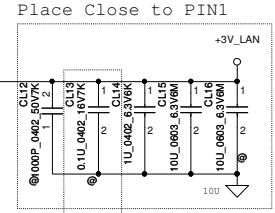
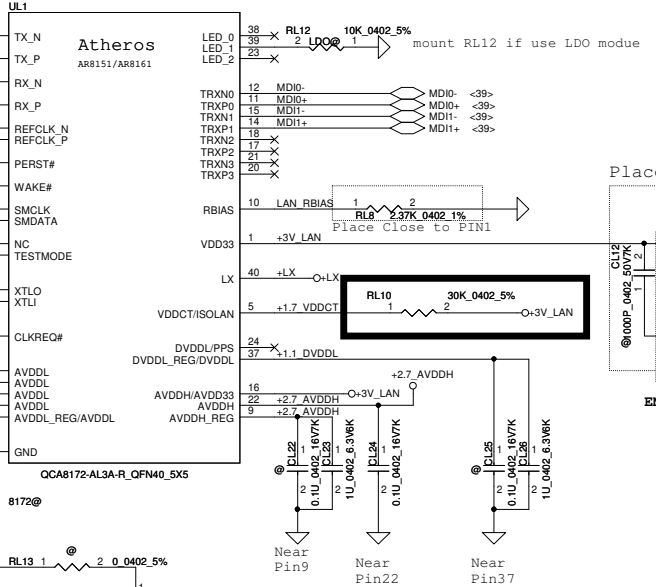
Vendor recommend reseve the PU resistor close LAN chip



SA000065400 S IC QCA8172-AL3A-R QFN 40P E-LAN CTRL  
 SA000052J10 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL



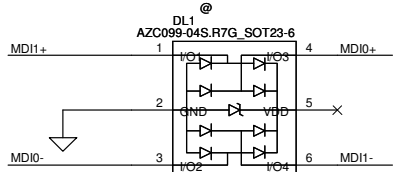
Vendor recommend reseve the PU resistor close LAN chip



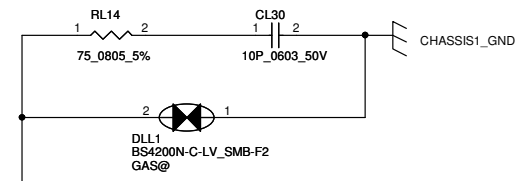
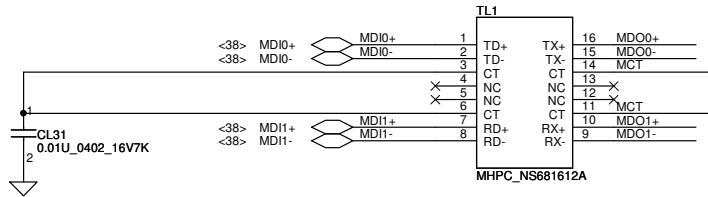
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Size	Document Number	Rev	LA-7982P	
Custom		1.0	Date: Thursday, October 11, 2012 Sheet 38 of 60	

**DL1**  
**1'S PN:SC300001G00**  
**2'S PN:SC300002E00**

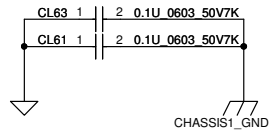
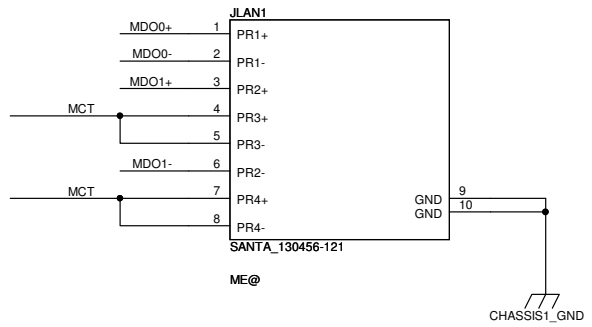
Place Close to TL1



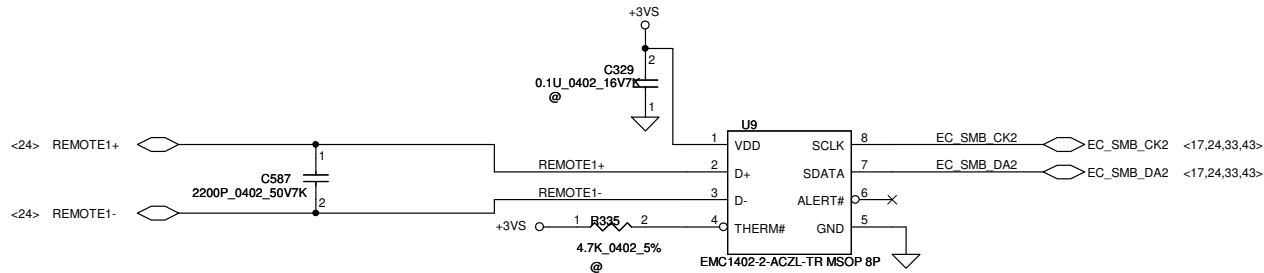
Reserve gas tube for EMI go rural solution



Need check Symbol

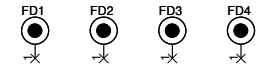
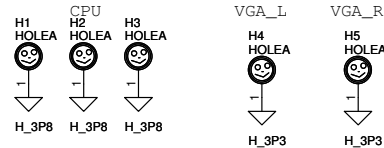


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				LA-7982P	1.0
Date: Thursday, October 11, 2012				Sheet	39 of 60

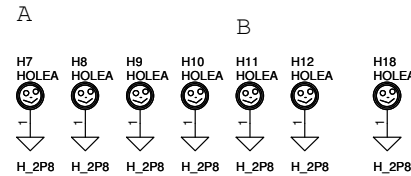
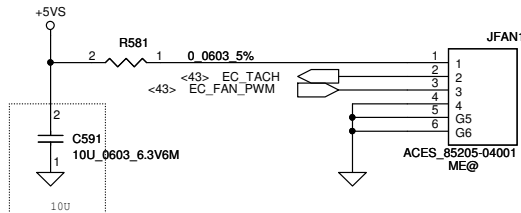


EMC1412-A (SA00003YA00)  
 Address 1111\_100xb  
 SIC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1, 2+/-:  
 Trace width/space: 10/10 mil  
 Trace length: <8"

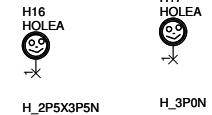


### FAN1 Conn



2P8 \* 7 pcd

M/B 橢圓孔 M/B 圓孔

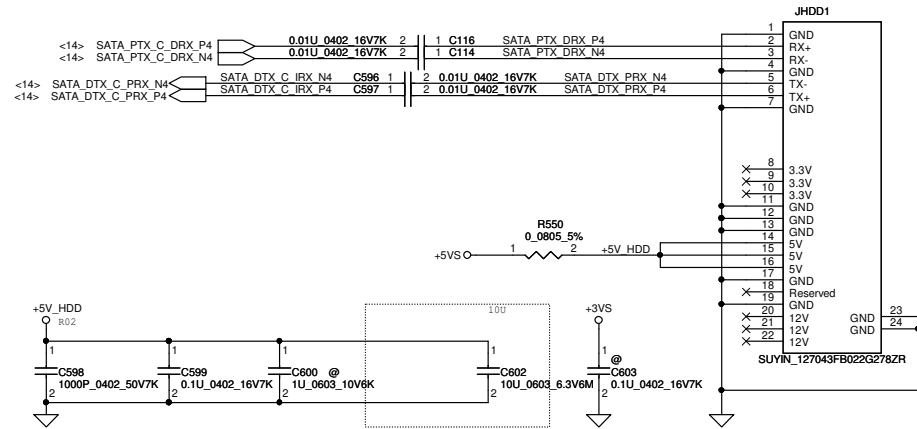


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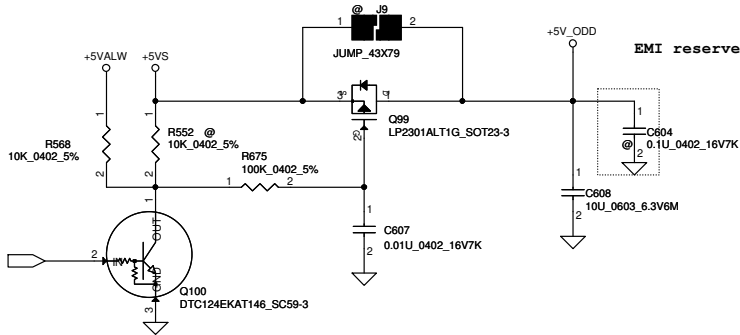
Security Classification	Compal Secret Data			<b>Compal Electronics, Ltd.</b>		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	<b>Fintek-Thermal IC/FAN/screw</b>	
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					<b>LA-9641P</b>	2.0
				Date: Thursday, October 11, 2012	Sheet	40 of 60



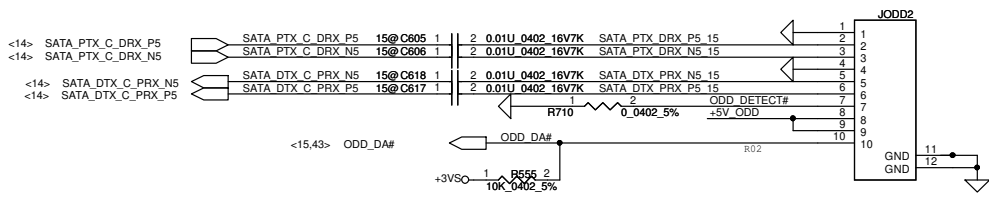
### SATA HDD Conn.



### ODD Power Control



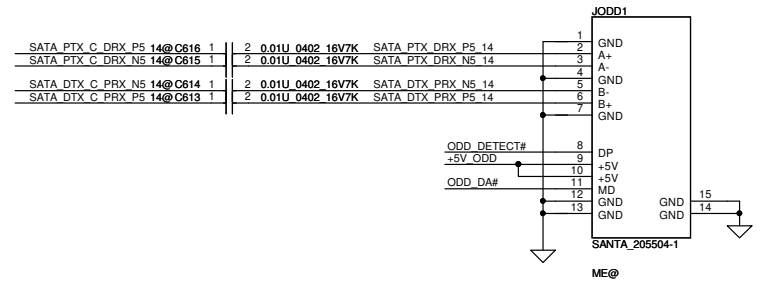
### FOR 15" SATA ODD FFC Conn.



HB\_A051020-SAHR21

Co-lay

### FOR 14" SATA ODD Conn.



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**Compal Electronics, Inc.**

**HDD/ODD/BT Connector**

Title: **LA-9641P**

Size: Custom Document Number: **LA-9641P** Rev: 2.0

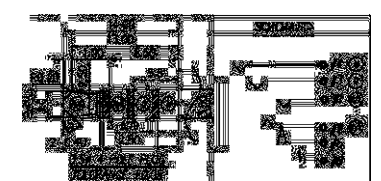
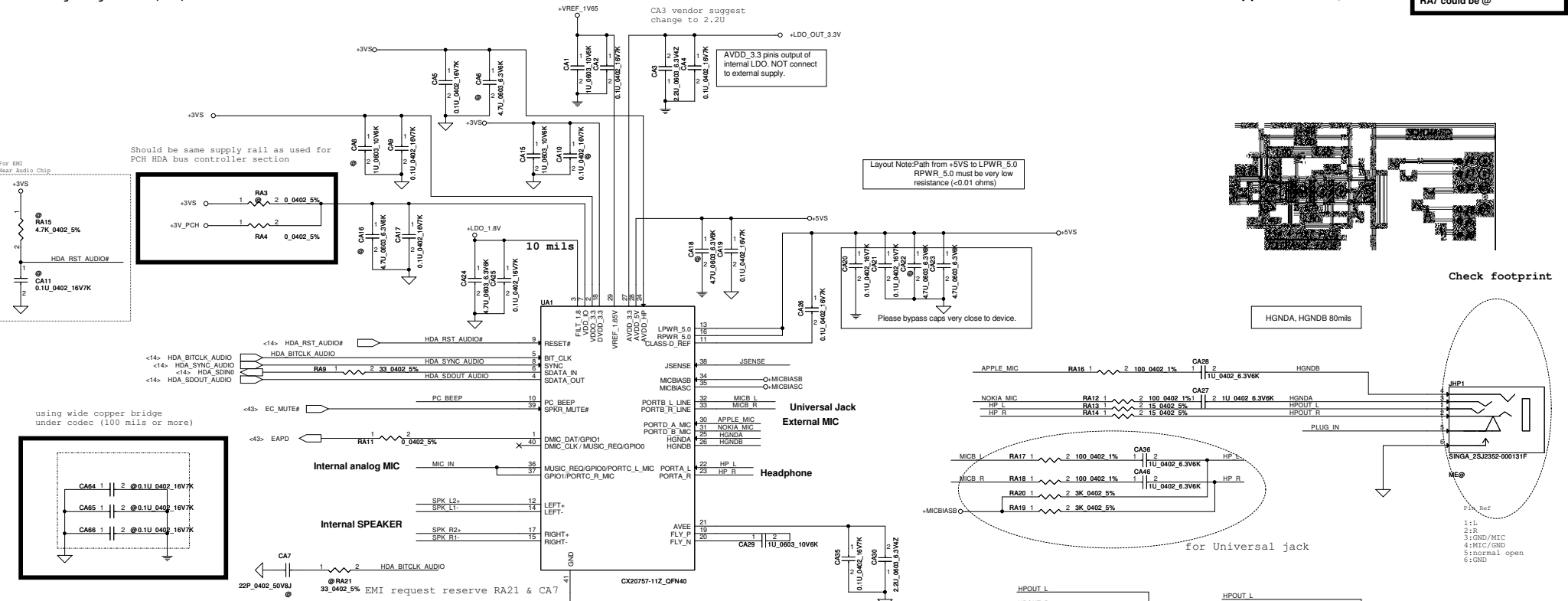
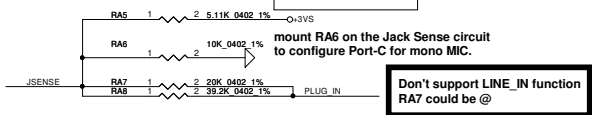
Date: Thursday, October 11, 2012 | Sheet 41 of 60

**CX20751**  
**High Definition Audio Codec SoC**  
**With Integrated Class-D Stereo**  
**Amplifier.**

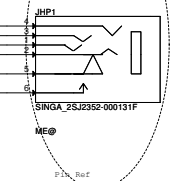
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).

An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).

Sense resistors must be connected same power that is used for VAUX\_3.3



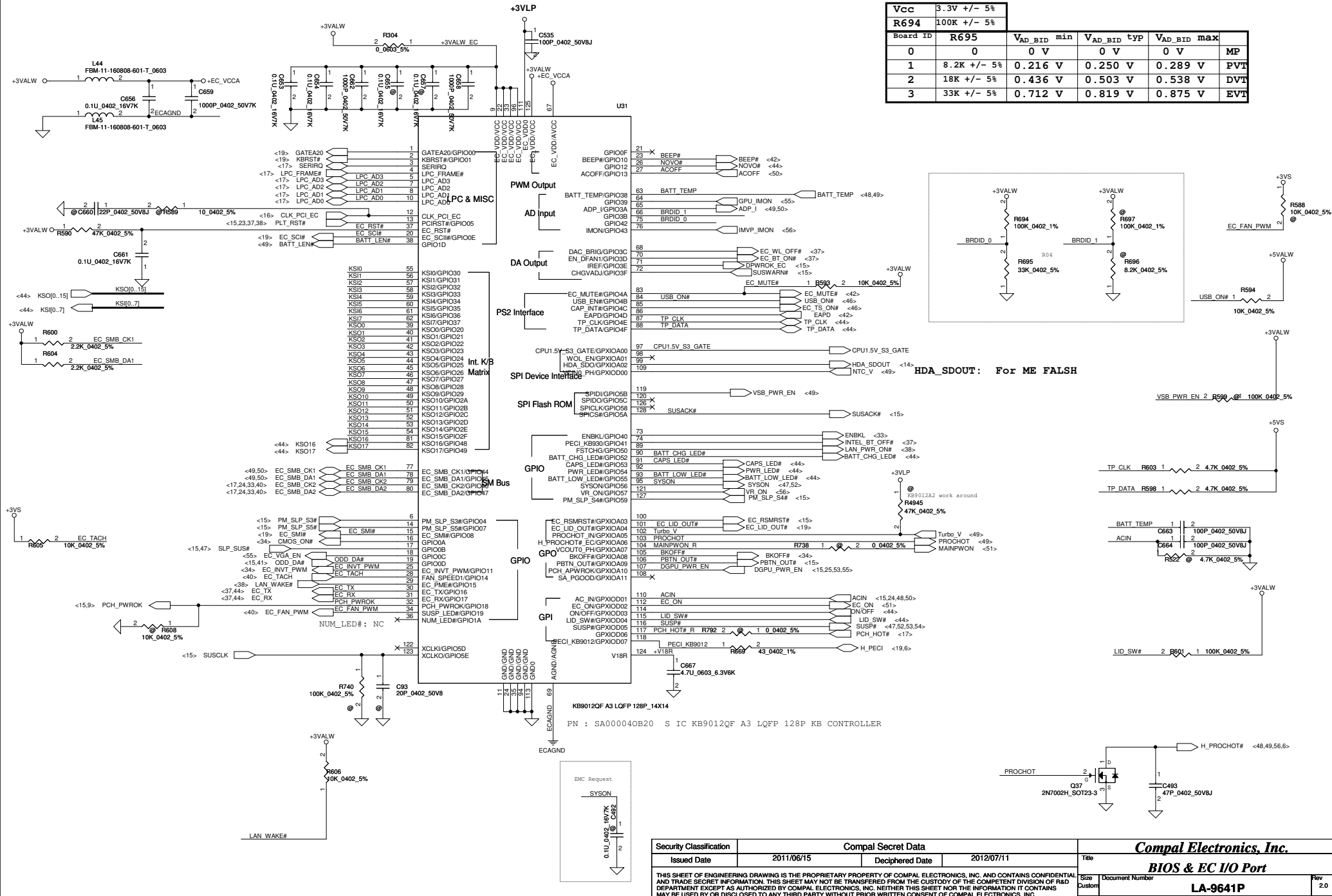
Check footprint



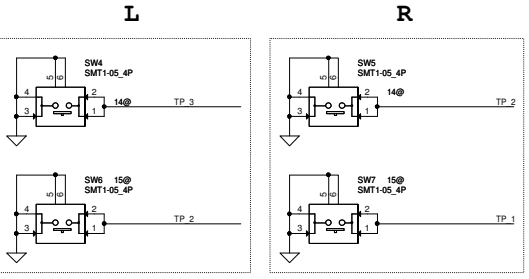
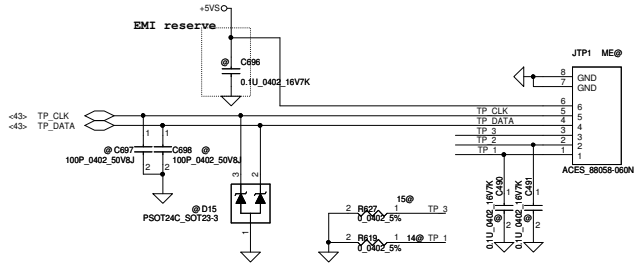
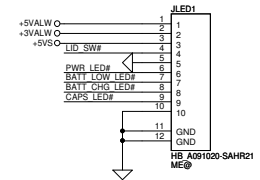
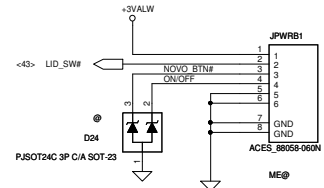
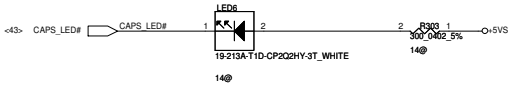
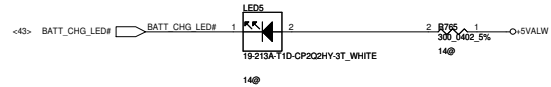
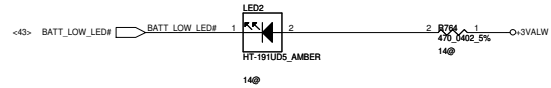
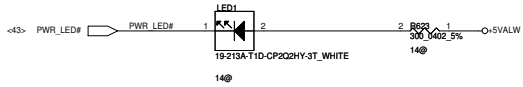
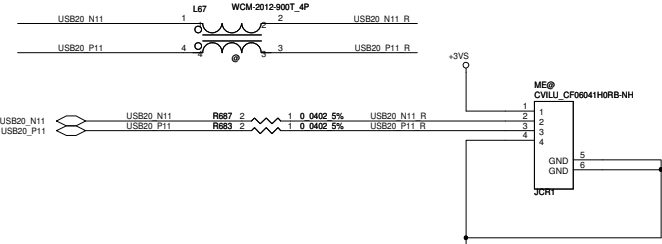
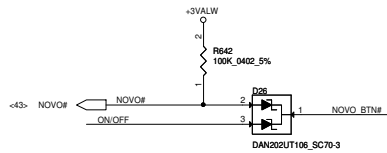
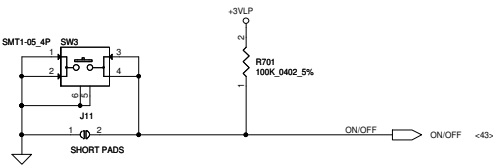
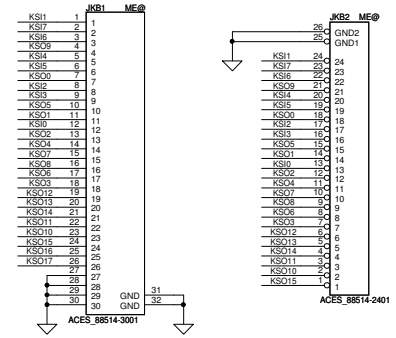
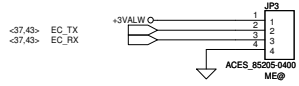
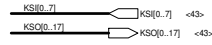
wide 20MIL

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Customer	LA-7982P	1.0		1.0	
Date:	Thursday, October 11, 2012	ISheet	42	of 60	

Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	MP
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT



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Compal Electronics, Inc.			BIOS & EC I/O Port	
Size	Document Number	Rev		
Custom	LA-9641P	2.0		
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15"

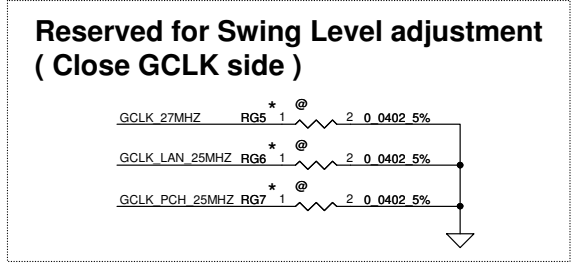
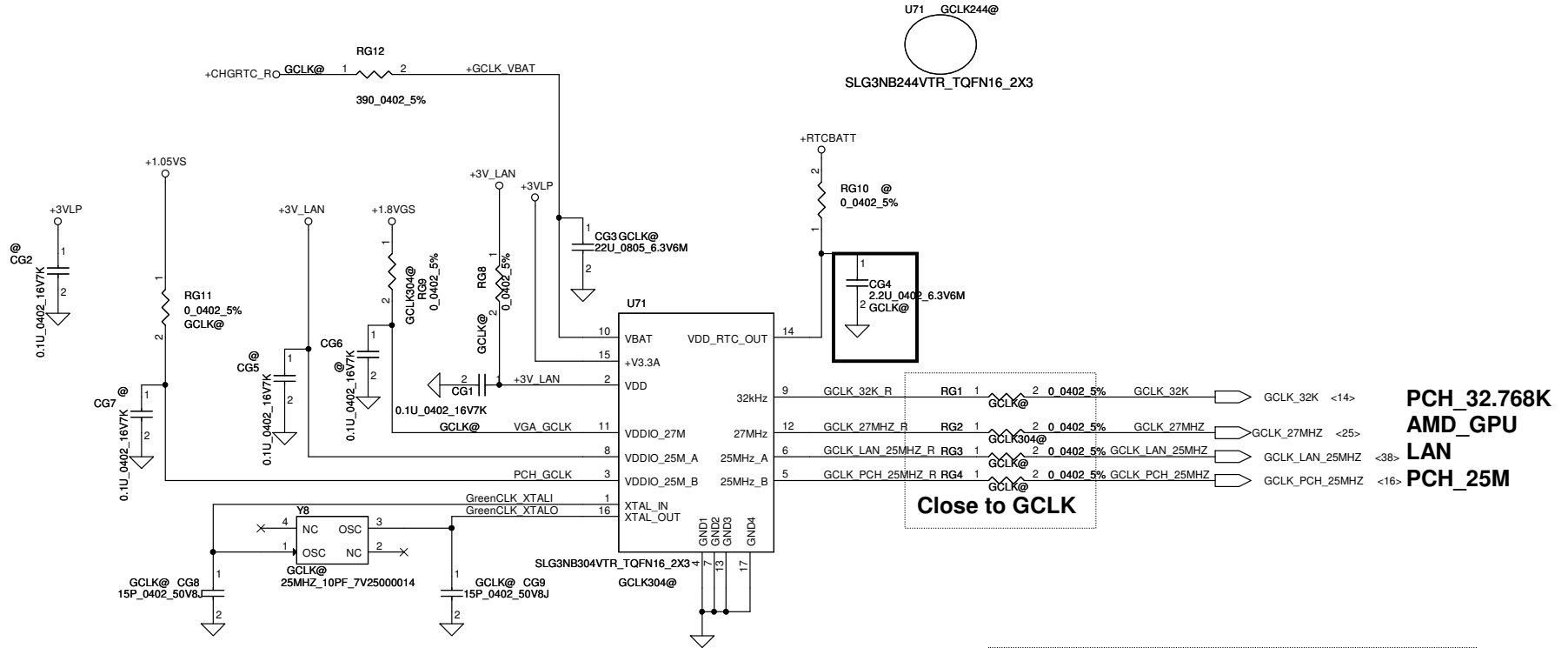
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"

1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

# Green Clock

Every power trace need:  
W=20mils



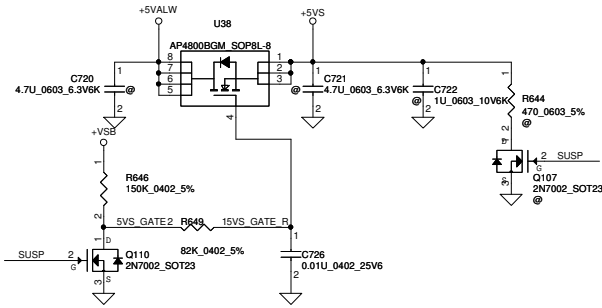
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				B	2.0
				Date:	Thursday, October 11, 2012
				Sheet	45 of 60

**PCH\_32.768K  
AMD\_GPU  
LAN  
PCH\_25M**

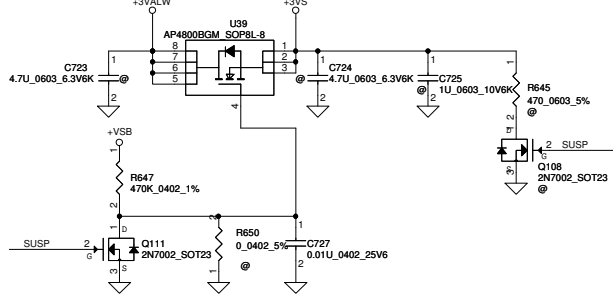
**LA-9641P**



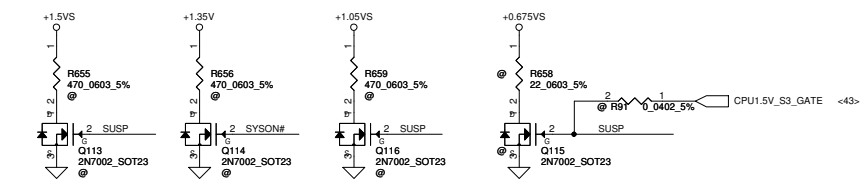
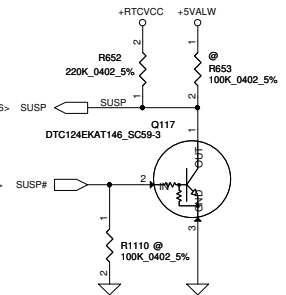
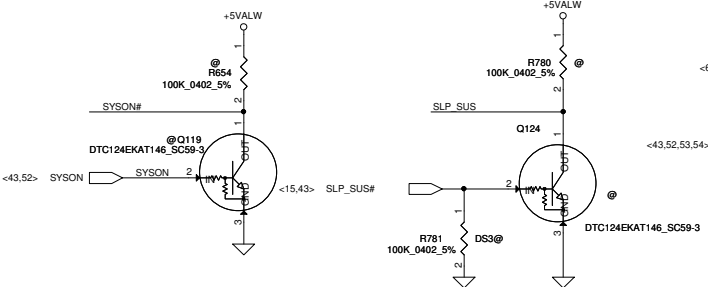
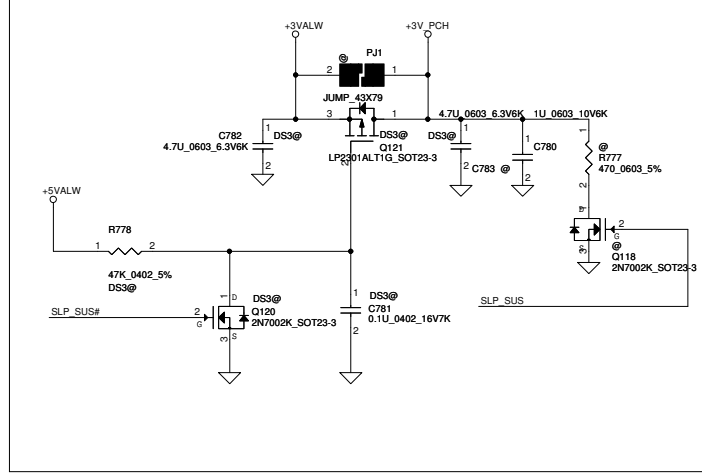
**+5VALW TO +5VS**



**+3VALW TO +3VS**

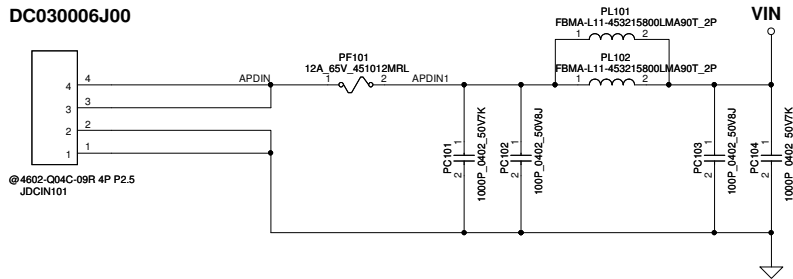


**+3VALW TO +3VALW(PCH AUX Power)**



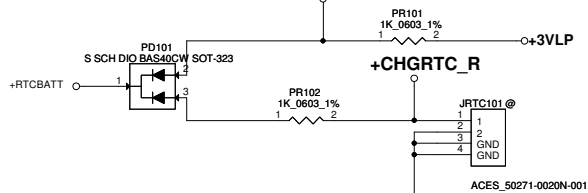
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				Document Number
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DC030006J00

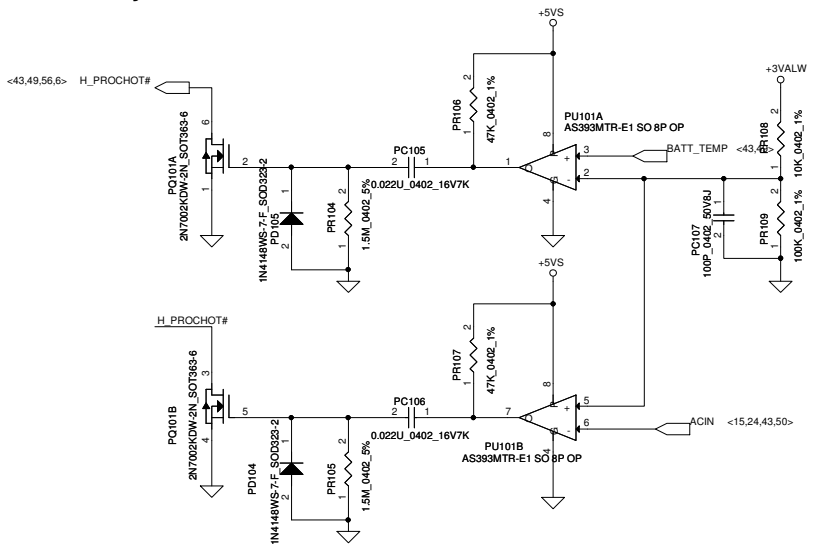


@ 4602-Q04G-09R 4P P2.5  
JDCIN101

+CHGRTC

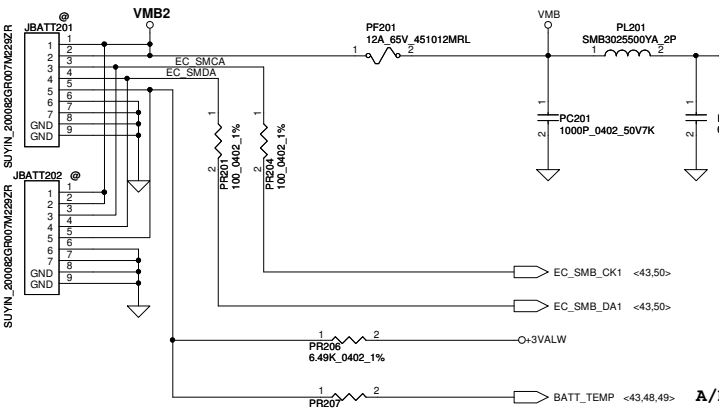


RTC Battery



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				PWR DCIN / RTC Battery
				Rev 0.1
				Date: Thursday, October 11, 2012 Sheet 48 of 59

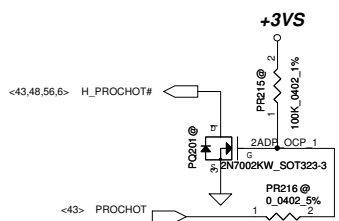




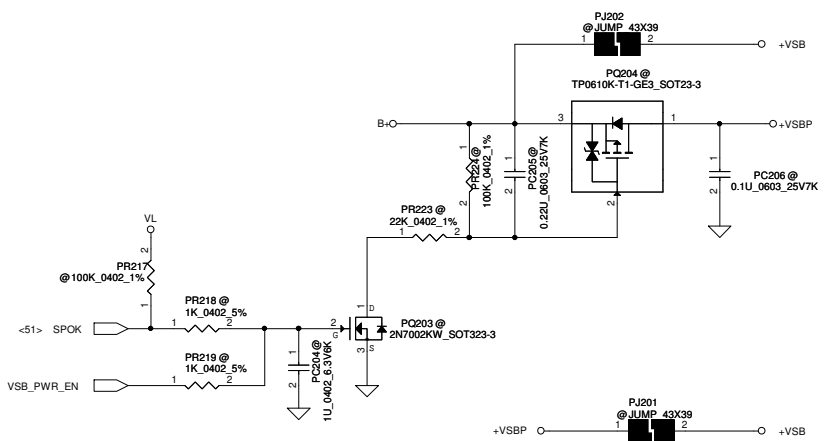
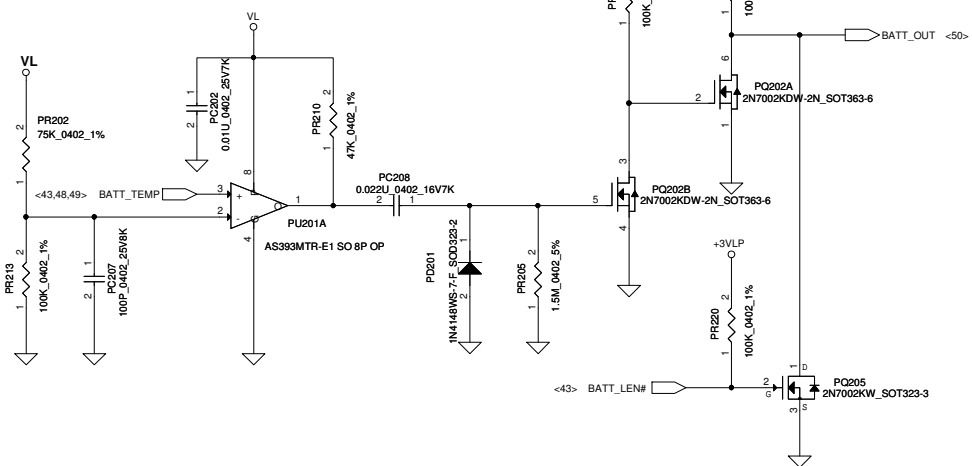
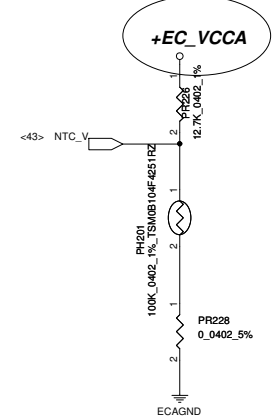
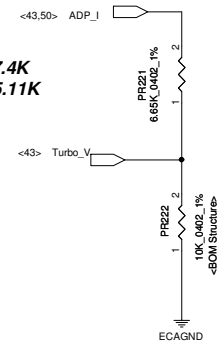
**PH201 under CPU bottom side :**  
**CPU thermal protection at 93 +-3 degree C**  
**Recovery at 56 +-3 degree C**

**90W(DIS) : 6.65K 100W active 90W recovery**  
**65W(UMA) : 1.65K 70W active 65W recovery**

20120314  
 Change to +EC\_VCCA from +3VLP

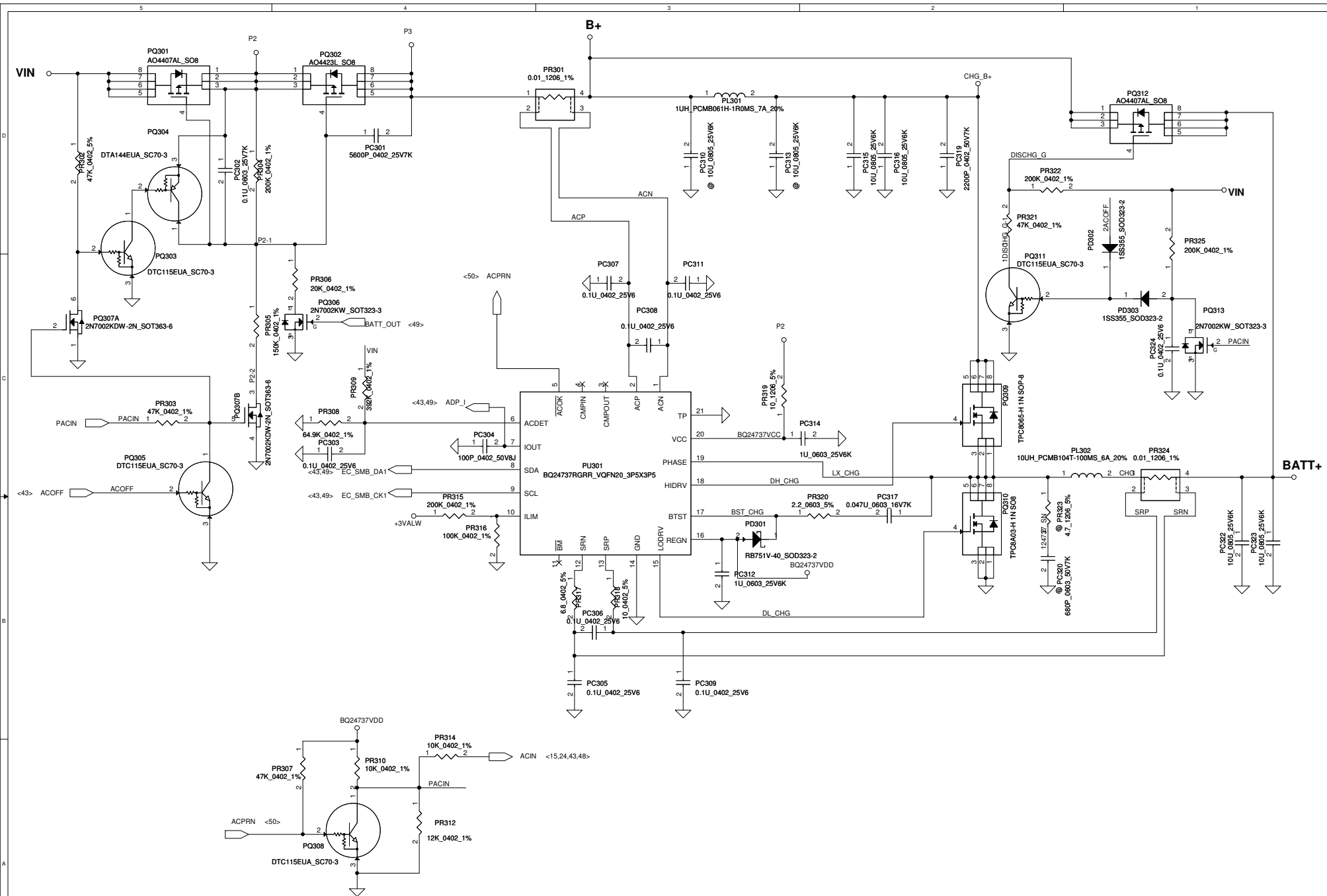


**90W(DIS) : 27.4K**  
**65W(UMA) : 5.11K**



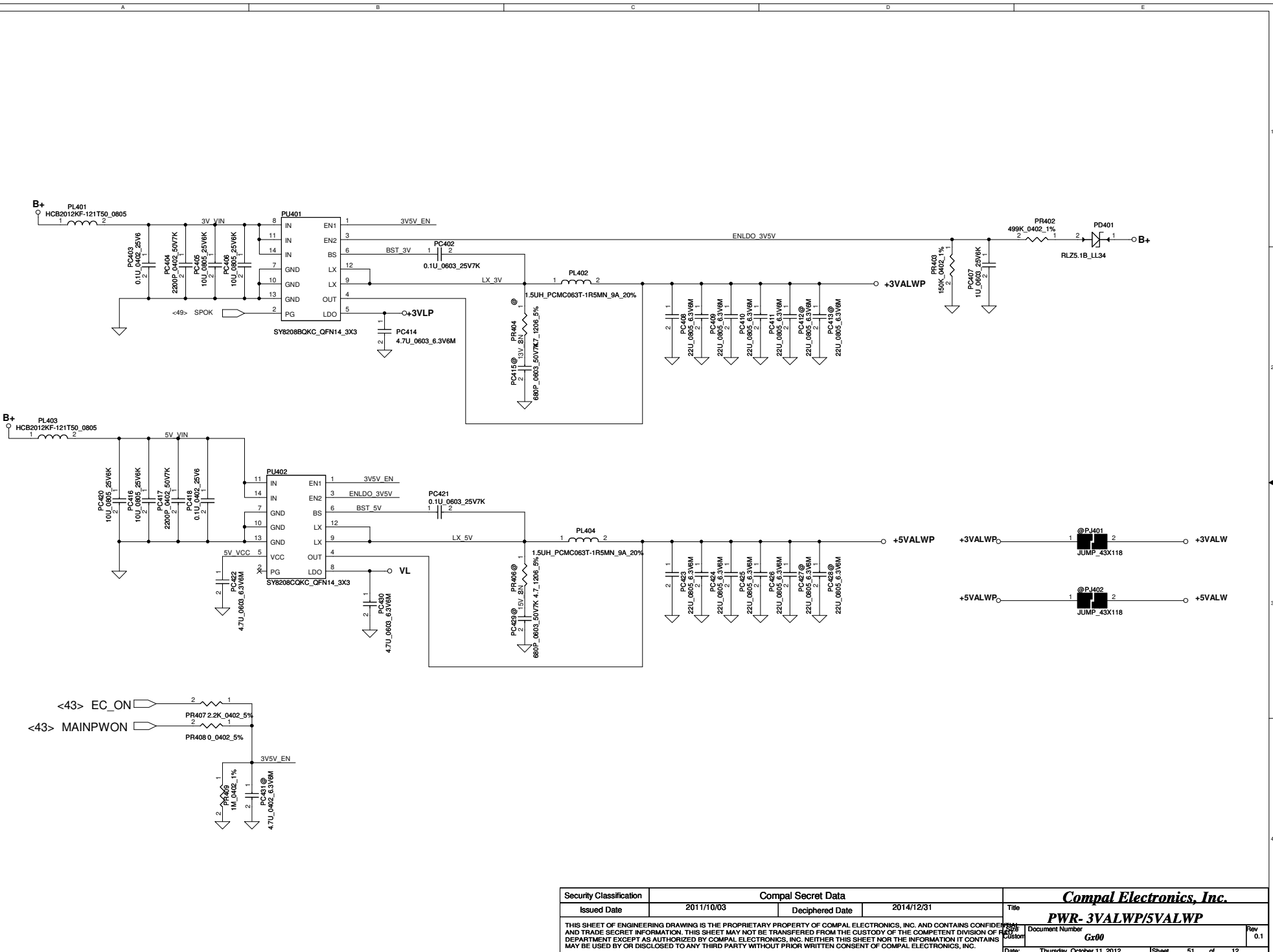
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<b>Compal Electronics, Inc.</b>	
<b>PWR-BATTERY CONN/OTP</b>	
Document Number	Rev
<b>Gx00</b>	0.1
Date: Thursday, October 11, 2012	Sheet 49 of 59



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	Gx00	0.1		
Date:	Thursday, October 11, 2012	Sheet	50	of 59

**Compal Electronics, Inc.**  
**CHARGER-BQ24737**

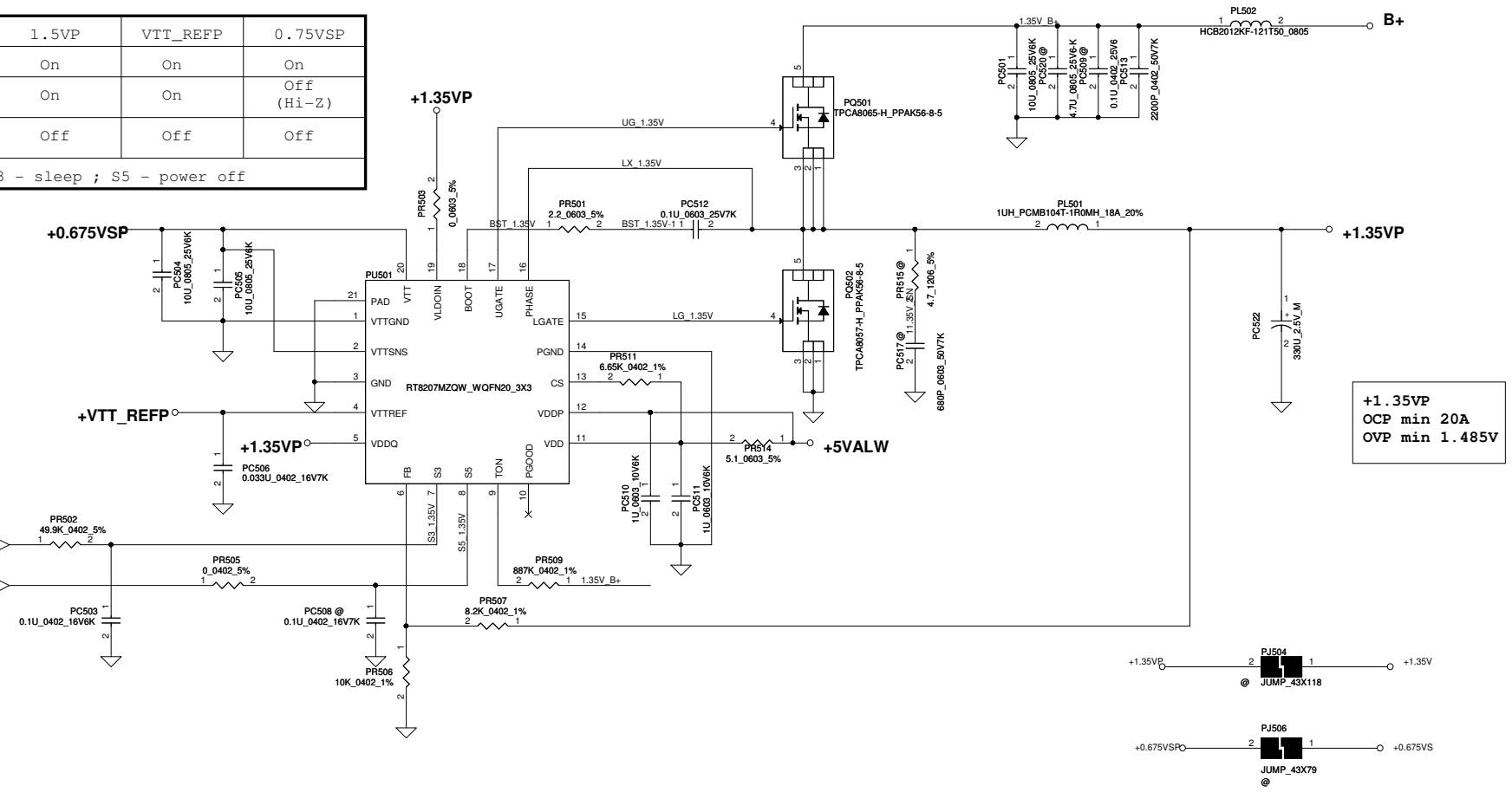


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				Gx00
				Rev 0.1
Date: Thursday, October 11, 2012				Sheet 51 of 12

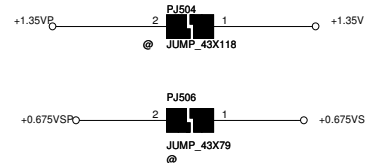
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

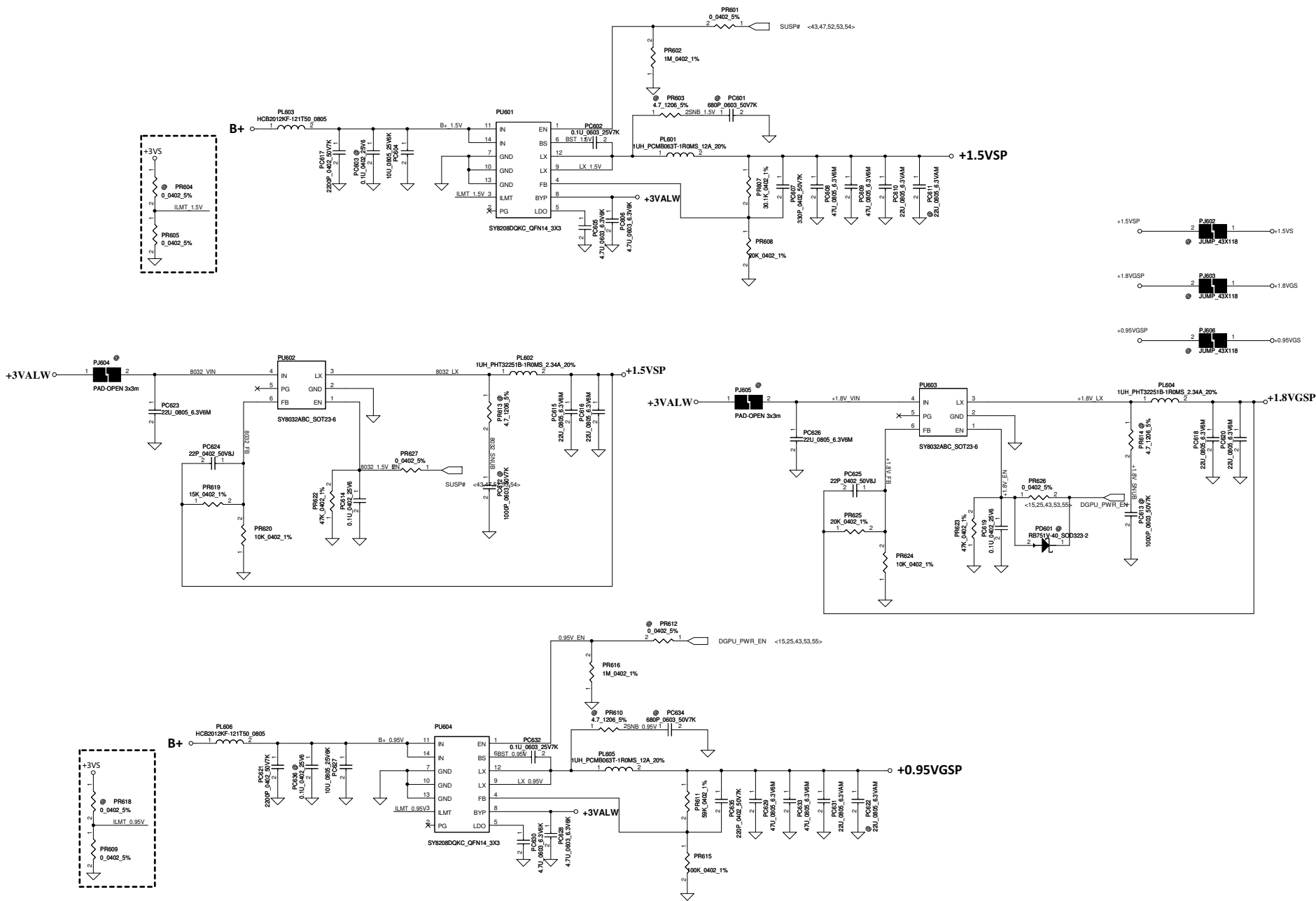
<43,47,53,54> SUSP#  
<43,47> SYSON



+1.35VP  
OCP min 20A  
OVP min 1.485V

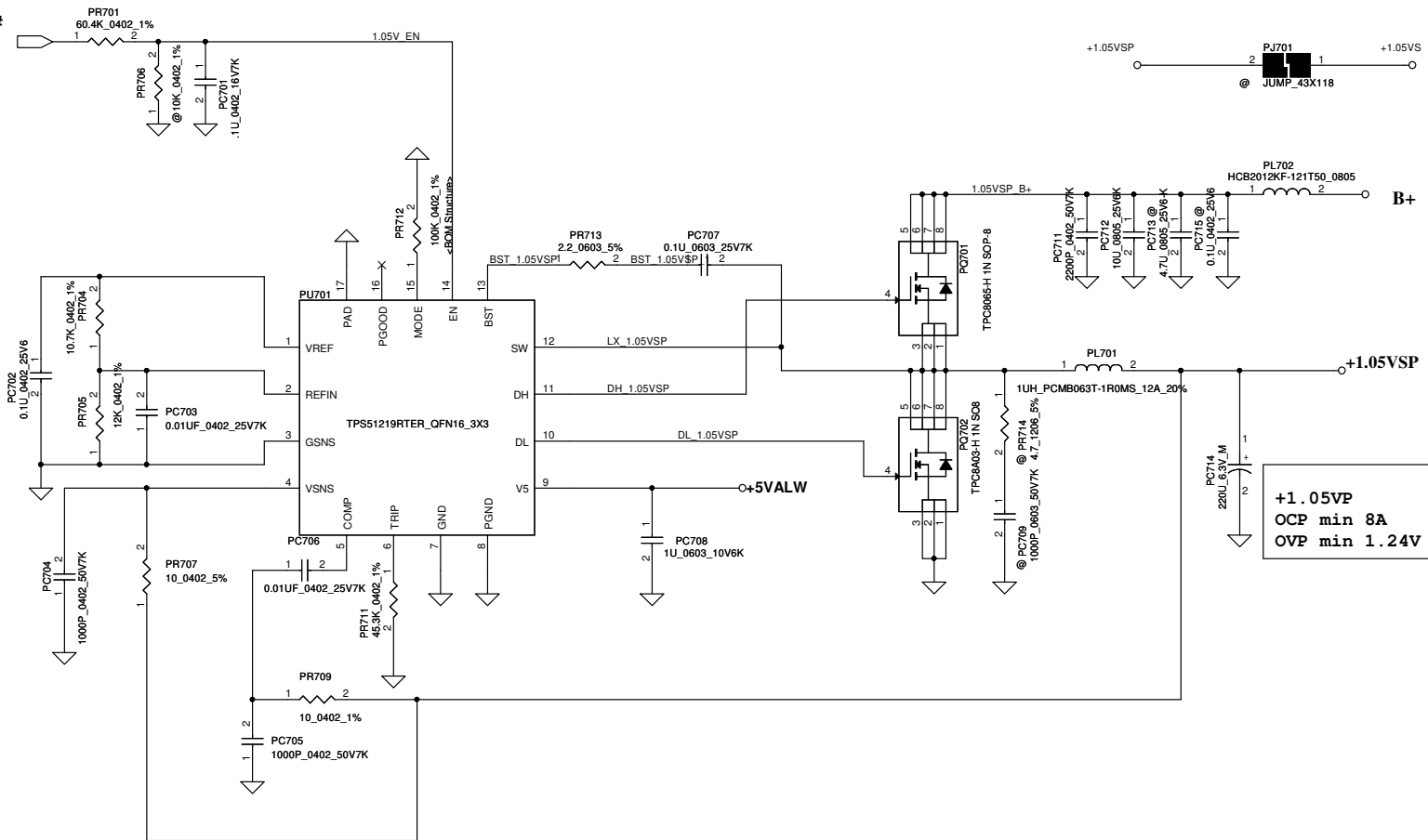


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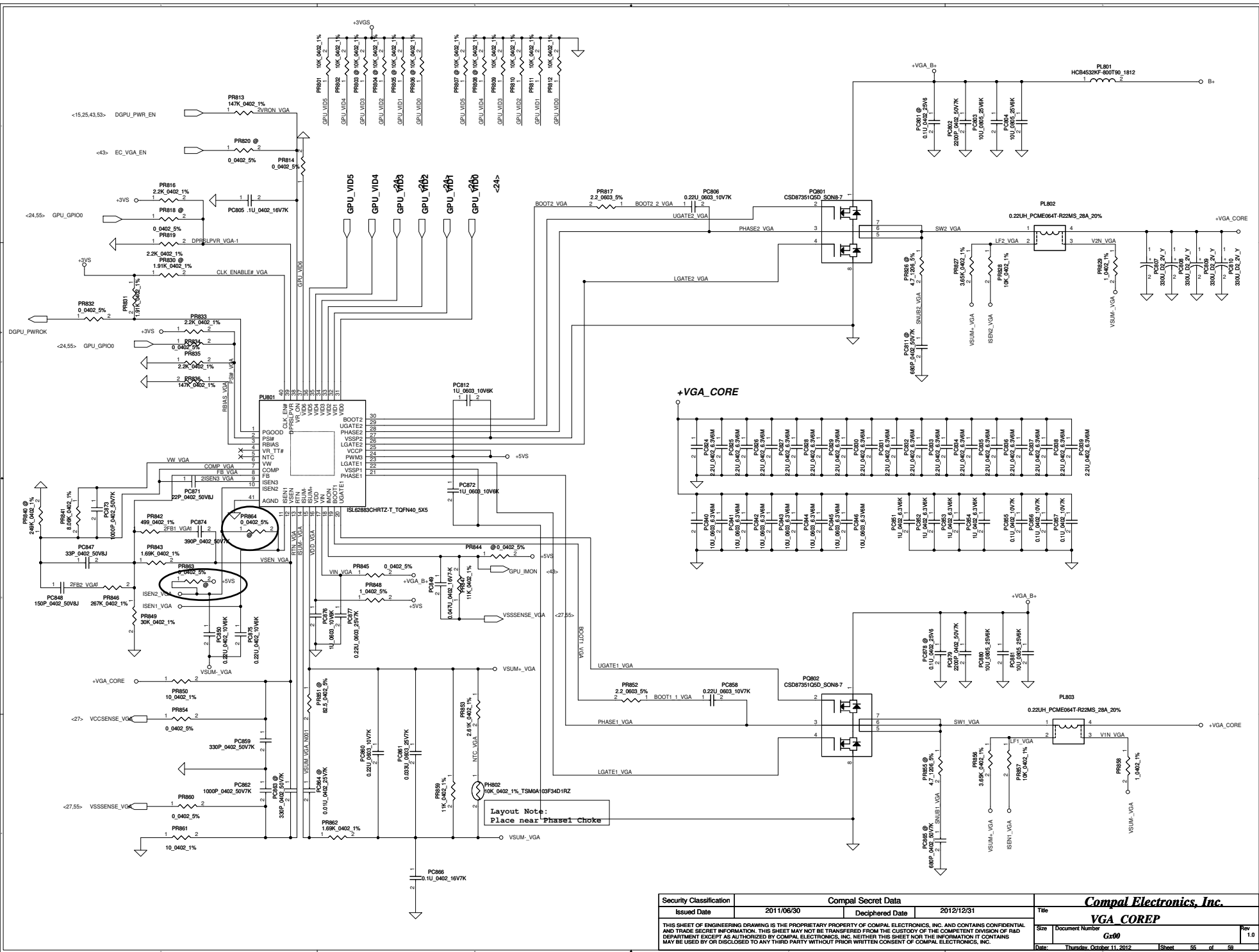


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				1.5V VRAM/1.8V/0.95V
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<43,47,52,53> SUSP#

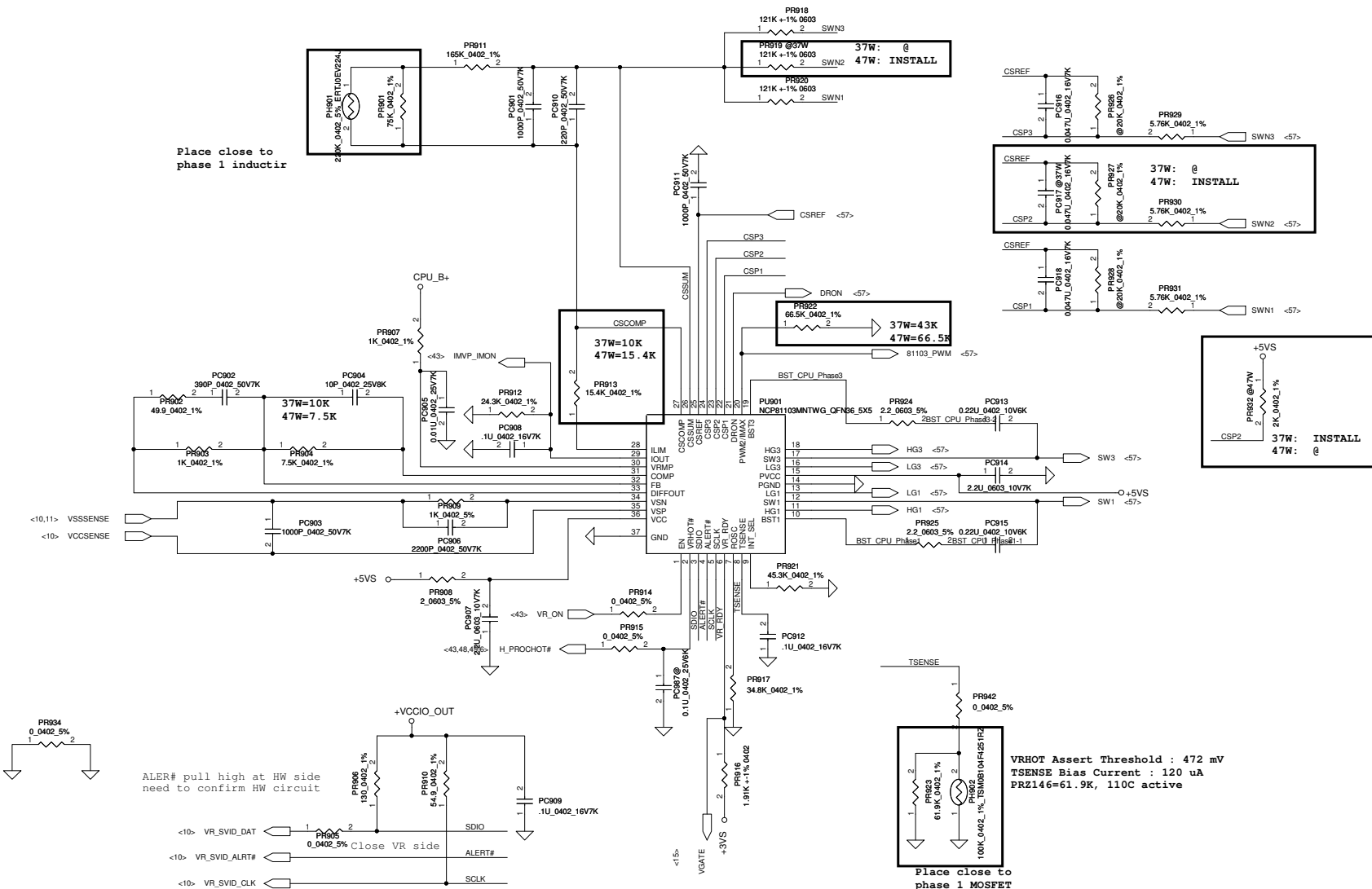


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Place close to phase 1 inductor



ALER# pull high at HW side need to confirm HW circuit

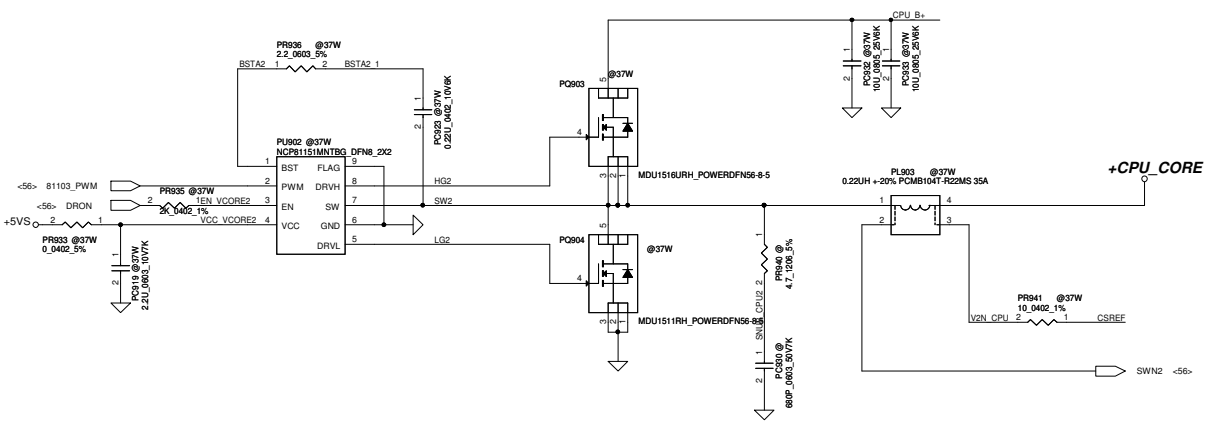
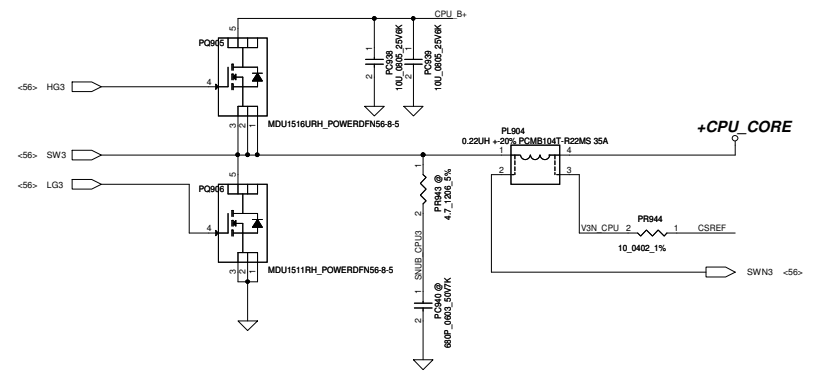
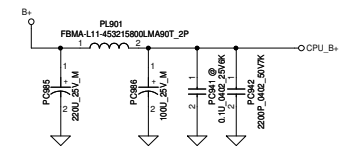
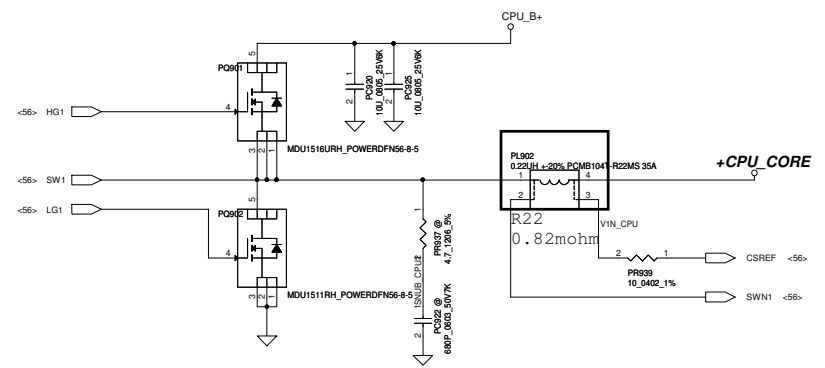
<10> VR\_SVID\_DAT  
 <10> VR\_SVID\_ALERT#  
 <10> VR\_SVID\_CLK

VRHOT Assert Threshold : 472 mV  
 TSENSE Bias Current : 120 uA  
 PR2146=61.9K, 110C active

Place close to phase 1 MOSFET

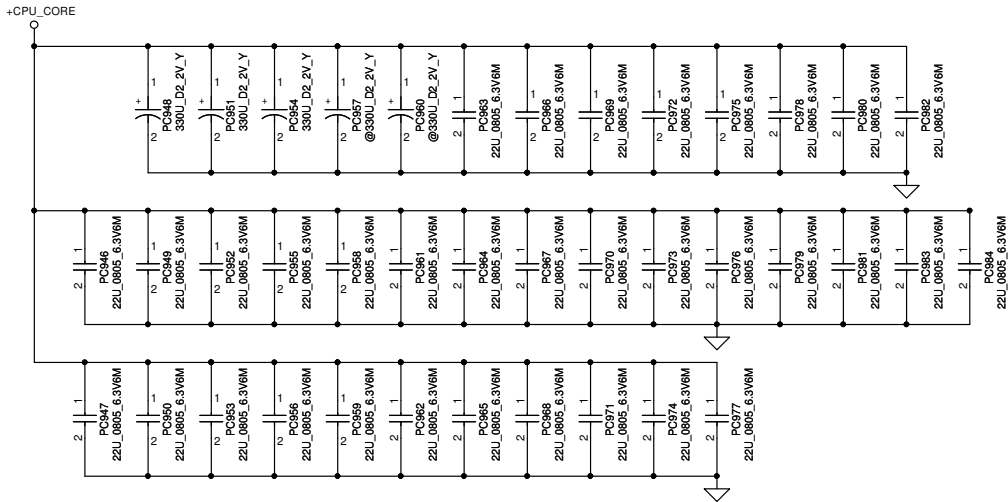
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Issued Date	2011/12/14	Deciphered Date	2012/12/31	Title	CPU CORE1
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**+CPU\_CORE** 3 X 330u/9m (47W) 2X330u/9m (37W)  
 34 X 22u/0805 34 X 22u/0805



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*Version change list (P.I.R. List)*

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for PWR*

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3					
4					
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10					
11					
12					
13					
14					
15					
16					

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