Compal Confidential

Q5WV8 Schematics Document

AMD "Comal" Platform

AMD Trinity APU / Hudson M3 FCH / ATI Thames XT

2012-01-05A

LA-8331P REV: 0.4

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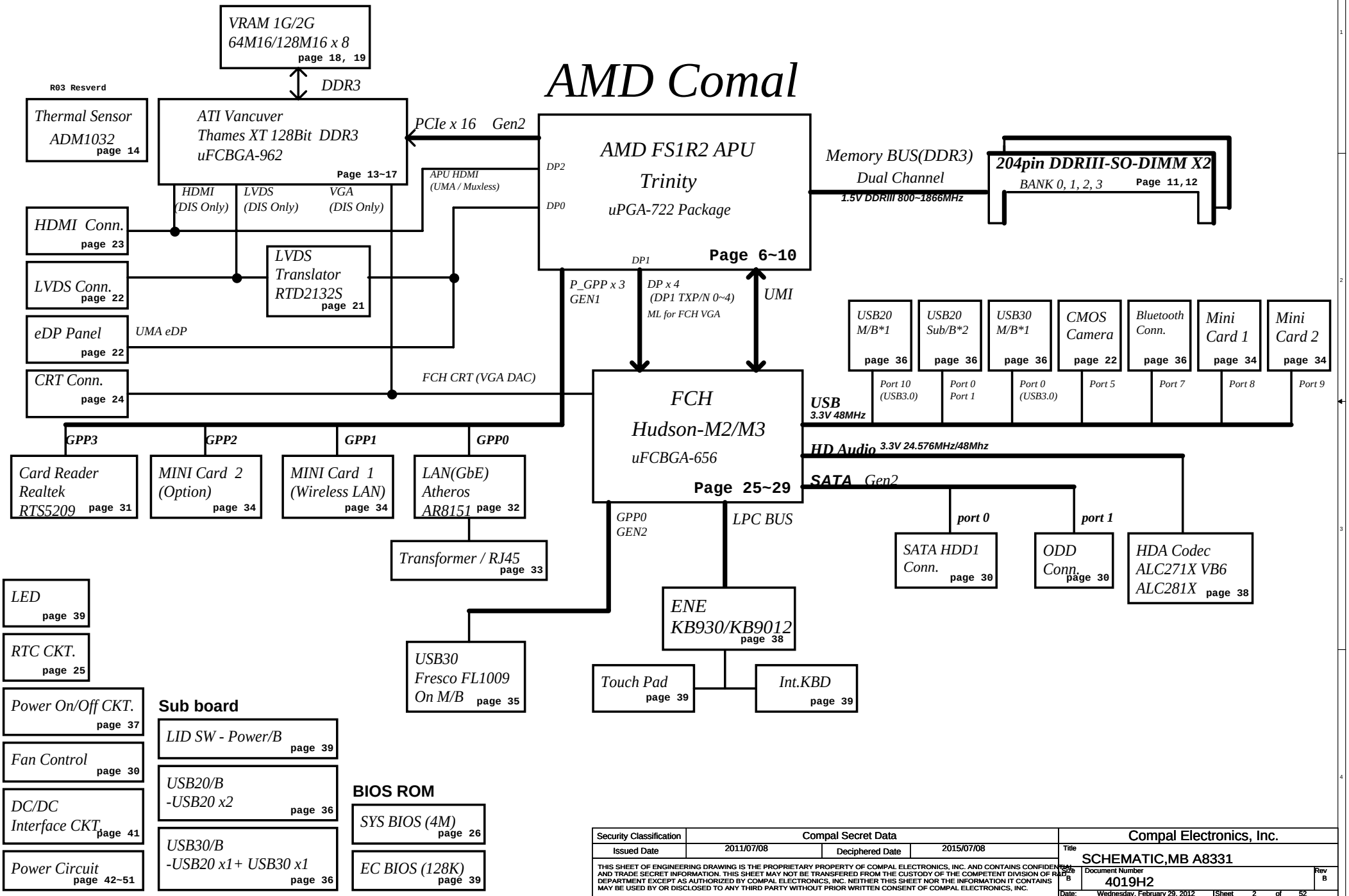
Model Name : Q5WV8



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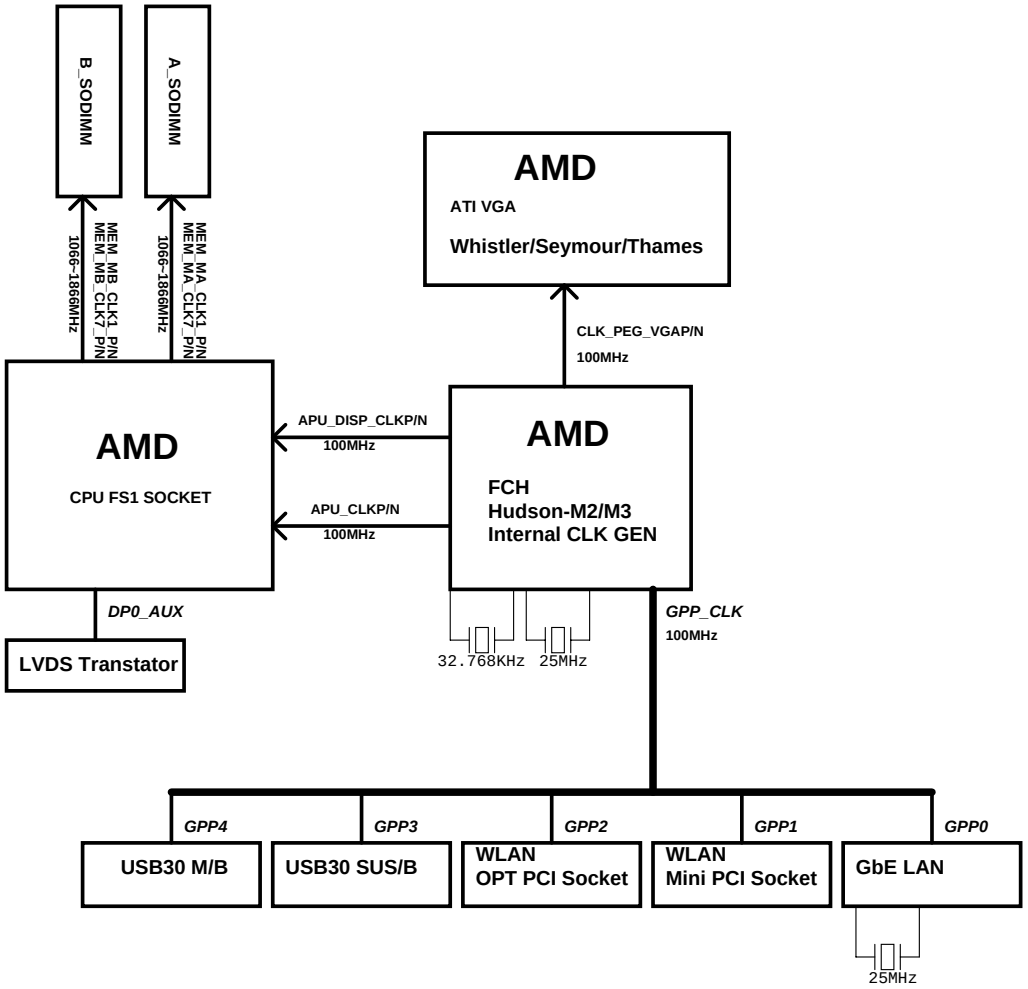
CLOCK DISTRIBUTION



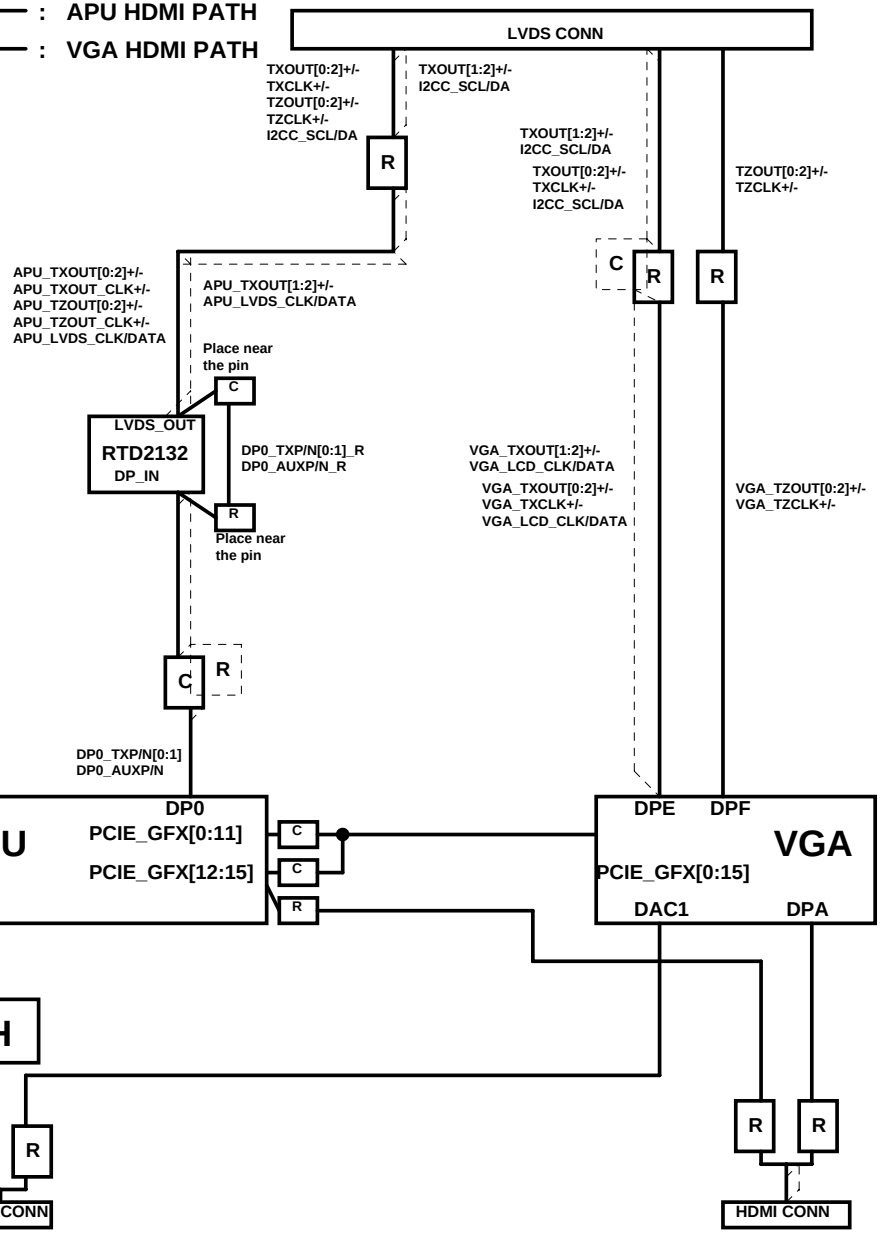
DISPLAY DISTRIBUTION

: LVDS PATH

: eDP PATH

: APU HDMI PATH

: VGA HDMI PATH



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ZZZ
PCB
Part Number = DA60000QV00
PCB 0OH LA-8331P REV0 M/B

ZZZ2
X76
Part Number = X76356BOL02
TMSSAM2G@

ZZZ3
X76
Part Number = X76356BOL03
SEYHYN1G@

ZZZ1
X76
Part Number = X76356BOL01
TMSHYN2G@

ZZZ4
X76
Part Number = X76356BOL04
SEYSAM1G@

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	EVT2
2	DVT
3	
4	
5	
6	
7	

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
LVDS TR(RTD-2132S)	1010 100X b	A8H
VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	90
DDR DIMM2	1101 001X b	94

FCH SM Bus 1 address

Device	Address	HEX

BOM Option Table

BOM Config

BOM Structure	Description	UMA	Thames	EVT2 UMA	DVT UMA-LVDS	DVT UMA-eDP	DVT PX5 1G-LVDS	DVT PX5 1G-eDP	DVT PX5 2G-LVDS		
M2@	Use Hudson-M2			V							
M3@	Use Hudson-M3	V	V		V	V	V	V	V		
930@	Use EC 930	V	V								
9012@	Use EC 9012			V	V	V	V	V	V		
UMA@	Display output from APU (UMA only or PX)	V	V	V	V	V	V	V	V		
DISO@	Display output from VGA (DIS only)										
VGALVDS@	VGA output LVDS (DIS only)										
VGA@	Use VGA (PX or DIS only)		V				V	V	V		
THA@	VGA: Thames		V				V	V	V		
SEY@	VGA: Seymour										
128@	Use VRAM channel A&B		V				V	V	V		
PX@	PX function		V				V	V	V		
BACO@	BACO function (PX4.0)		V								
NOBACO@	Without BACO function (DISO and PX5.0)						V	V	V		
TL@	LVDS Translator (for LVDS)	V	V	V	V		V		V		
EDP@	Use eDP Panel					V		V			
APUEDP@	APU output eDP					V		V			
VGAEDP@	VGA output eDP (DIS only)										
271@	Realtek ALC271x VB6	V	V	V	V	V	V	V	V		
281@	Realtek ALC281x										
ZERO@	ZERO Power ODD function										
FL@	Fresco FL1009 USB3.0 Controller			V							
8151@	LAN Atheros AR8151 10/100/1000M LAN			V	V	V	V	V	V		
8152@	LAN Atheros AR8152 10/100M LAN										
X76@	VRAM ID Table (Load By X76J)										
CONN@	Connector (Control by ME)										

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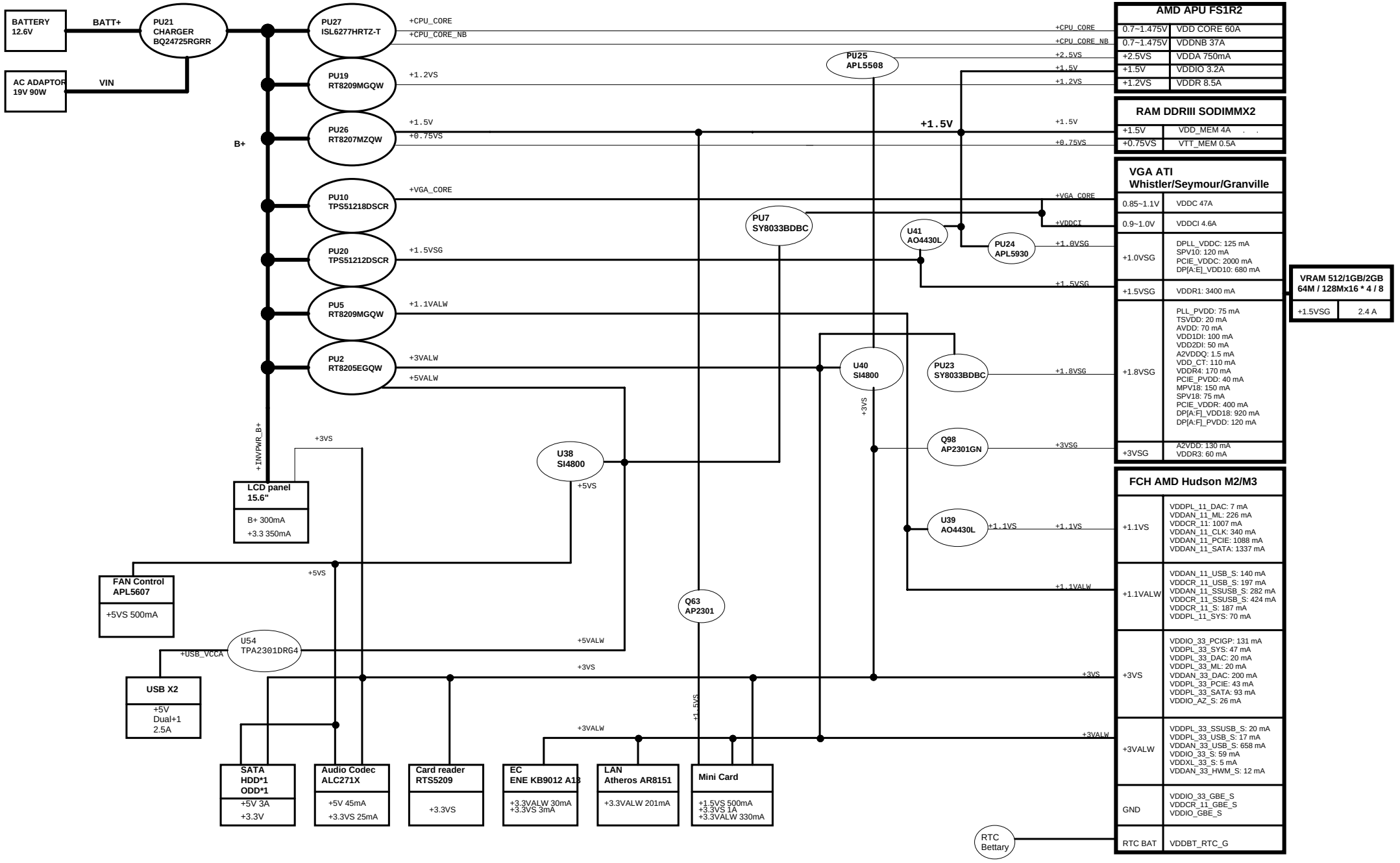

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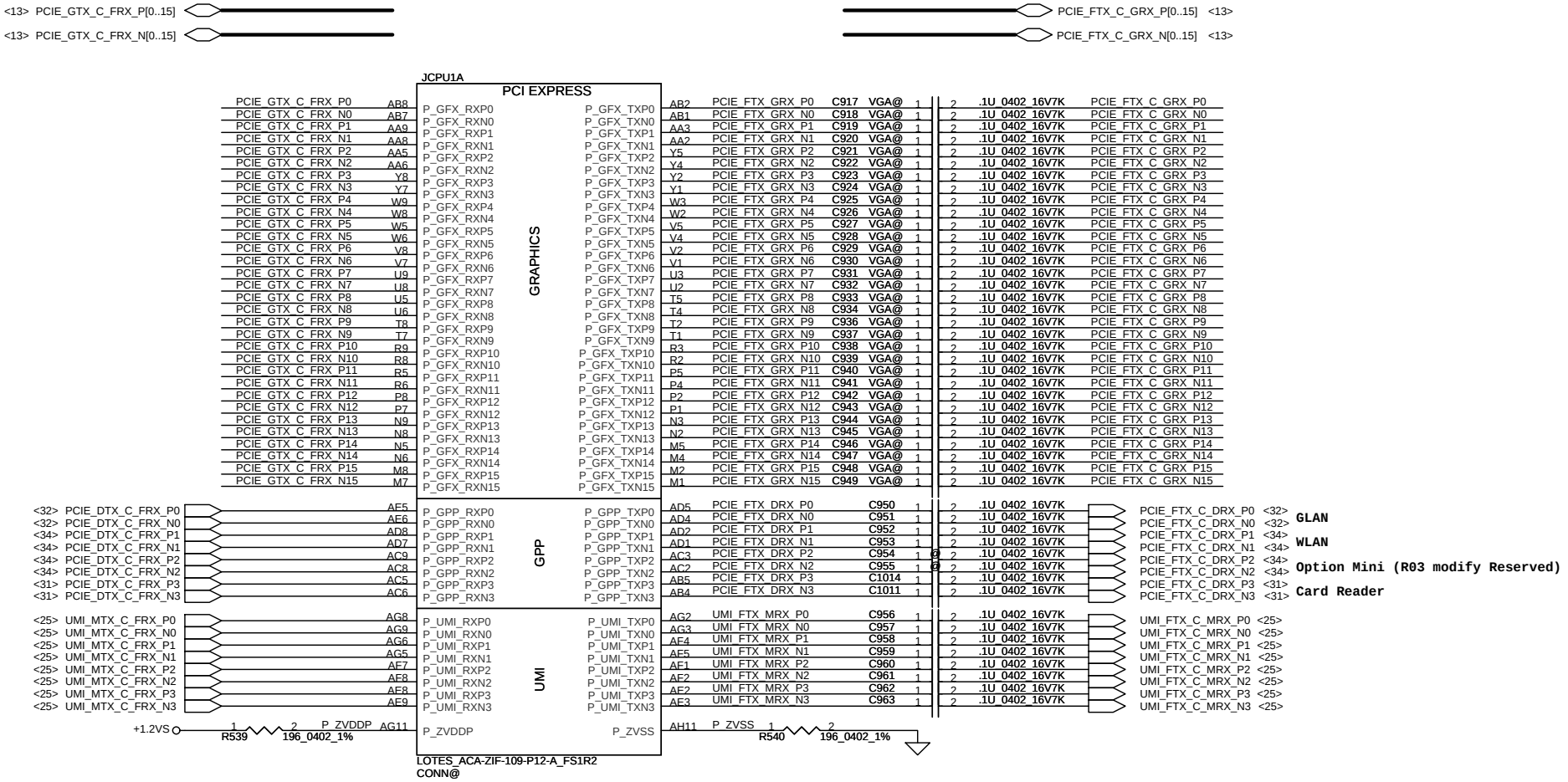

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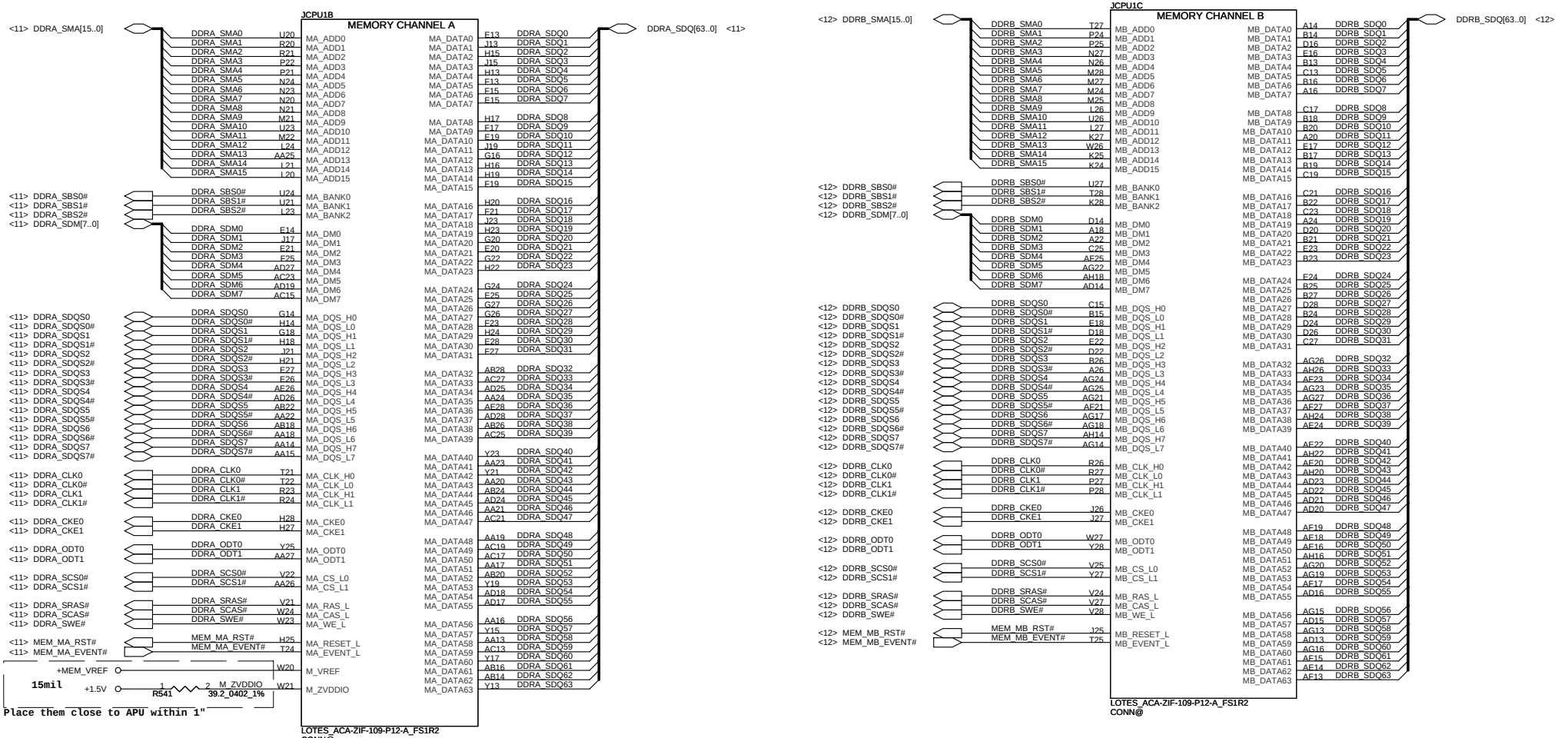
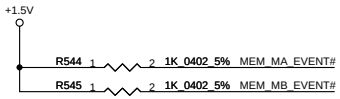
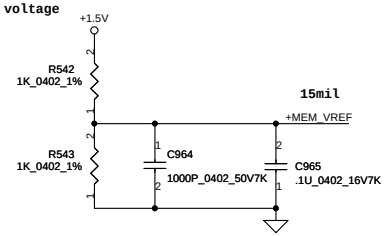


EVENT# pull high



0.75V reference voltage



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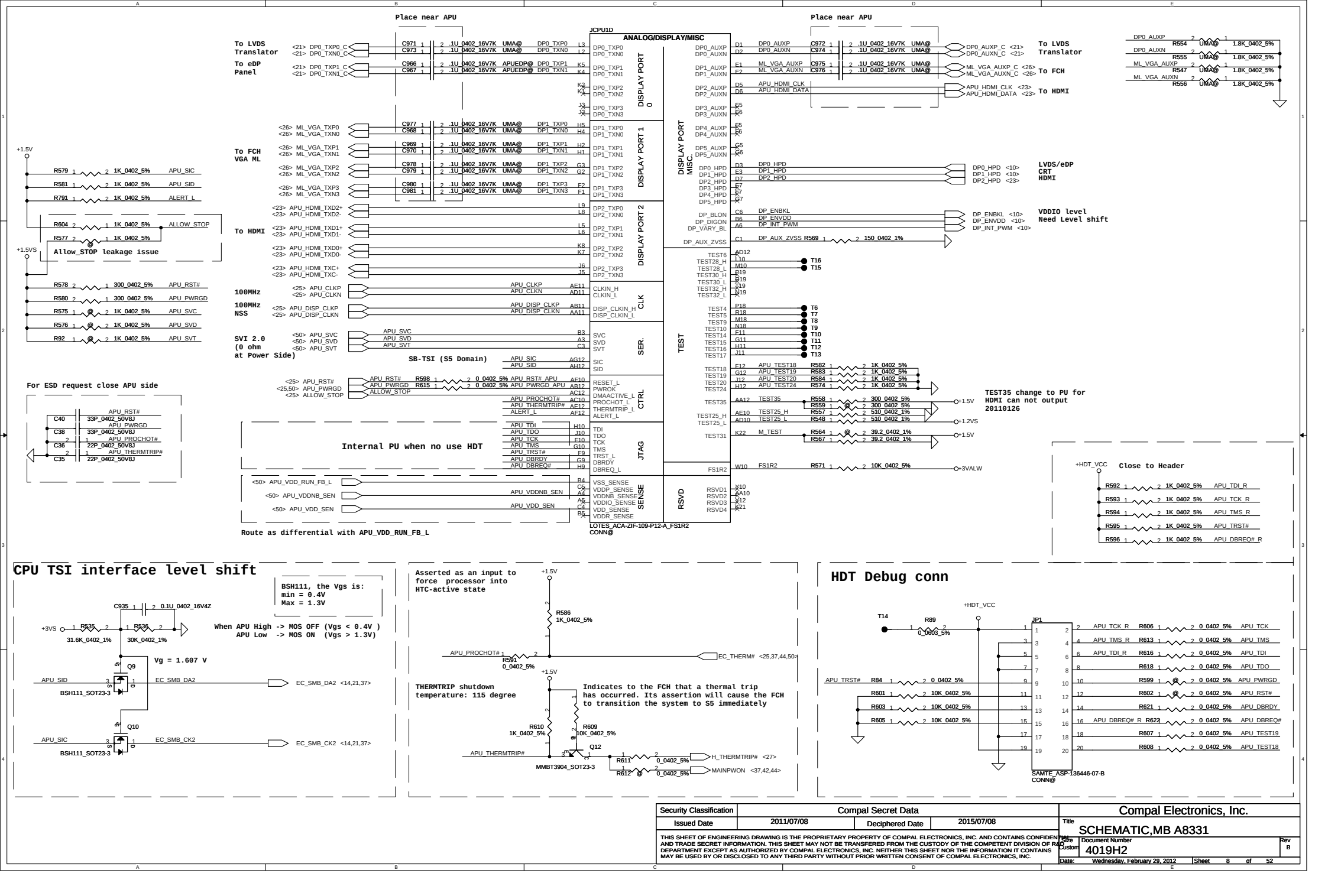

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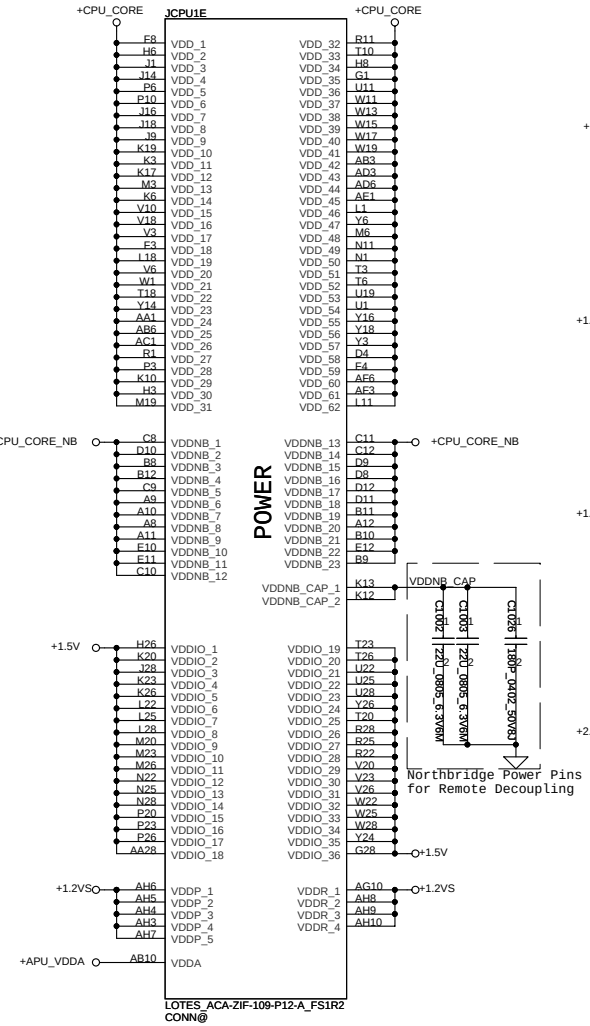
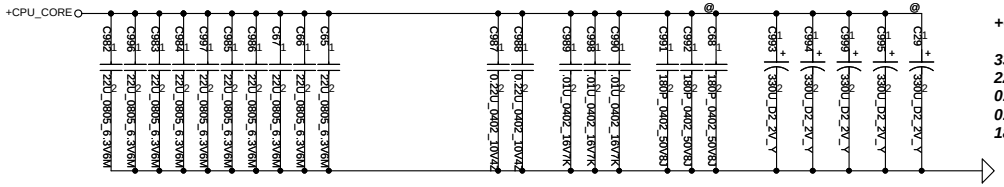
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A

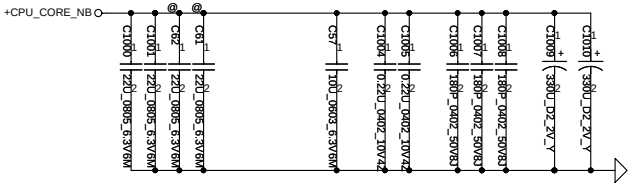


Northbridge Power Pins for Remote Decoupling



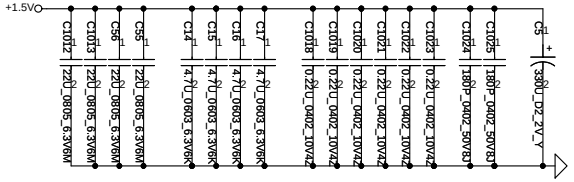
+CPU_CORE Decoupling

330uF x 3@ x2
22uF x 10 @ x5
0.22uF x2
0.01uF x3
180pF x2 @ x1



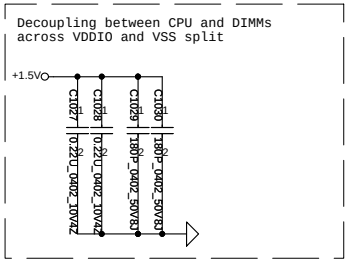
+CPU_CORE_NB Decoupling

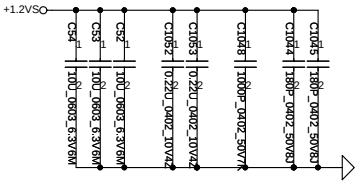
330uF x2
22uF x2 @ x5
10uF x1
0.22uF x2
180pF x3



+1.5V / VDDIO Decoupling

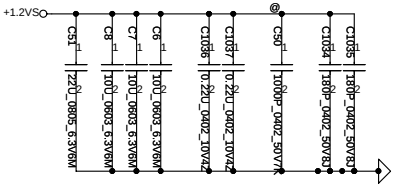
330uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1





VDDR Decoupling
Close JCPU1.AG10,AH8,AH9,AH10

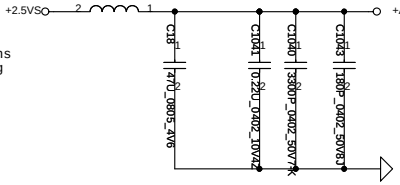
10uF x3
0.22uF x2
1000pF x1
180pF x2



VDDP Decoupling
Close JCPU1.AH3~7

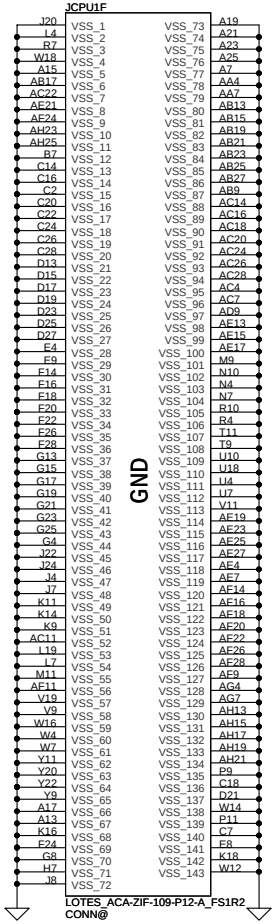
22uF x1
10uF x3
0.22uF x2
1000pF @x1
180pF x2

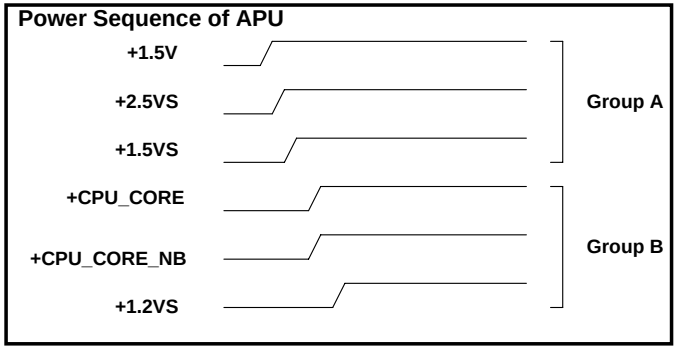
FBMA-L11-201209-221LMA30T_0805
L1



VDDA Decoupling

47uF x1
0.22uF x1
3300pF x1
180pF x1





Decoupling Caps.

Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0			0	19/11	7	5	17	3	1	1 / 1	13/3
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

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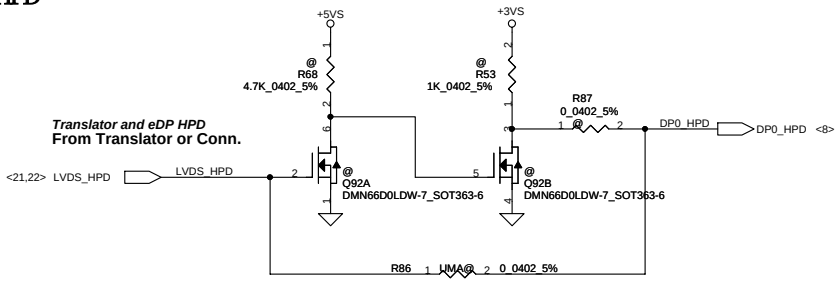
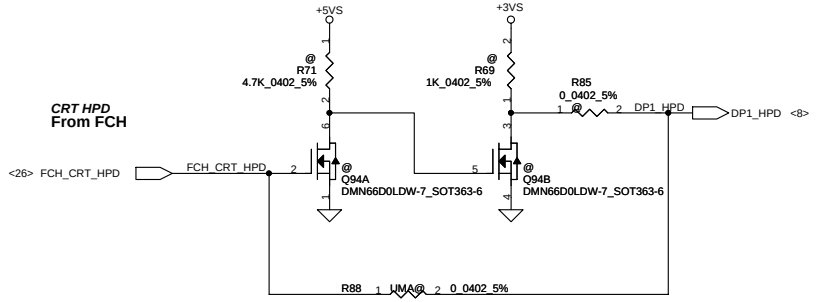
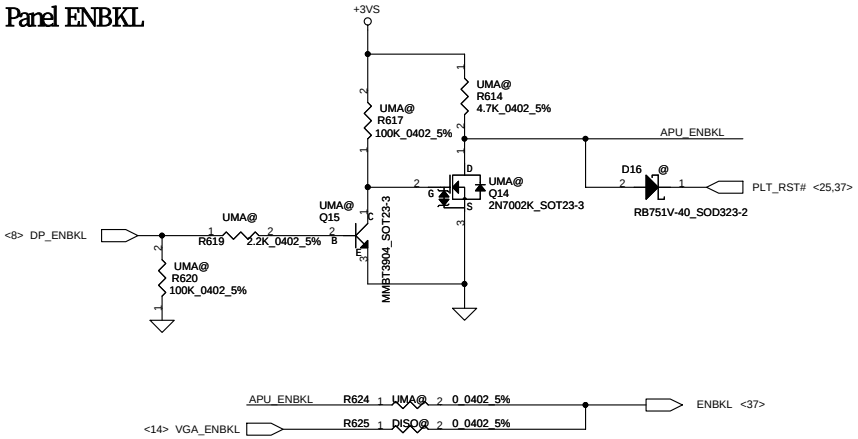
HPD

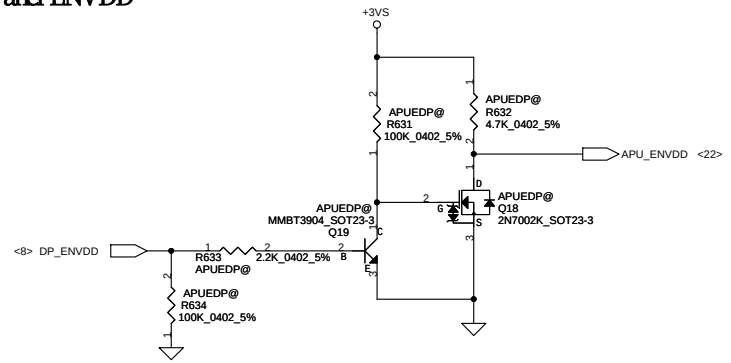




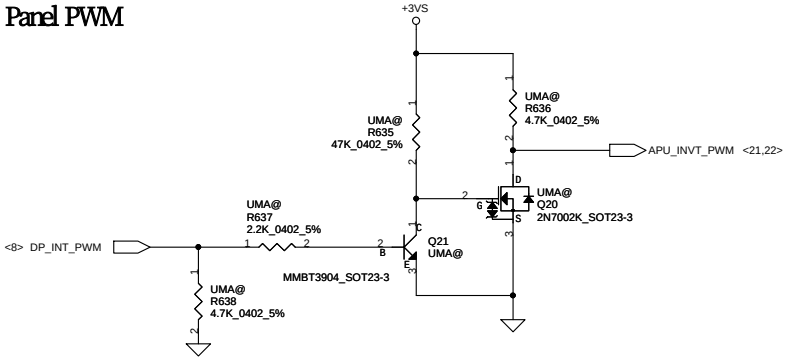
Panel ENBKL



Panel ENVDD



Panel PWM



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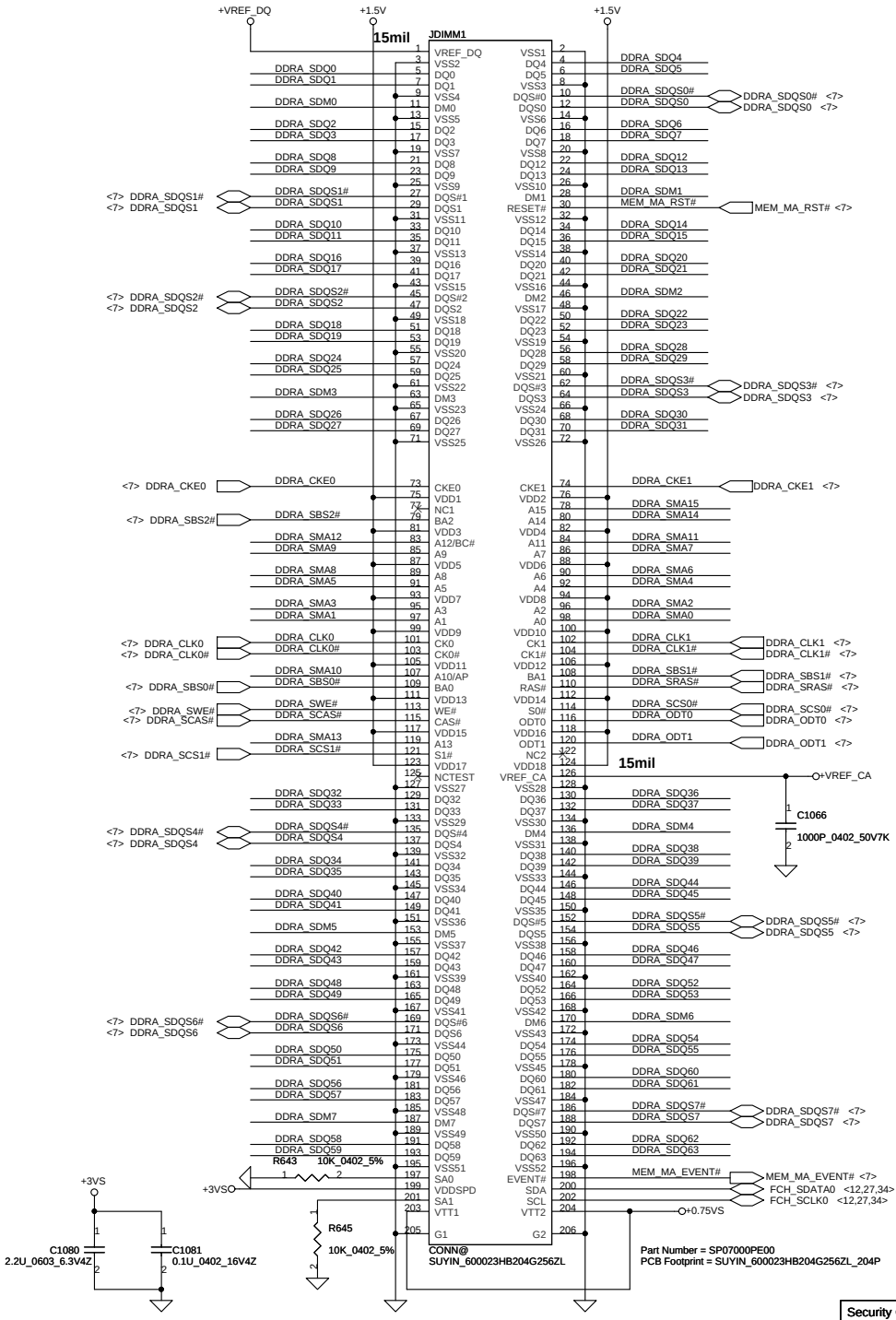
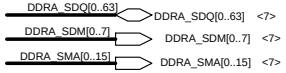
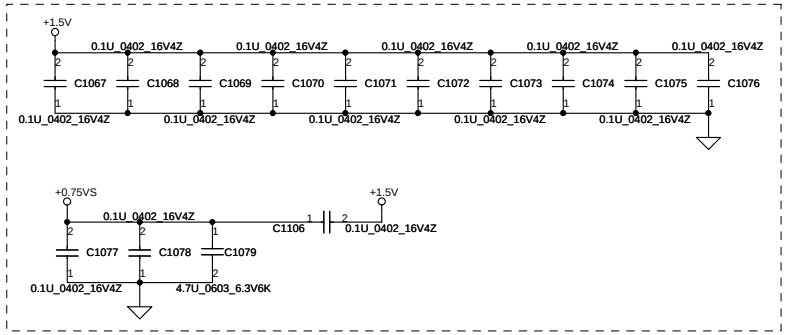
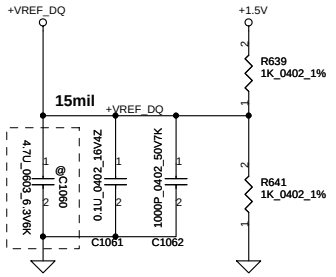
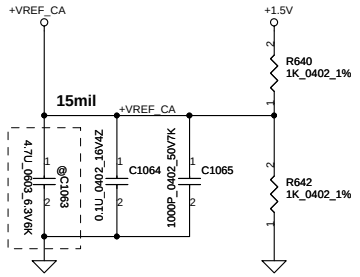




Place near DIMM1







DIMM_A STD H:8mm

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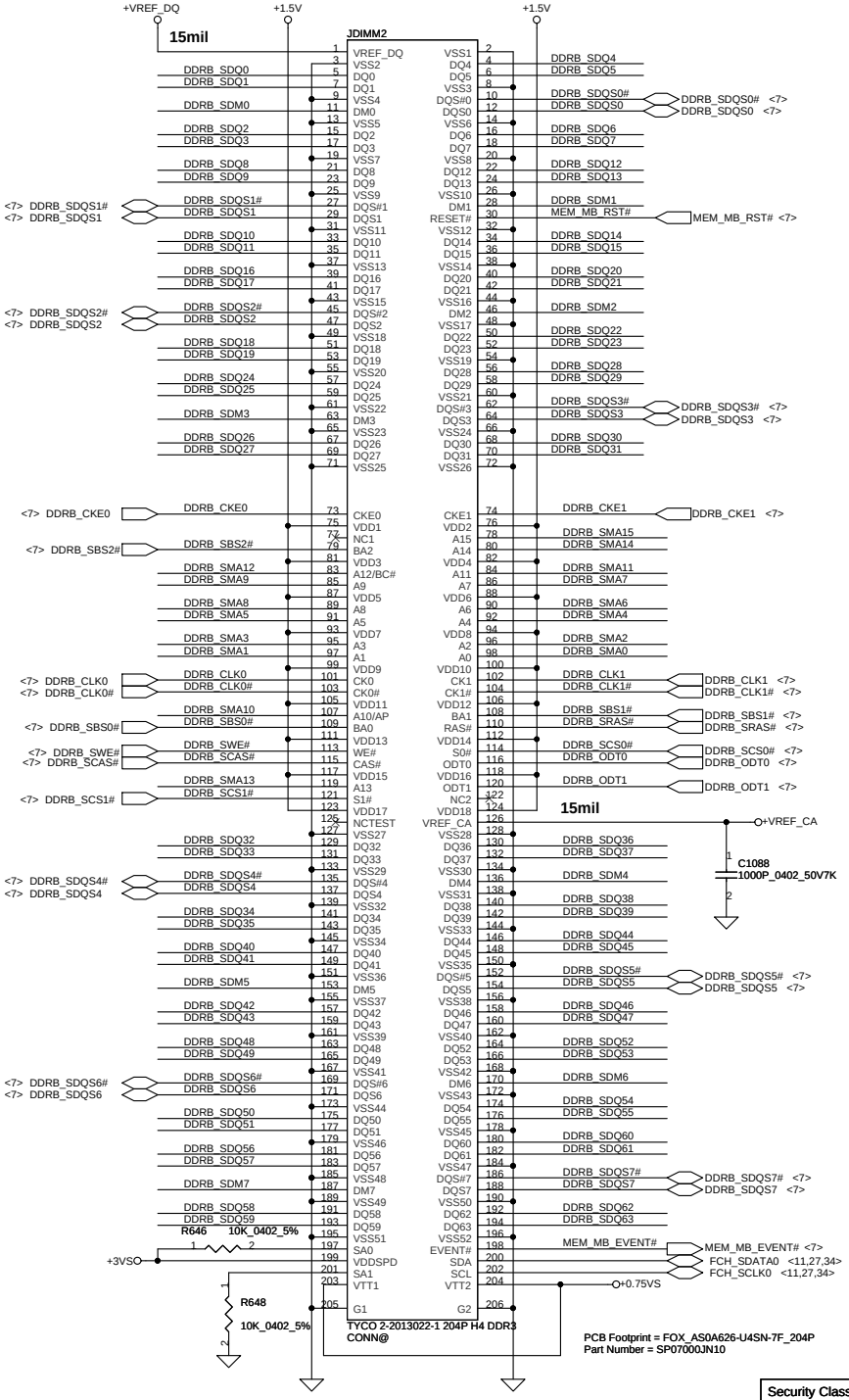

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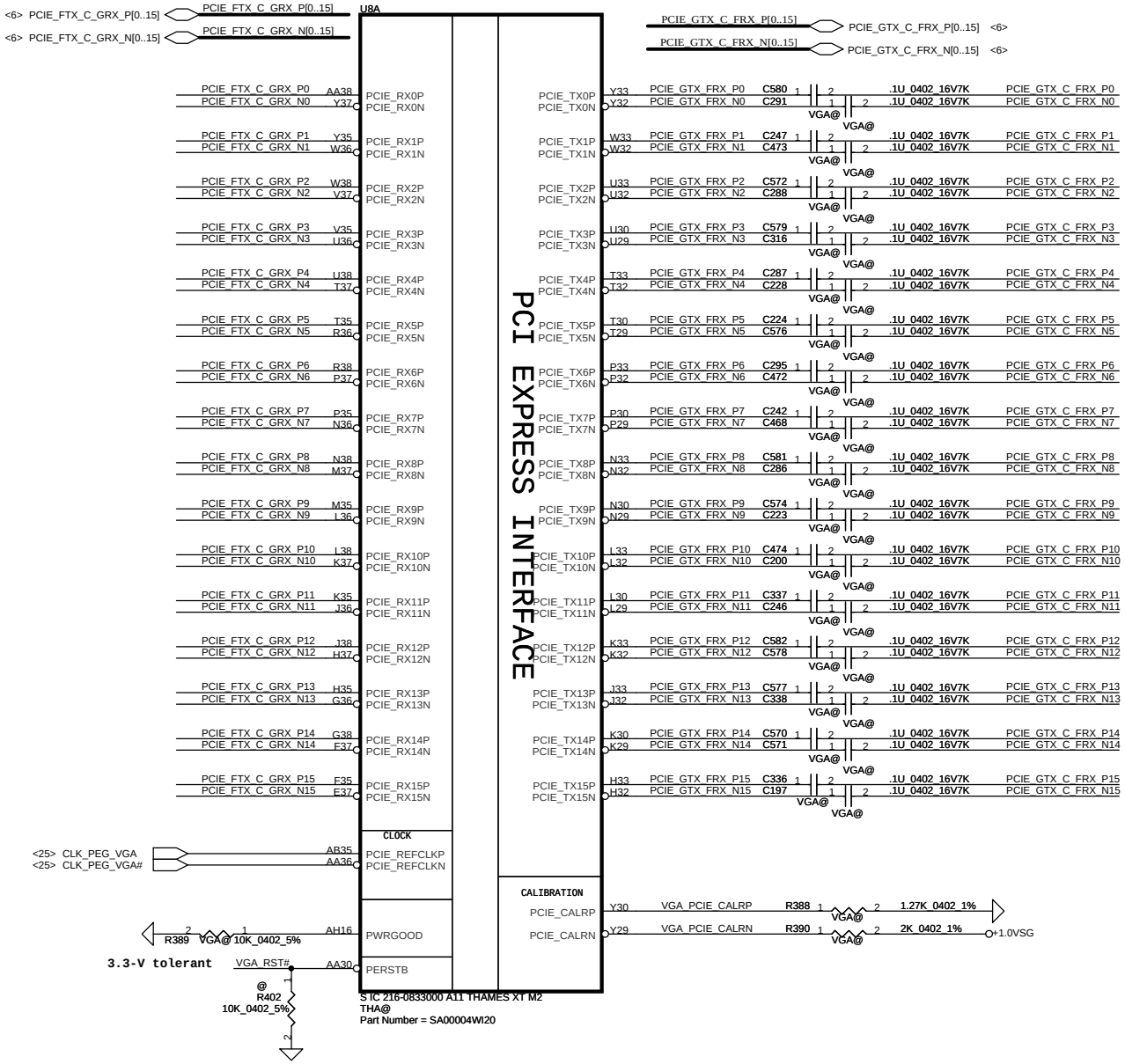
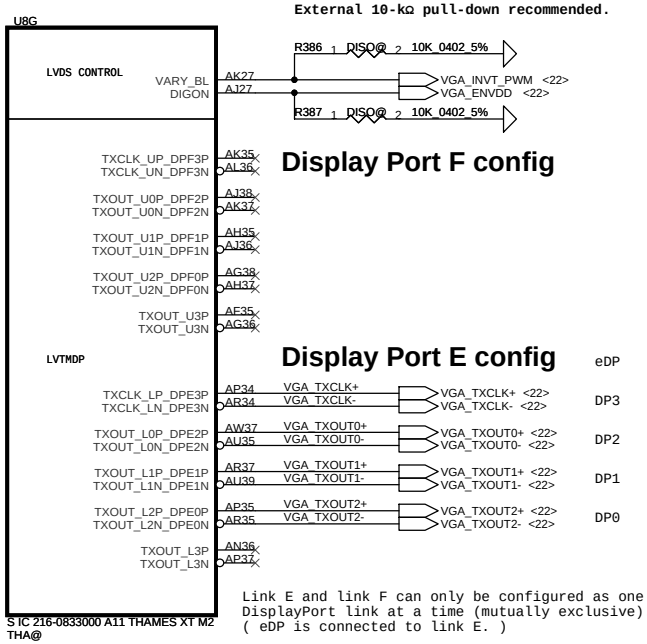
GFX PCIE LANE REVERSAL

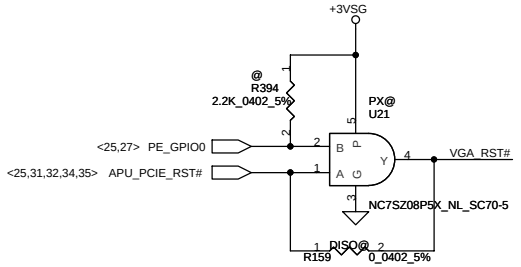


<DIGON>
Controls panel digital power on/off.
Active High
External 10-kΩ pull-down recommended.

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High
External 10-kΩ pull-down recommended.



Link E and link F can only be configured as one DisplayPort link at a time (mutually exclusive).
(eDP is connected to link E.)



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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines 256 MB 001 * the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

External VGA Thermal Sensor

U9 @ ADM1032ARMZ-2REEL_MSOP8

C324 @ 0.1U_0402_16V4Z

GPU_THERM_D+ — 2200P_0402_50V7K — C325 @

GPU_THERM_D-

VGA_SMB_CK2 <8,21,37>

VGA_SMB_DA2 <8,21,37>

THM_ALERT#

R391 @ 4.7K_0402_5%

R03 modify BOM

R392 4.7K_0402_5% VGA@

R393 4.7K_0402_5% VGA@

VGA@ Q8A DMN66D0LDW-7_SOT363-6

VGA@ Q8B DMN66D0LDW-7_SOT363-6

VRAM ID

DVPDATA	ID3	ID2	ID1	ID0	Van SPD Name
00h	0	0	0	0	SAM 933 K4W1G1646G-BC11 64Mx16
01h	0	0	0	1	SAM 933 K4W2G1646C-HC11 128Mx16
02h	0	0	1	0	
03h	0	0	1	1	
04h	0	1	0	0	AMD 900 23EY2387MB11 64Mx16
05h	0	1	0	1	AMD 900 23EY4187MA11 128Mx16
06h	0	1	1	0	
07h	0	1	1	1	
08h	1	0	0	0	HYN 900 H5TQ1G63DFR-11C
09h	1	0	0	1	HYN 900 H5TQ2G63BFR-11C
0Ah	1	0	1	0	
0Bh	1	0	1	1	
0Ch	1	1	0	0	MIC 900 MT41J64M16JT-107G:G
0Dh	1	1	0	1	MIC 900 MT41J128M16HA-107G:D
0Eh	1	1	1	0	
0Fh	1	1	1	1	

Global Swap Lock on Multiple GPUs

GPIO5 fast-power reduction: HW control will casue display disturb should use SW method control

GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N

DISCRETE ONLY — PD100K at EC side

R02 modify, R03 modify BOM

GPIO7 Controls backlight on/off. Active High ,need external PD

if GPIO22 High ,GPIO 11-13->CFG[0:2] Config ROM type ,GPU has internal PD

GPIO6,15,16,20 Voltage control signal GPIO6,15 no use can NC Thermal monitor interrupt

Critical temperature fault

Reserved

External BIOS device ON(1)/OFF(0) inter PD

Internal Debug no use can floating ON(1)/OFF(0)

Stereo Sync no use can NC

For ATI Cross fire no use can NC

ROM

Not share via for other GND

VREFG:Use a voltage divider to set VREFG = 1.80 V / 3 (or 0.60-V nominal).

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

CRT,HDMI DDC

HDMI

LVDS

CRT

Outputs are open drain and 5-V tolerant. External pull-up resistors to 3.3 V or 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before or after VDDC and VDD_CT are powered up.

A source detection pull-down resistor (100-k 5% tolerance) is required on each AUXP signal and a pull-up resistor (100-k 5% tolerance) to 3.3 V is required on each AUXN signal.

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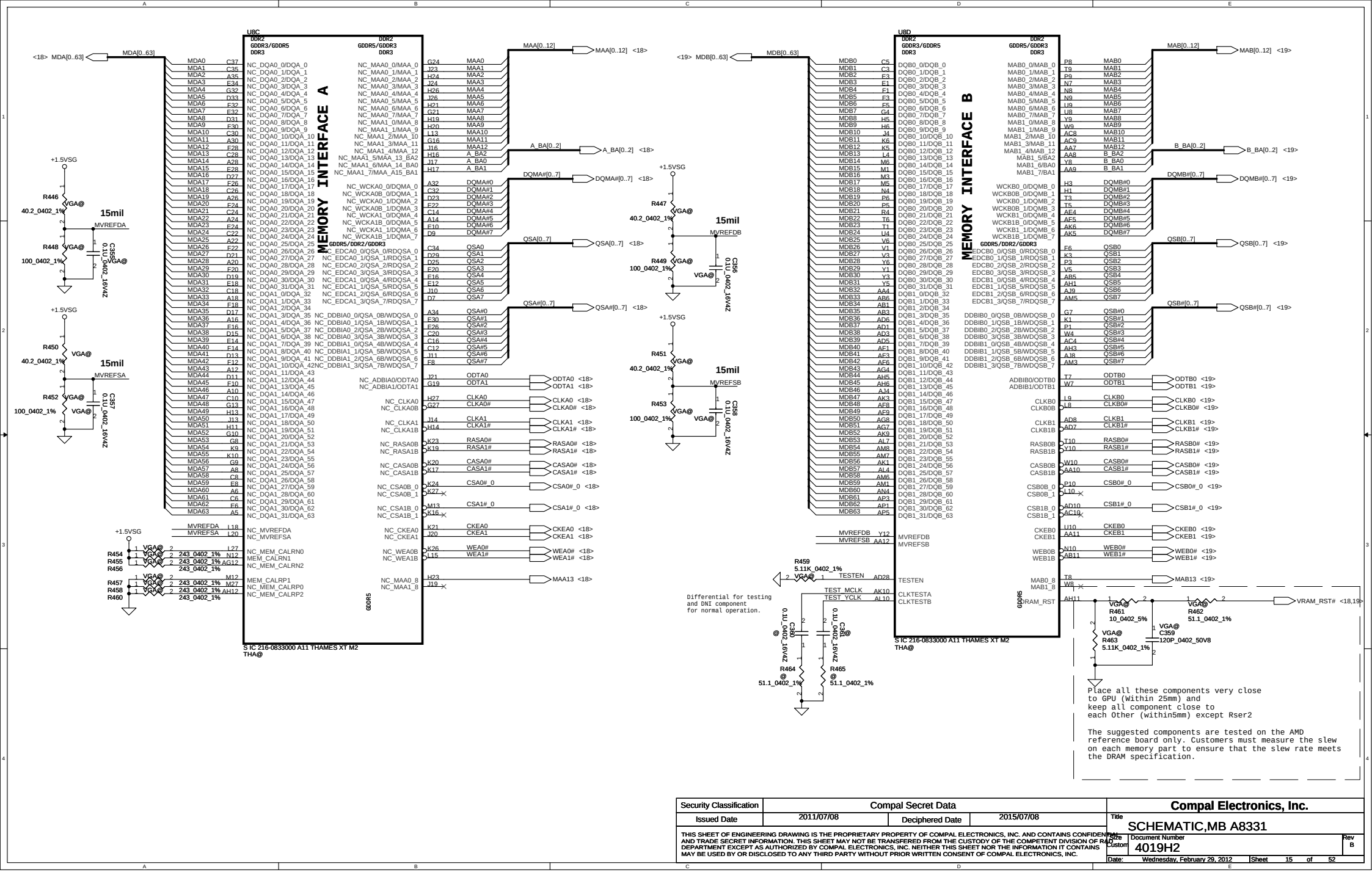

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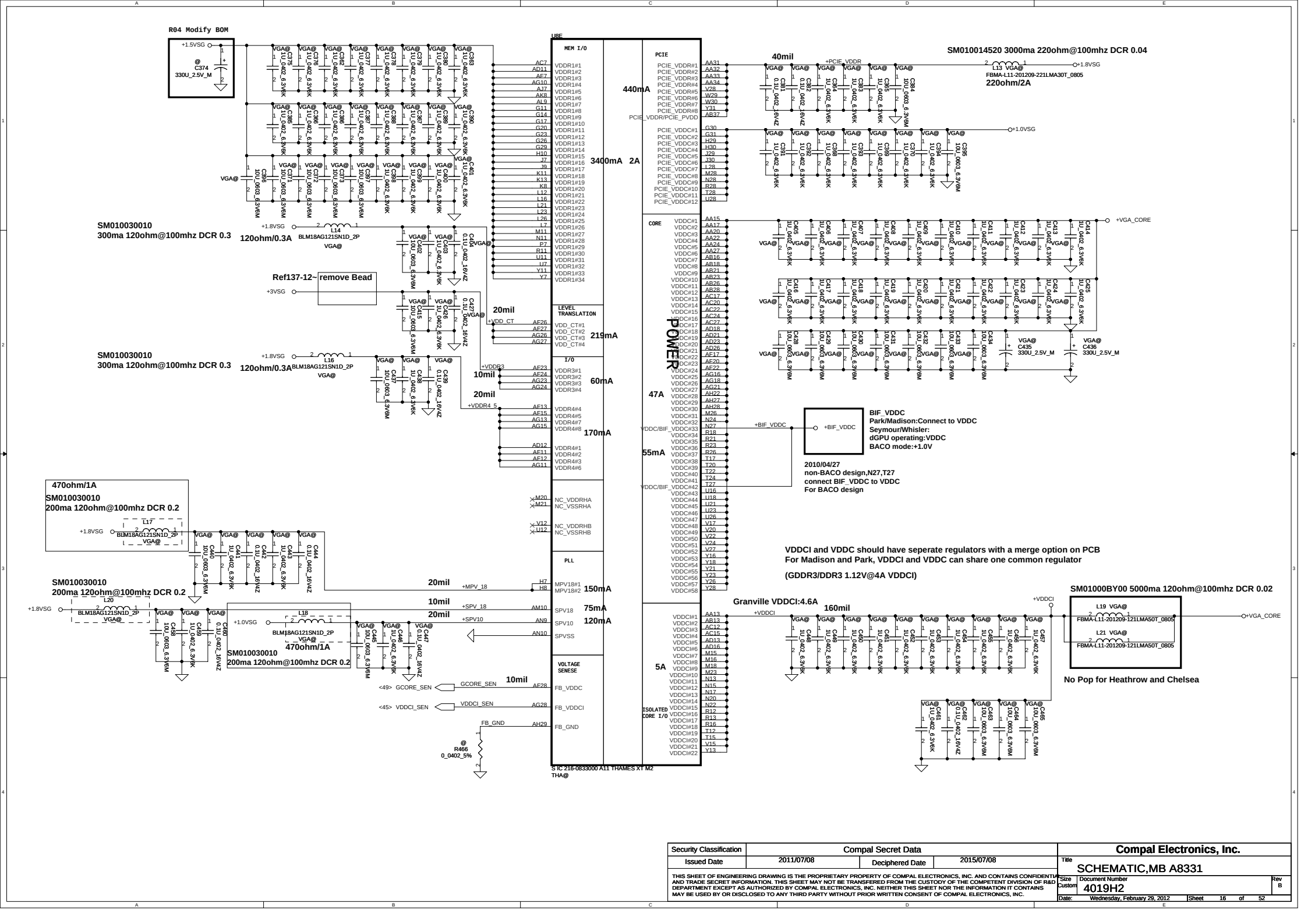

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DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

Seymour/Whistler：
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

U8F

GND

S IC 216-0833000 A11 THAMES XT M2
THA@

REF137-13 update

PX_EN <20>

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

U8H

DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER

Manhatann:300mA
Seymour:150mA
Manhatann:220mA
Seymour:110mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2

DP mode:300mA
LVDS mode:440mA
DP mode:220mA
LVDS mode:240mA

R467 150_0402_1%
R468 150_0402_1%
R470 150_0402_1%

S IC 216-0833000 A11 THAMES XT M2
THA@

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

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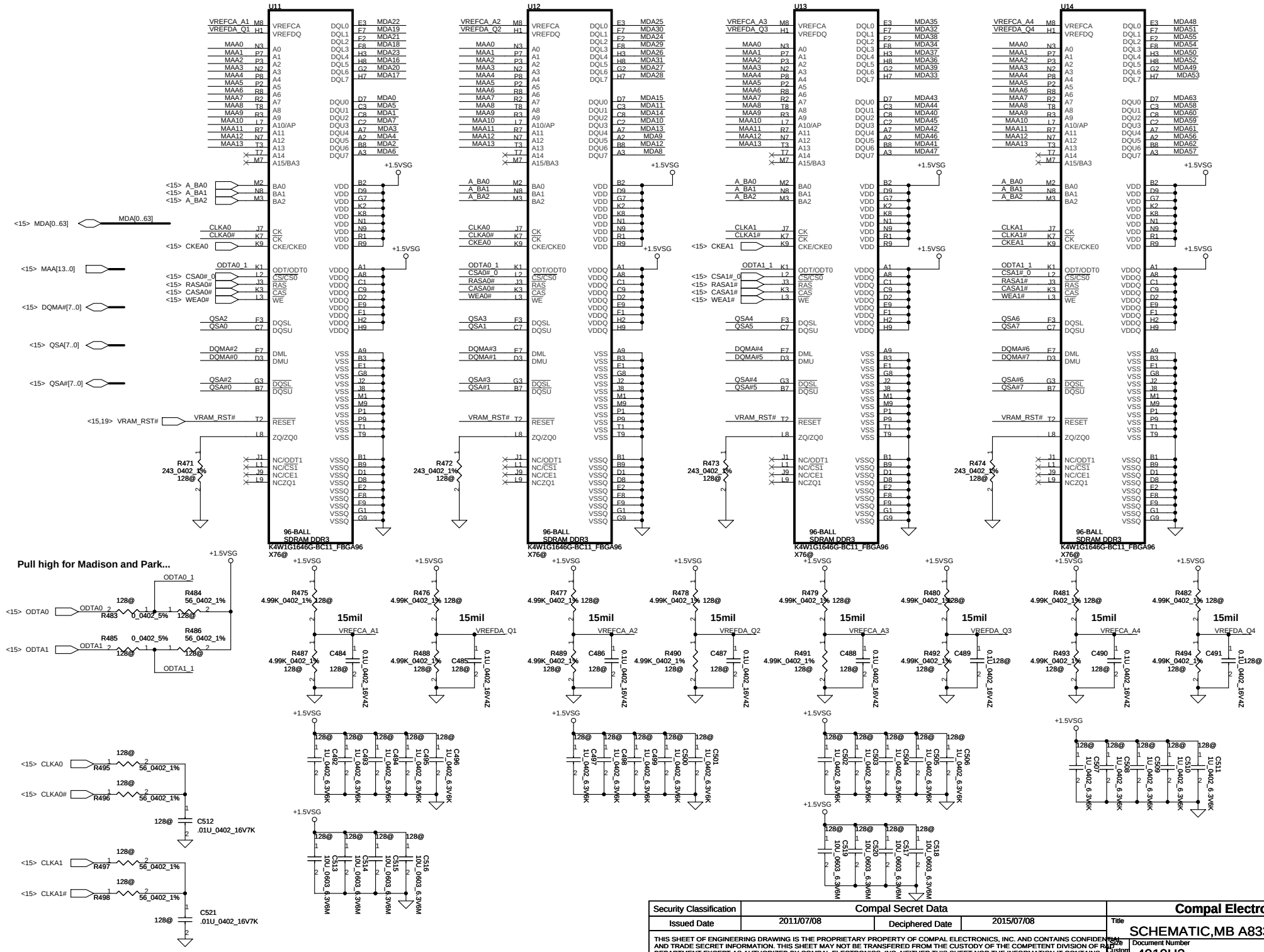

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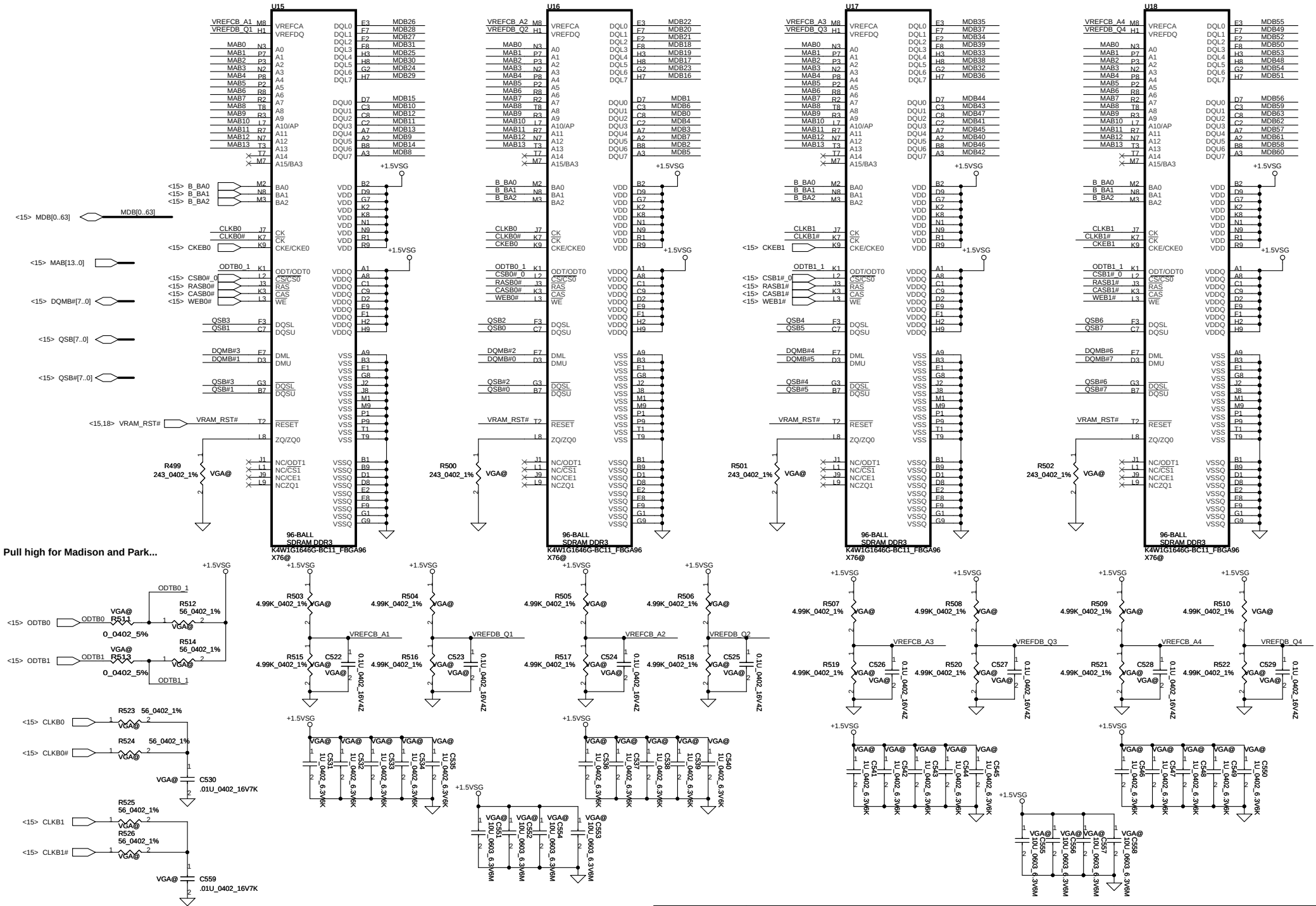

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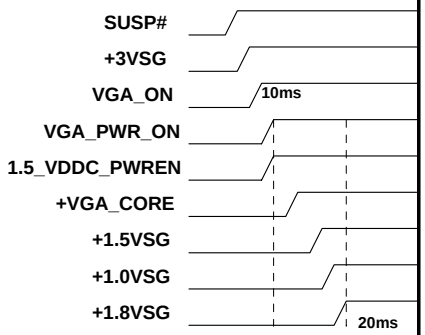
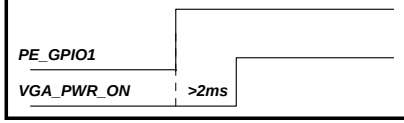
Power Sequence of Thames



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

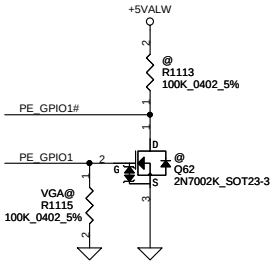


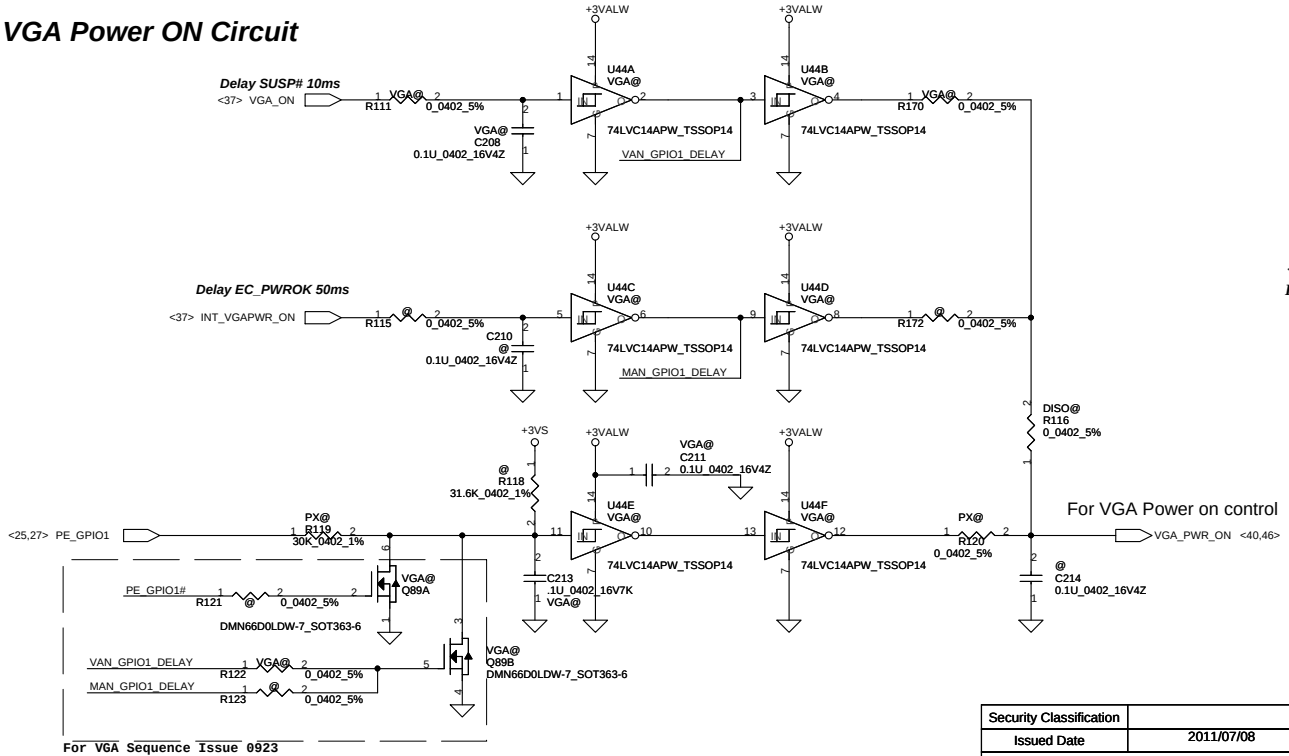
VGA Muxless and Dis only Status Mapping table			
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

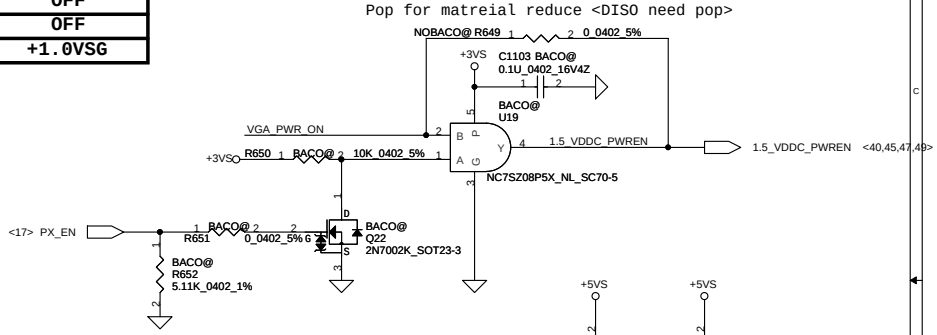
VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

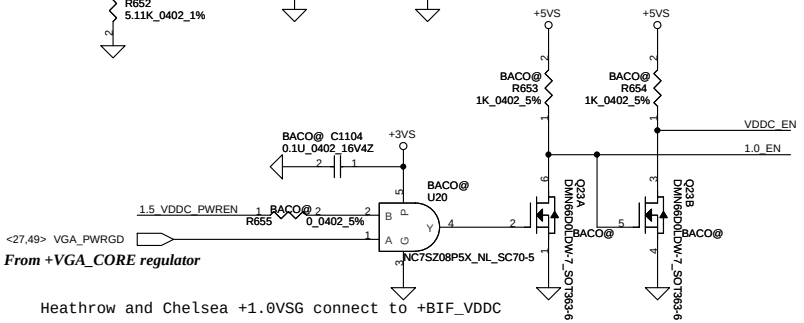
VGA Power ON Circuit



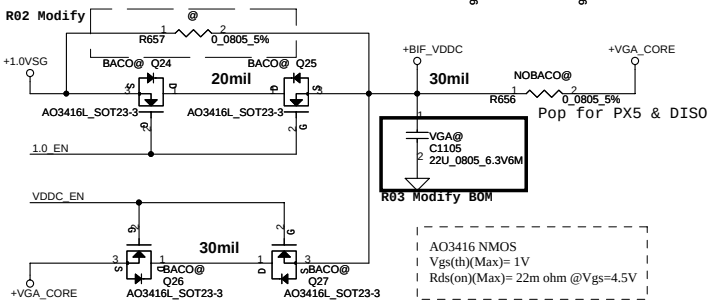


Pop for matreial reduce <DISO need pop>





Heathrow and Chelsea +1.0VSG connect to +BIF_VDDC



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Swap for Meet 40 pin LVDS define (FW Support)

+3VS — 30mil — R1160 2 TL@ 1 0_0603_5% — 30mil — +3VS_PS

Close to Pin3

DP_V33 — C20 10U_0603_6.3V6M TL@ — C1482 0.1U_0402_16V4Z TL@ — C1483 0.1U_0402_16V4Z TL@

+1.2VS — 60mil — R1178 2 TL@ 1 0_0603_5% — SWR_V12

R04 Modify BOM

+3VS_PS — L76 TL@ FBMA-L11-201209-221LMA30T_0805 — DP_V33 — 40mil

+3VS_PS — L78 TL@ FBMA-L11-201209-221LMA30T_0805 — SWR_VDD — 60mil

SWR_V12 — L77 4.7UH_PG031B-4R7MS_1.1A_20% @ — SWR_LX — 60mil

U46 TL@

DP_V33	3			
SWR_VDD PVCC	13 18	Power	LVDS	TXEC+ TXEC- 19 20 — APU_TXOUT0- APU_TXOUT0+ — APU_TXOUT0- <22> APU_TXOUT0+ <22>
SWR_LX SWR_VCCK VCCK	12 11 27			TXE2+ TXE2- 21 22 — APU_TXOUT1- APU_TXOUT1+ — APU_TXOUT1- <22> APU_TXOUT1+ <22>
DP_V12	7			TXE1+ TXE1- 23 24 — APU_TXOUT2- APU_TXOUT2+ — APU_TXOUT2- <22> APU_TXOUT2+ <22>
				TXE0+ TXE0- 25 26 — APU_TXOUT_CLK- APU_TXOUT_CLK+ — APU_TXOUT_CLK- <22> APU_TXOUT_CLK+ <22>

RTD2132S

AUX_P AUX_N		DP-IN	GPIO	GPIO(PWM OUT) GPIO(Panel_VCC) GPIO(PWM IN) GPIO(BL_EN) 14 15 16 17 — R1161 0_0402_5% R1162 0_0402_5% — TL_INVT_PWM <22> TL_ENVDD <22> APU_INVT_PWM <10,22> TL_BKOFF# <22>
LANE0P LANE0N				
CIICSCL1 CIICSDA1		Other	LVDS EDID	MIICSCL1 MIICDA1 — 29 28 — APU_LVDS_CLK APU_LVDS_DAT — APU_LVDS_CLK <22> APU_LVDS_DAT <22>
HPD	32		ROM	MIICSCL0 MIICSDA0 — 31 30 — MIIC_SCL MIIC_SDA
DP_REXT DP_GND	8 4			GND 33

<8> DP0_AUXP_C — DP0_AUXP_C 2
<8> DP0_AUXN_C — DP0_AUXN_C 1
<8> DP0_TXP0_C — DP0_TXP0_C 5
<8> DP0_TXN0_C — DP0_TXN0_C 6
CSCL — CSCL 9
CSDA — CSDA 10
TL_HPD — TL_HPD 32

RTD2132S-VE-CG_QFN32_5X5
Part Number = SA00004EU10
R04 Modify BOM

Close to L2 — C21 10U_0603_6.3V6M TL@ — C1485 0.1U_0402_16V4Z TL@ — C1486 22U_0805_6.3V6M TL@ — C1487 0.1U_0402_16V4Z TL@ — C1488 0.1U_0402_16V4Z TL@ — SWR_VDD

Close to Pin13

Close to P18

<10,22> LVDS_HPD — R1169 1K_0402_5% TL@ — R1168 100K_0402_5% TL@ — R30 12K_0402_1% TL@

Change to 12Kohm 1% (DG ref.)
20101114

Pop when no use EEEPRON

@ R1177 10K_0402_5%

+3VS_PS

APU_LVDS_DAT	R1163	4.7K_0402_5%
APU_LVDS_CLK	R1164	4.7K_0402_5%
MIIC_SCL	R1165	4.7K_0402_5%
MIIC_SDA	R1166	4.7K_0402_5%
CSCL	R1167	4.7K_0402_5%
CSDA	R1170	4.7K_0402_5%

Close to L3 — C1489 22U_0805_6.3V6M TL@ — C1490 0.1U_0402_16V4Z TL@ — C1491 0.1U_0402_16V4Z TL@ — C1492 0.1U_0402_16V4Z TL@ — SWR_V12

Close to Pin27

Close to Pin7

APU Co-lay eDP function

<8> DP0_TXP1_C
<8> DP0_TXN1_C

DP0_TXP0_C	R1171	APUEDP@	0_0402_5%	APU_TXOUT2+
DP0_TXN0_C	R1172	APUEDP@	0_0402_5%	APU_TXOUT2-
DP0_TXP1_C	R1173	APUEDP@	0_0402_5%	APU_TXOUT1+
DP0_TXN1_C	R1174	APUEDP@	0_0402_5%	APU_TXOUT1-
DP0_AUXP_C	R1175	APUEDP@	0_0402_5%	APU_LVDS_CLK
DP0_AUXN_C	R1176	APUEDP@	0_0402_5%	APU_LVDS_DAT

EEROM

SWR_VDD — U2 TL@ — CAT24C64WI-GT3_SO8

8	VCC	A0	1
7	WP	A1	2
6	SCL	A2	3
5	SDA	GND	4

MIIC_SCL
MIIC_SDA

+3VS — 10K_0402_5% R1182 — 10K_0402_5% R1181 — +3VS_PS

<37> TL_DATA — @ R1179 0_0402_5% — CSDA — TL@ Q90A DMN66D0LDW-7_SOT363-6 — TL@ Q90B — EC_SMB_DA2 — EC_SMB_DA2 <8,14,37>

<37> TL_CLK — @ R1180 0_0402_5% — CSCL — DMN66D0LDW-7_SOT363-6 — EC_SMB_CK2 — EC_SMB_CK2 <8,14,37>

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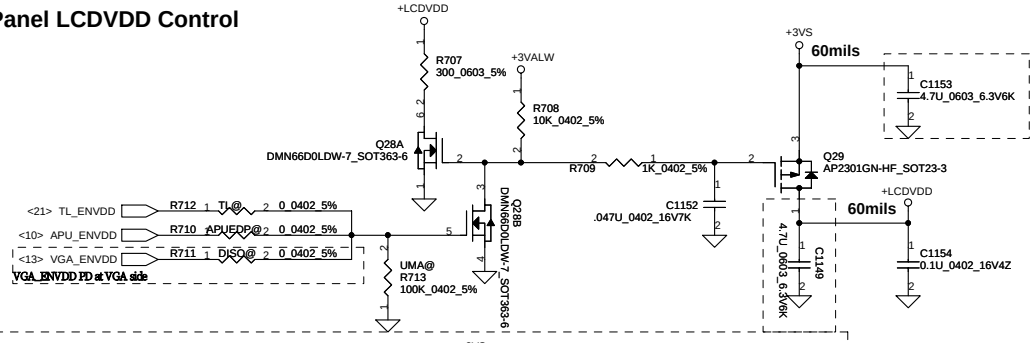
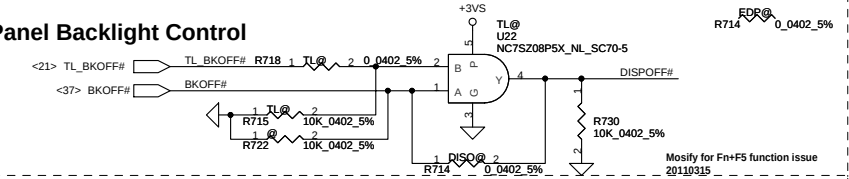
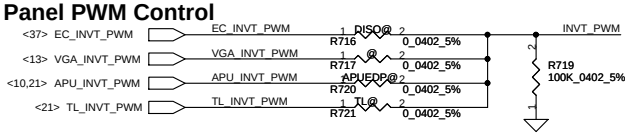
Panel LCDVDD Control



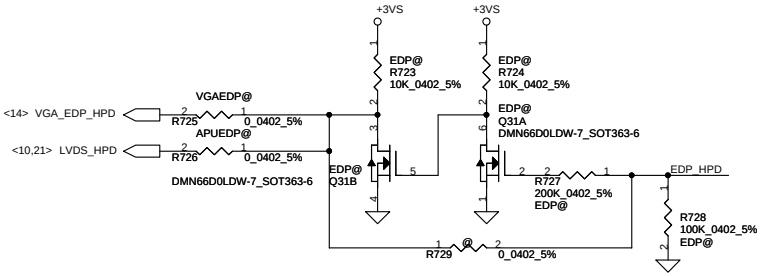
Panel Backlight Control



Panel PWM Control



eDP HDP for APU and VGA



Translator LVDS Output

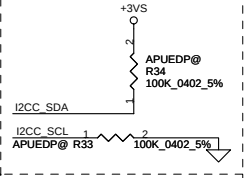
Place near LVDS Conn

	<21> APU_TXOUT0-	UMA@ R1240	0_0402_5%	TXOUT0-
	<21> APU_TXOUT0+	UMA@ R1241	0_0402_5%	TXOUT0+
eDP_TX1N / eDP_TX1P	<21> APU_TXOUT1-	UMA@ R1242	0_0402_5%	TXOUT1-
	<21> APU_TXOUT1+	UMA@ R1243	0_0402_5%	TXOUT1+
eDP_TX0N / eDP_TX0P	<21> APU_TXOUT2-	UMA@ R1244	0_0402_5%	TXOUT2-
	<21> APU_TXOUT2+	UMA@ R1245	0_0402_5%	TXOUT2+
	<21> APU_TXOUT_CLK-	UMA@ R1246	0_0402_5%	TXCLK-
	<21> APU_TXOUT_CLK+	UMA@ R1247	0_0402_5%	TXCLK+
eDP_AUXP / eDP_AUXN	<21> APU_LVDS_CLK	UMA@ R1248	0_0402_5%	I2CC_SCL
	<21> APU_LVDS_DAT	UMA@ R1249	0_0402_5%	I2CC_SDA

VGA LVDS Output

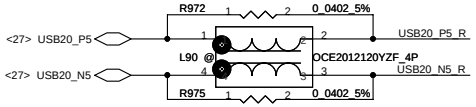
	<13> VGA_TXOUT0-	VGALVDS@ R732	0_0402_5%	TXOUT0-
	<13> VGA_TXOUT0+	VGALVDS@ R735	0_0402_5%	TXOUT0+
eDP_TX1N / eDP_TX1P	<13> VGA_TXOUT1-	VGALVDS@ R731	0_0402_5%	TXOUT1-
	<13> VGA_TXOUT1+	VGALVDS@ R733	0_0402_5%	TXOUT1+
eDP_TX0N / eDP_TX0P	<13> VGA_TXOUT2-	VGALVDS@ R734	0_0402_5%	TXOUT2-
	<13> VGA_TXOUT2+	VGALVDS@ R736	0_0402_5%	TXOUT2+
	<13> VGA_TXCLK-	VGALVDS@ R737	0_0402_5%	TXCLK-
	<13> VGA_TXCLK+	VGALVDS@ R738	0_0402_5%	TXCLK+
eDP_AUXP / eDP_AUXN	<14> VGA_LCD_CLK	VGALVDS@ R741	0_0402_5%	I2CC_SCL
	<14> VGA_LCD_DAT	VGALVDS@ R742	0_0402_5%	I2CC_SDA

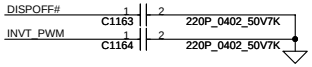
DG ref. Need close to eDP Conn. 201011251400

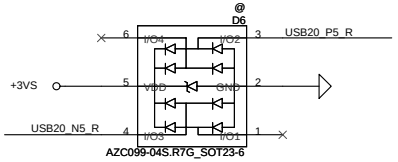


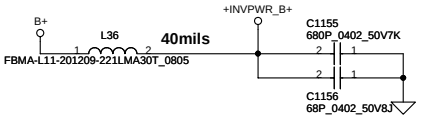
VGA Co-lay eDP function

VGAEDP@ R732	1U_0402_16V7K	
VGAEDP@ R735	1U_0402_16V7K	
VGAEDP@ R737	1U_0402_16V7K	
VGAEDP@ R738	1U_0402_16V7K	
VGAEDP@ R741	1U_0402_16V7K	
VGAEDP@ R742	1U_0402_16V7K	

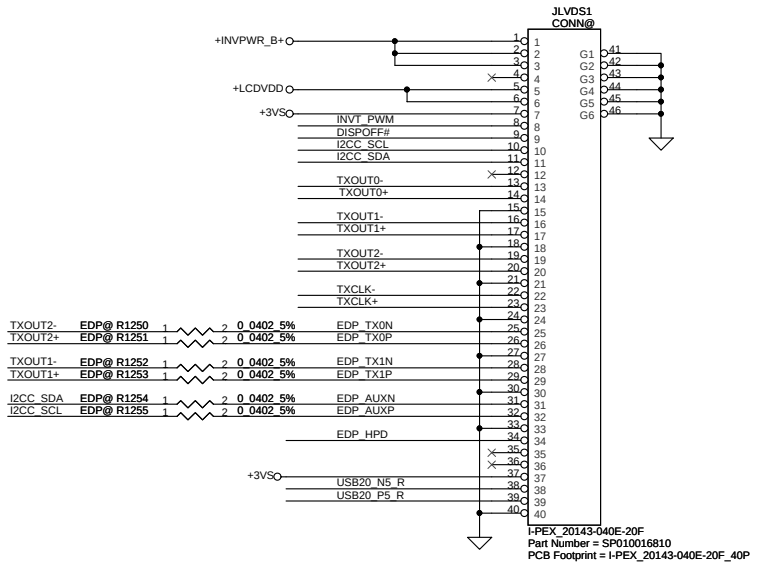








LCD/LED PANEL Conn.



UMA/DIS LVDS/eDP Mapping table				
UMA		DIS		Panel
LVDS	eDP	LVDS	eDP	Conn.
APU_TXOUT0+ APU_TXOUT0-		VGA_TXOUT0+ VGA_TXOUT0-		TXOUT0+ TXOUT0-
APU_TXOUT1+ APU_TXOUT1-	DP0_TXP1_R DP0_TXN1_R	VGA_TXOUT1+ VGA_TXOUT1-	eDP_TX1P eDP_TX1N	TXOUT1+ TXOUT1-
APU_TXOUT2+ APU_TXOUT2-	DP0_TXP0_R DP0_TXN0_R	VGA_TXOUT2+ VGA_TXOUT2-	eDP_TX0P eDP_TX0N	TXOUT2+ TXOUT2-
APU_TXOUT_CLK+ APU_TXOUT_CLK-		VGA_TXCLK+ VGA_TXCLK-		TXCLK+ TXCLK-
APU_TZOUT0+ APU_TZOUT0-		VGA_TZOUT0+ VGA_TZOUT0-		TZOUT0+ TZOUT0-
APU_TZOUT1+ APU_TZOUT1-		VGA_TZOUT1+ VGA_TZOUT1-		TZOUT1+ TZOUT1-
APU_TZOUT2+ APU_TZOUT2-		VGA_TZOUT2+ VGA_TZOUT2-		TZOUT2+ TZOUT2-
APU_TZOUT_CLK+ APU_TZOUT_CLK-		VGA_TZCLK+ VGA_TZCLK-		TZCLK+ TZCLK-
APU_LVDS_CLK APU_LVDS_DAT	DP0_AUXP_R DP0_AUXN_R	VGA_LCD_CLK VGA_LCD_DATA	eDP_AUXP eDP_AUXN	I2CC_SCL I2CC_SDA

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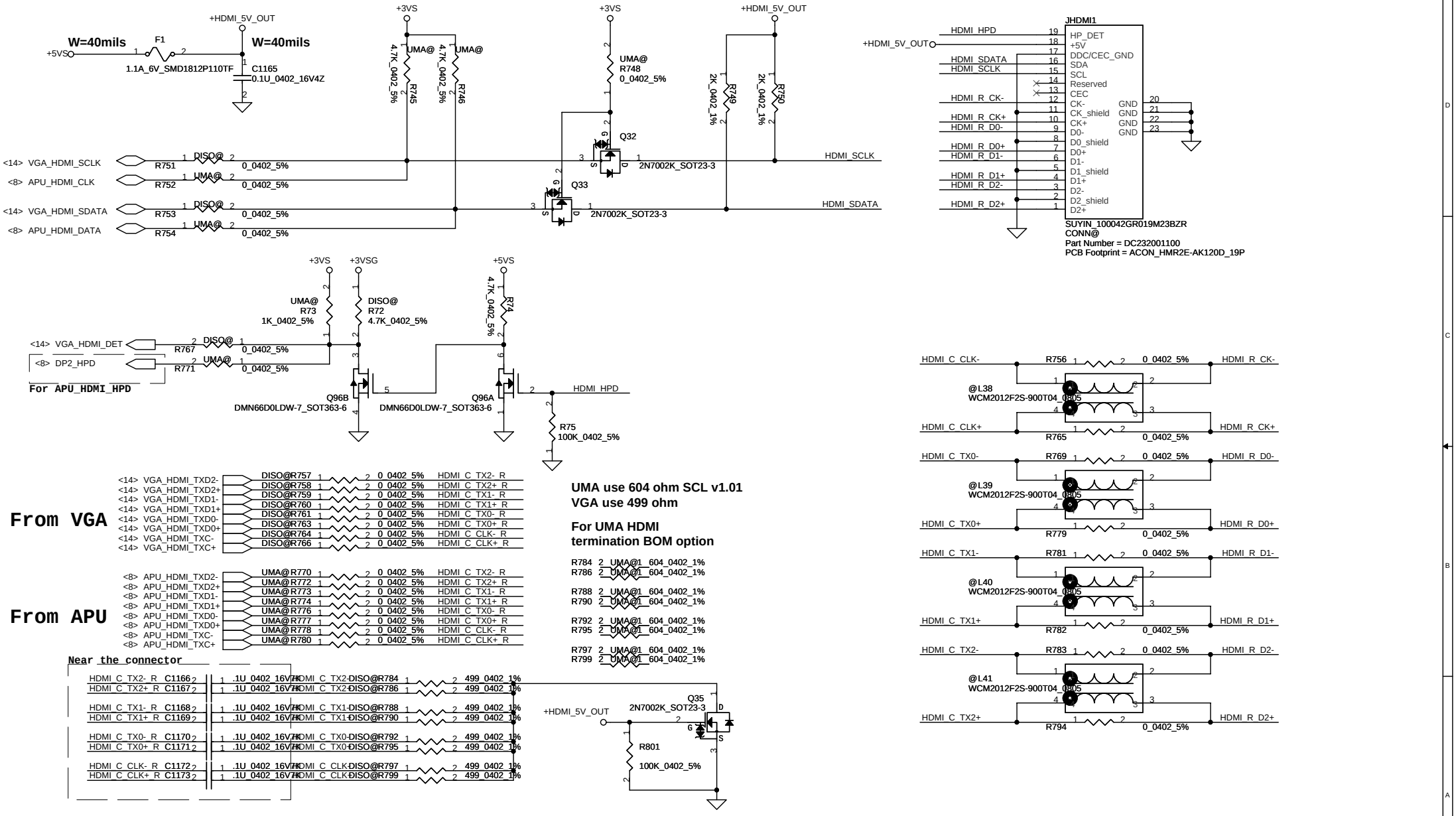

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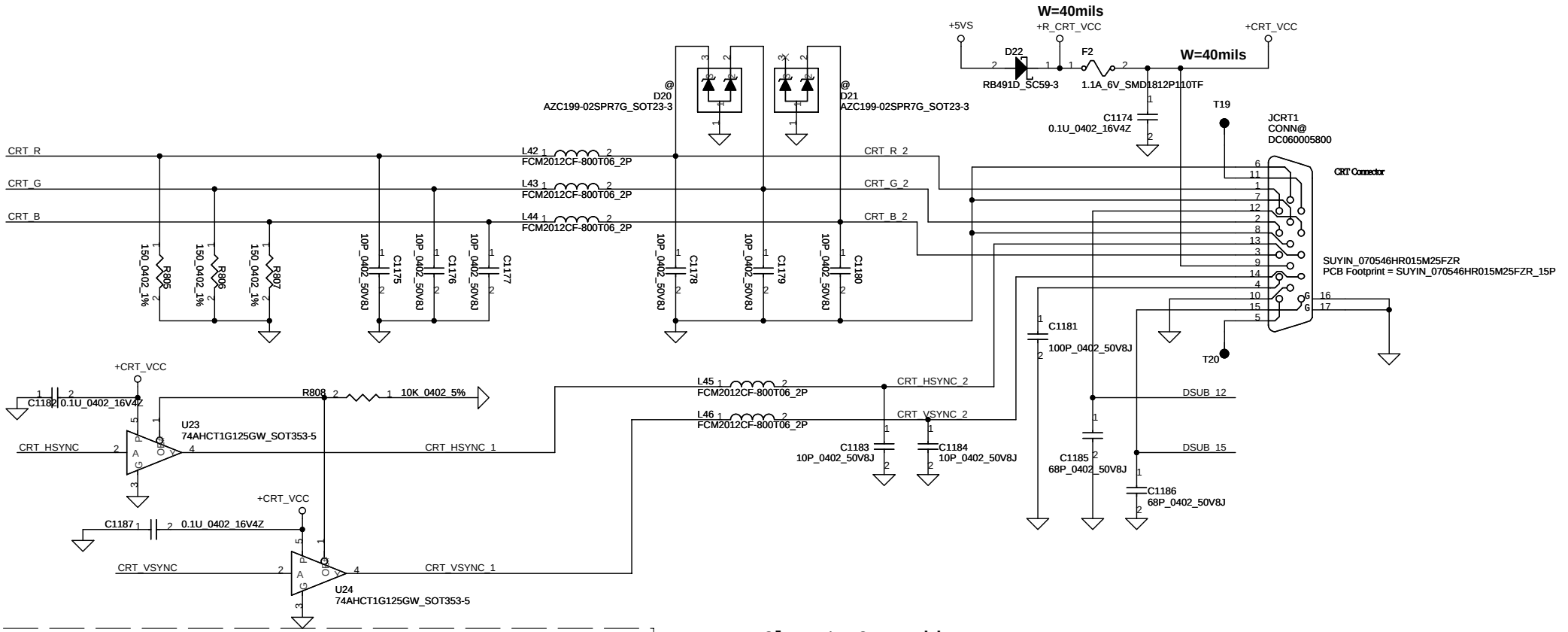


Use common via

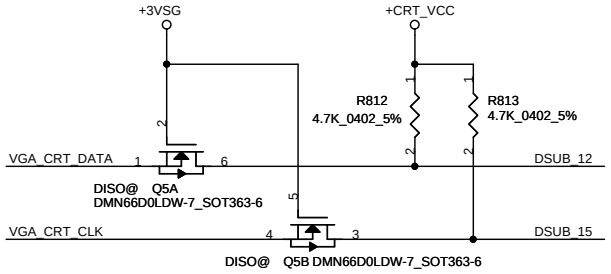
From FCH

<26> FCH_CRT_R	FCH_CRT_R	R809	UMA@	0_0402_5%	CRT_R
<26> FCH_CRT_G	FCH_CRT_G	R810	UMA@	0_0402_5%	CRT_G
<26> FCH_CRT_B	FCH_CRT_B	R811	UMA@	0_0402_5%	CRT_B
<26> FCH_CRT_HSYNC	FCH_CRT_HSYNC	R814	UMA@	0_0402_5%	CRT_HSYNC
<26> FCH_CRT_VSYNC	FCH_CRT_VSYNC	R815	UMA@	0_0402_5%	CRT_VSYNC
<26> FCH_CRT_DDC_SDA	FCH_CRT_DDC_SDA	R816	UMA@	0_0402_5%	DSUB_12
<26> FCH_CRT_DDC_SCL	FCH_CRT_DDC_SCL	R817	UMA@	0_0402_5%	DSUB_15

From VGA

<14> VGA_CRT_R	VGA_CRT_R	R818	DISO@	0_0402_5%	CRT_R
<14> VGA_CRT_G	VGA_CRT_G	R819	DISO@	0_0402_5%	CRT_G
<14> VGA_CRT_B	VGA_CRT_B	R820	DISO@	0_0402_5%	CRT_B
<14> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R821	DISO@	0_0402_5%	CRT_HSYNC
<14> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R822	DISO@	0_0402_5%	CRT_VSYNC
<14> VGA_CRT_DATA	VGA_CRT_DATA				
<14> VGA_CRT_CLK	VGA_CRT_CLK				

Close to Conn side



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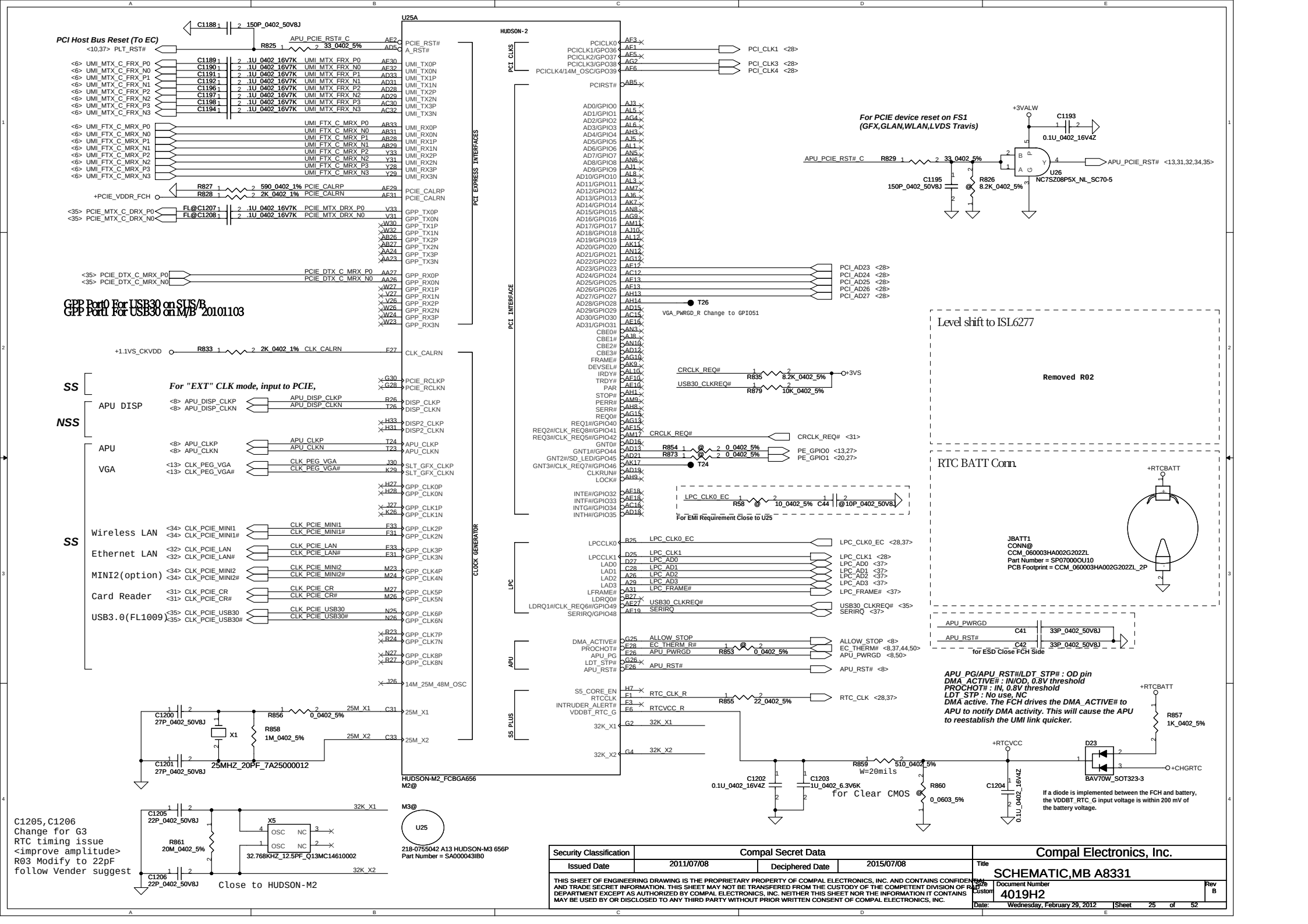

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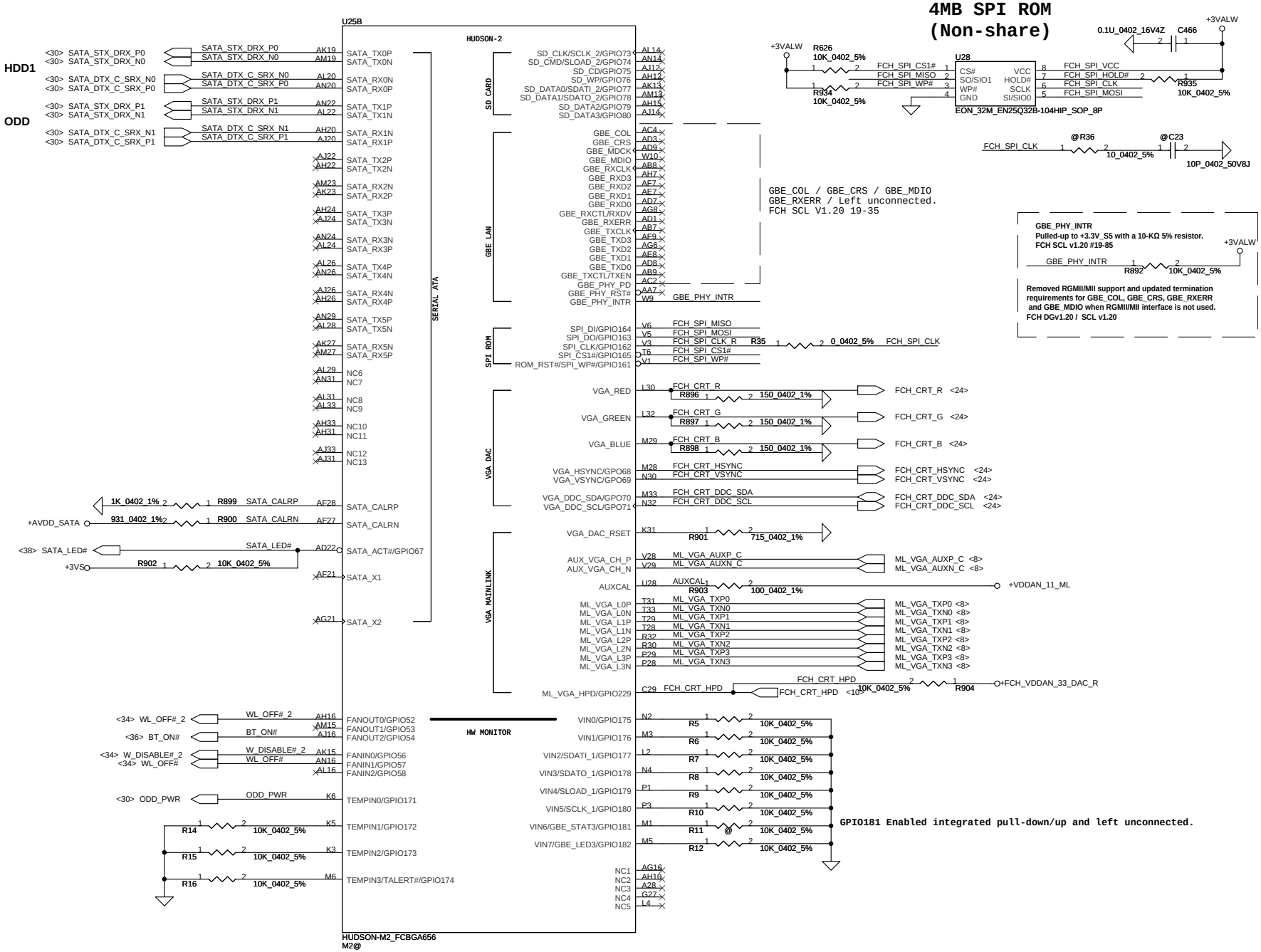

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FCH_PCIE_RST# IS FOR PCIE
DEVICES ON Hudson-M2/M3

FL@ C1211 150P_0402_50V8J

R03 modify
Update BOM Structure

HUDSON-2

U25D

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage

R03 modify for TP 6P/8P

R03 modify for Resverd

R03 modify remove D44/D45

33ohm termination resistor at CODEC side

For FCH internal debug use

R03 modify

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

Hudson-M2/M3 OHCI CTL DEV 20, Fn 5 <Disable CTL>

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>

Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

30 Pin Sub board USB3.0 Conn

On board USB Conn

Mini2-Option

Hudson-M2/M3 EHCI CTL DEV 19, Fn 2

Mini1-WLAN

BT

Camera

Hudson-M2/M3 EHCI CTL DEV 18, Fn 2 <Support Wakeup>

For Right Side USB2.0 Port

Project SKU ID	Value	
GPIO189 (use VGA)	Low (UMA)	High (VGA)
GPIO190 (use PX)	Low (noPX)	High (PX)
GPIO188 (USB2/3)	High (2.0)	Low (3.0)
GPIO187 (LVDS/eDP)	Low (LVDS)	High (eDP)
GPIO166 (Resverd)		

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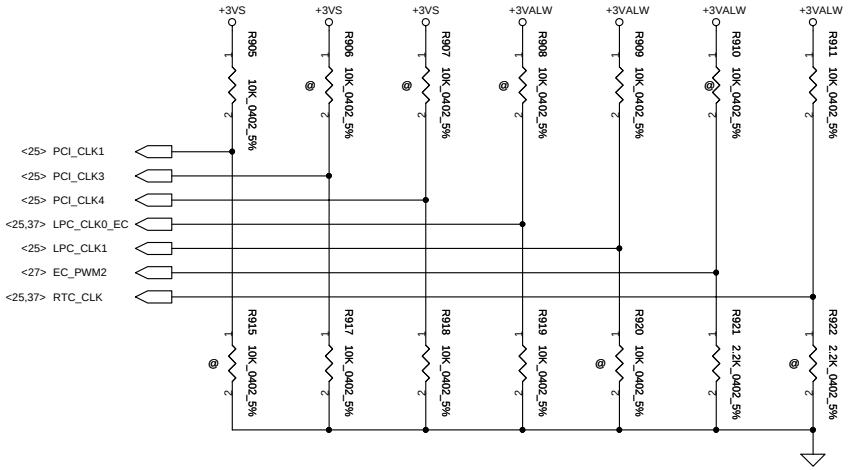
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

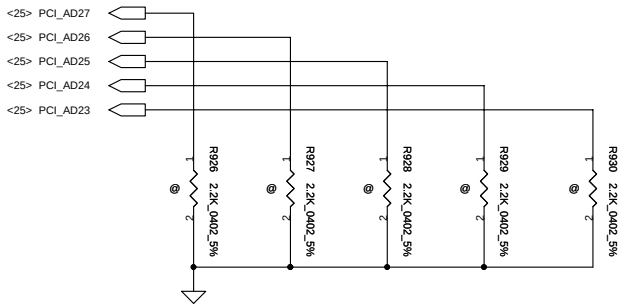


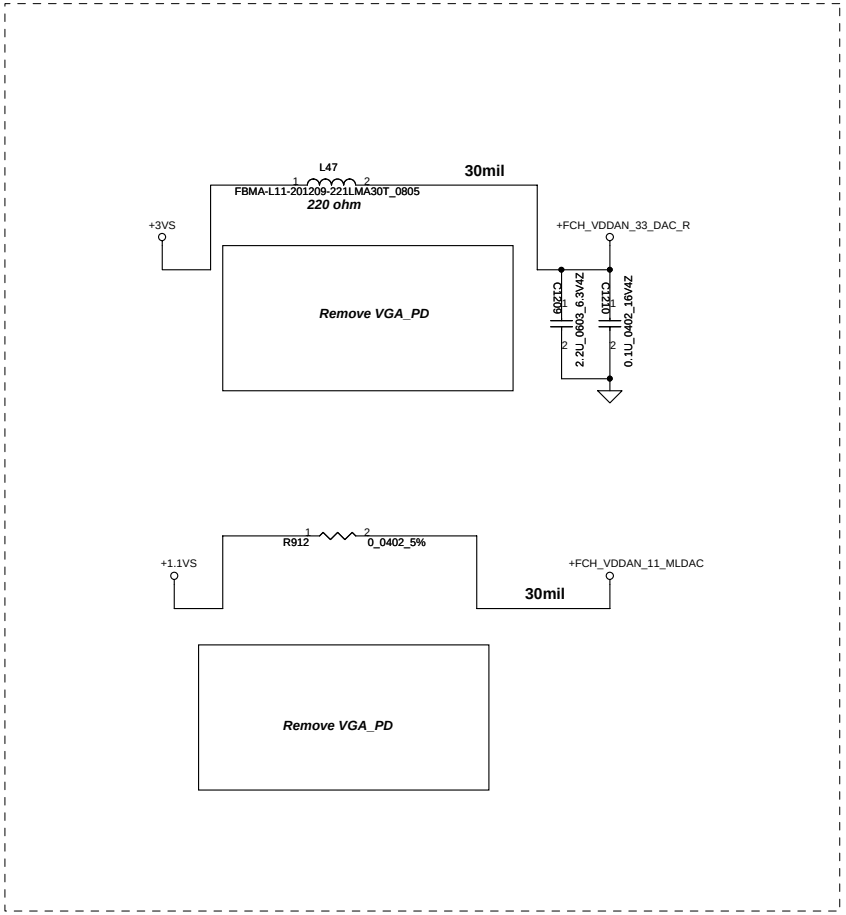
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26

	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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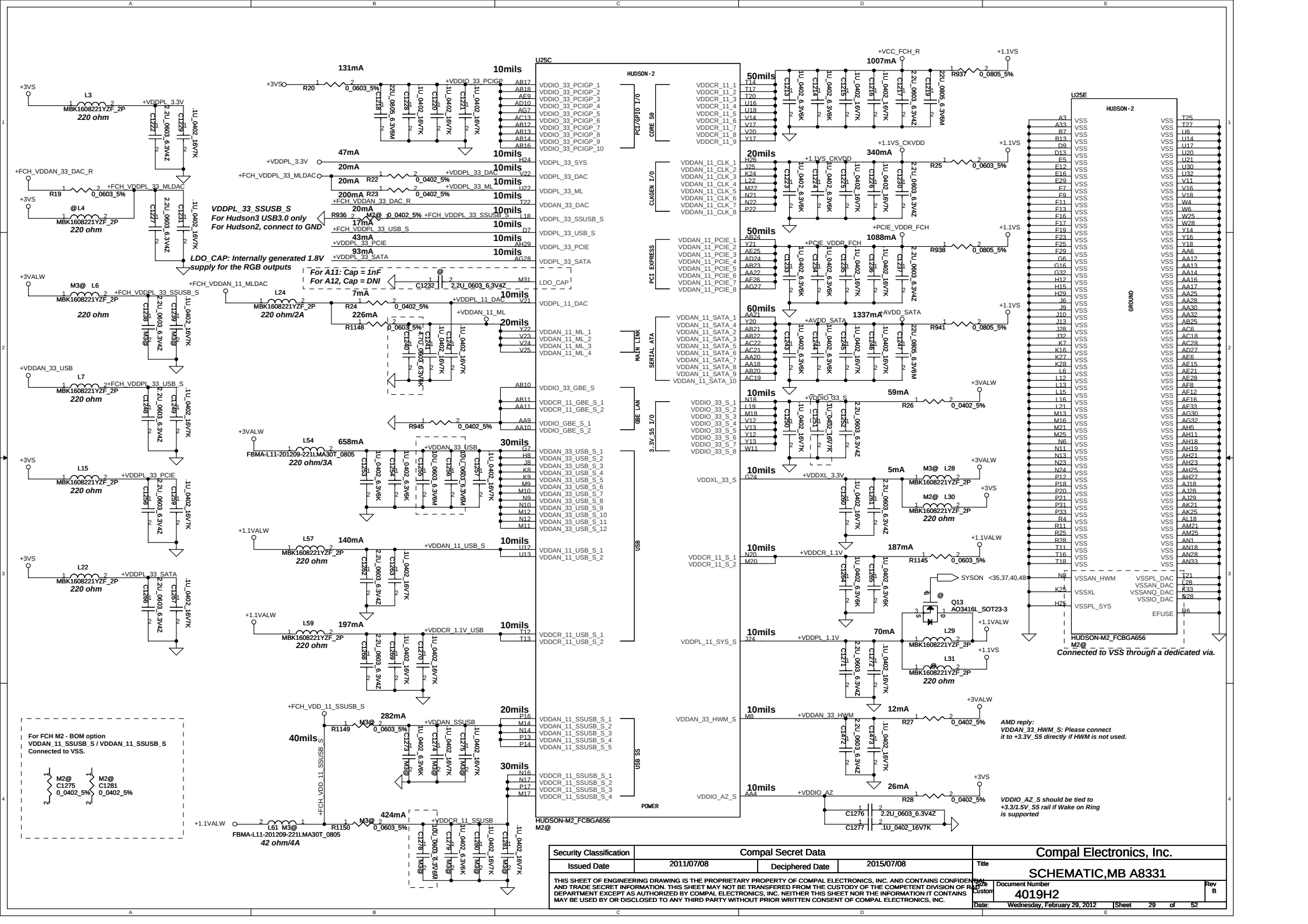

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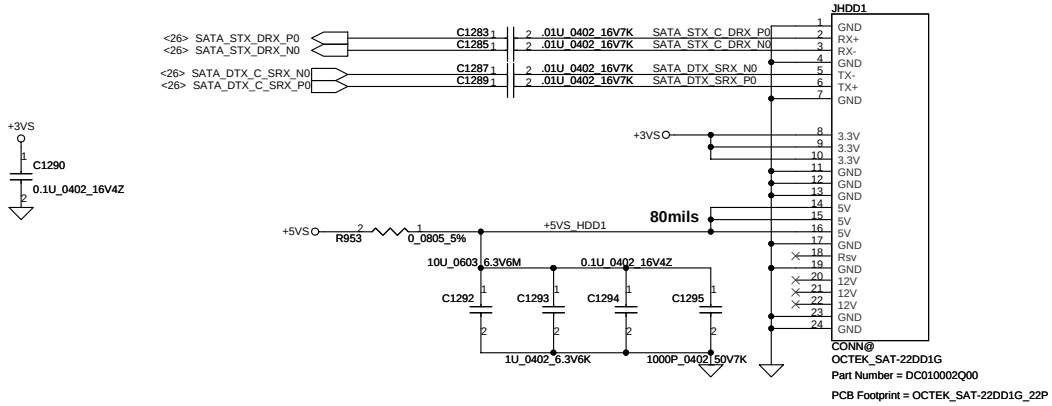
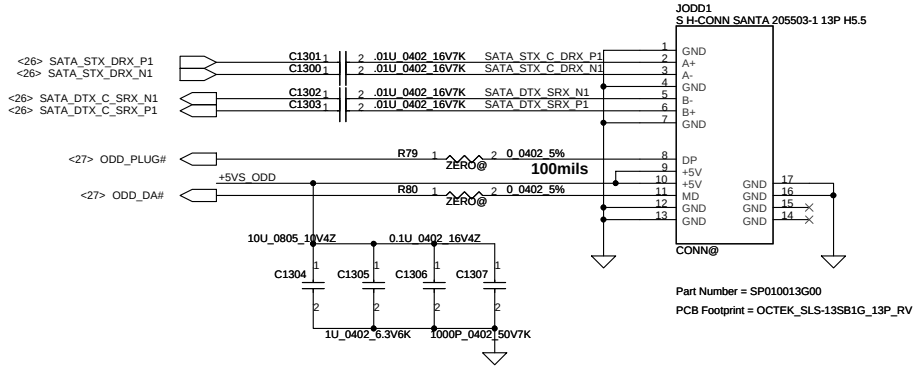
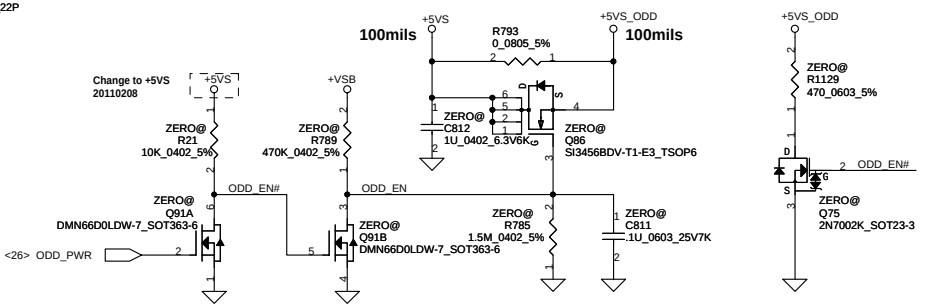
SATA HDD1 Conn.

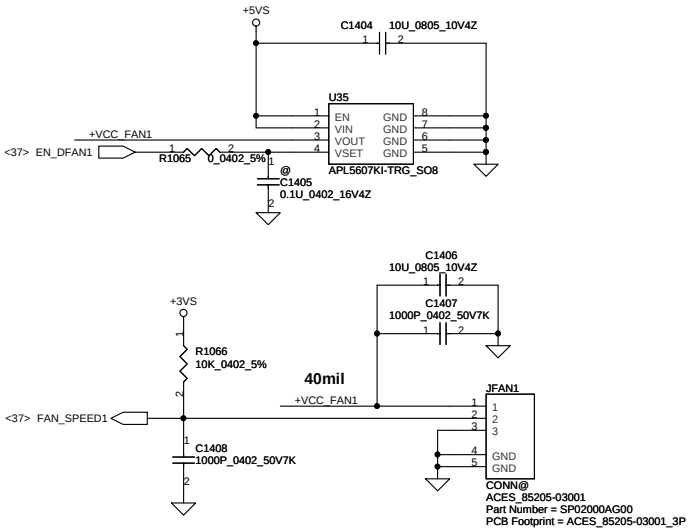


SATA ODD Conn.





FAN



Screw Hole Follow P5WE0

FAN Stand-Off

H1 H_3P4
H2 H_3P4
H3 H_3P4
H7 H_3P4
H8 H_3P0
H9 H_3P0
H10 H_3P0
H11 H_3P0
H13 H_3P0
H14 H_3P0
H15 H_3P0
H16 H_3P0
H17 H_3P0
H18 H_3P0
H28 H_3P0
H19 H_4P0
H20 H_4P0
H21 H_4P2
H22 H_4P2
H23 H_4P2
H24 H_4P2

For Layout request
Delete H25
20110419

H26 H_3P0N
H27 H_3P5X3P0N
H29 H_3P5N
R03 Add

FD1 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

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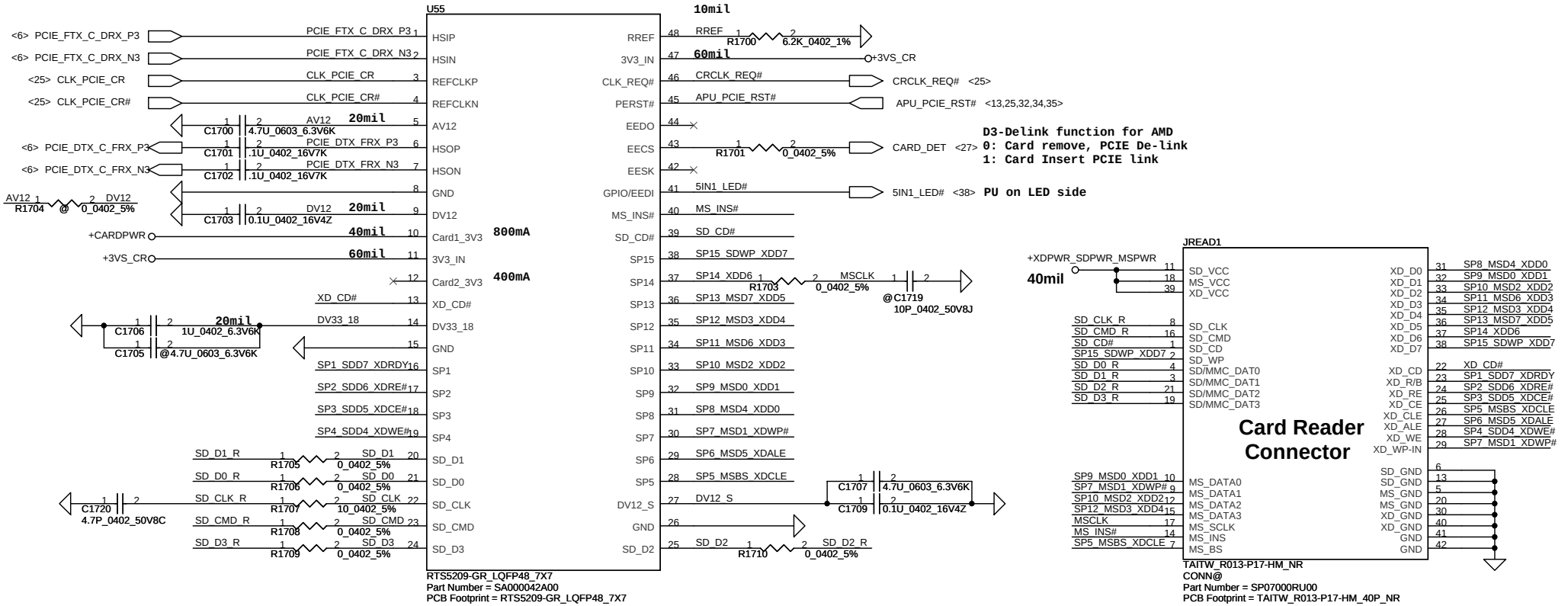

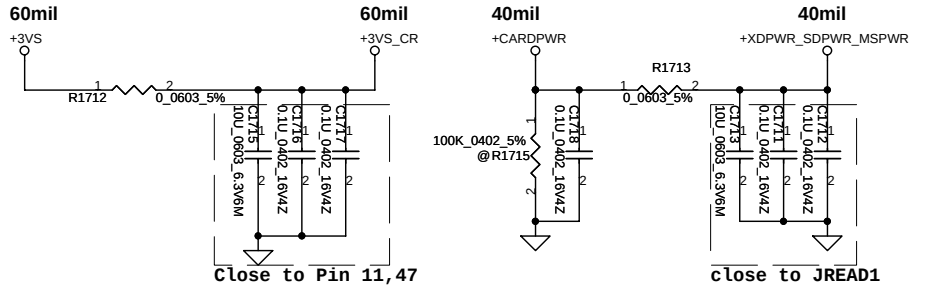

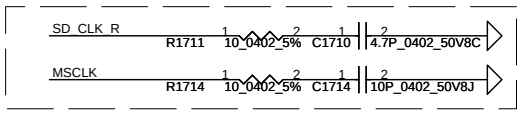

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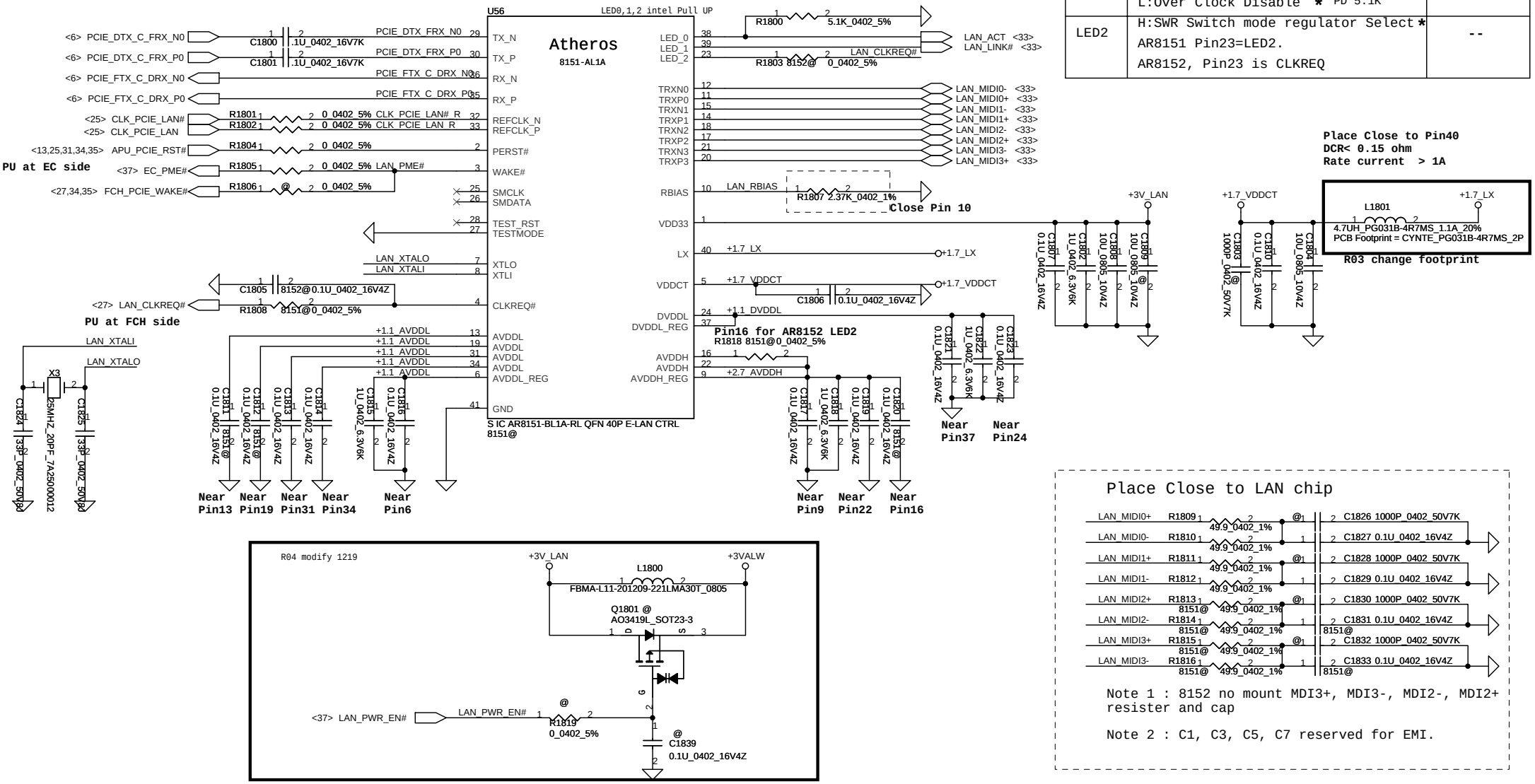
Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable * PD 5.1K	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--



Place Close to LAN chip

Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resister and cap

Note 2 : C1, C3, C5, C7 reserved for EMI.

	Pin4	Configure R1808	Configure C1805		Pin23	Configure R1803
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

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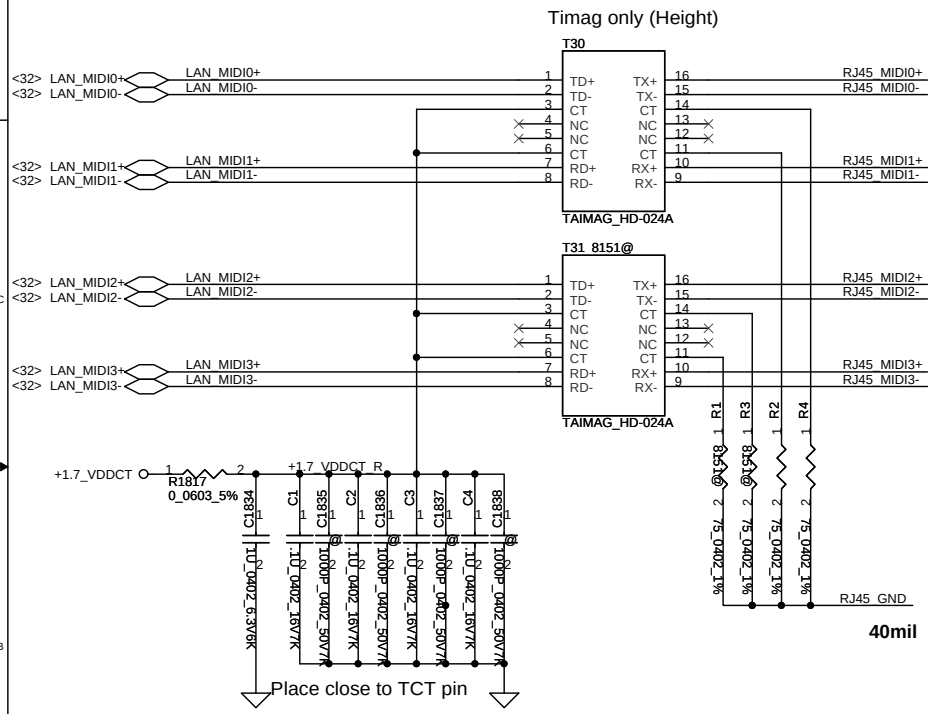
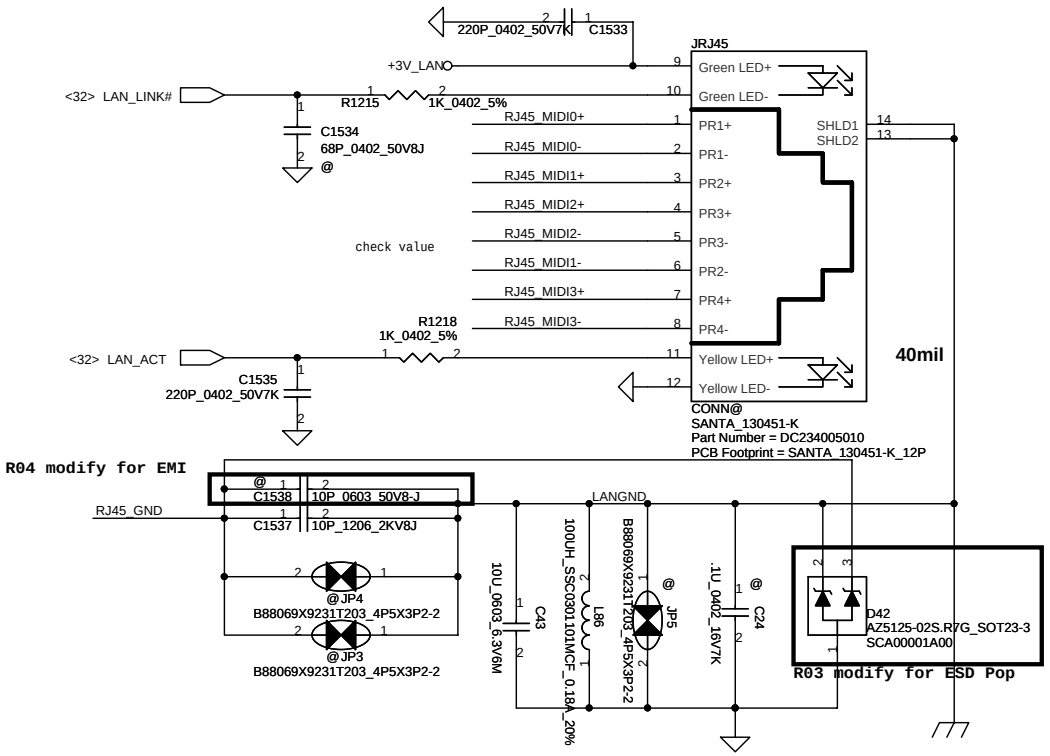
LAN Connector





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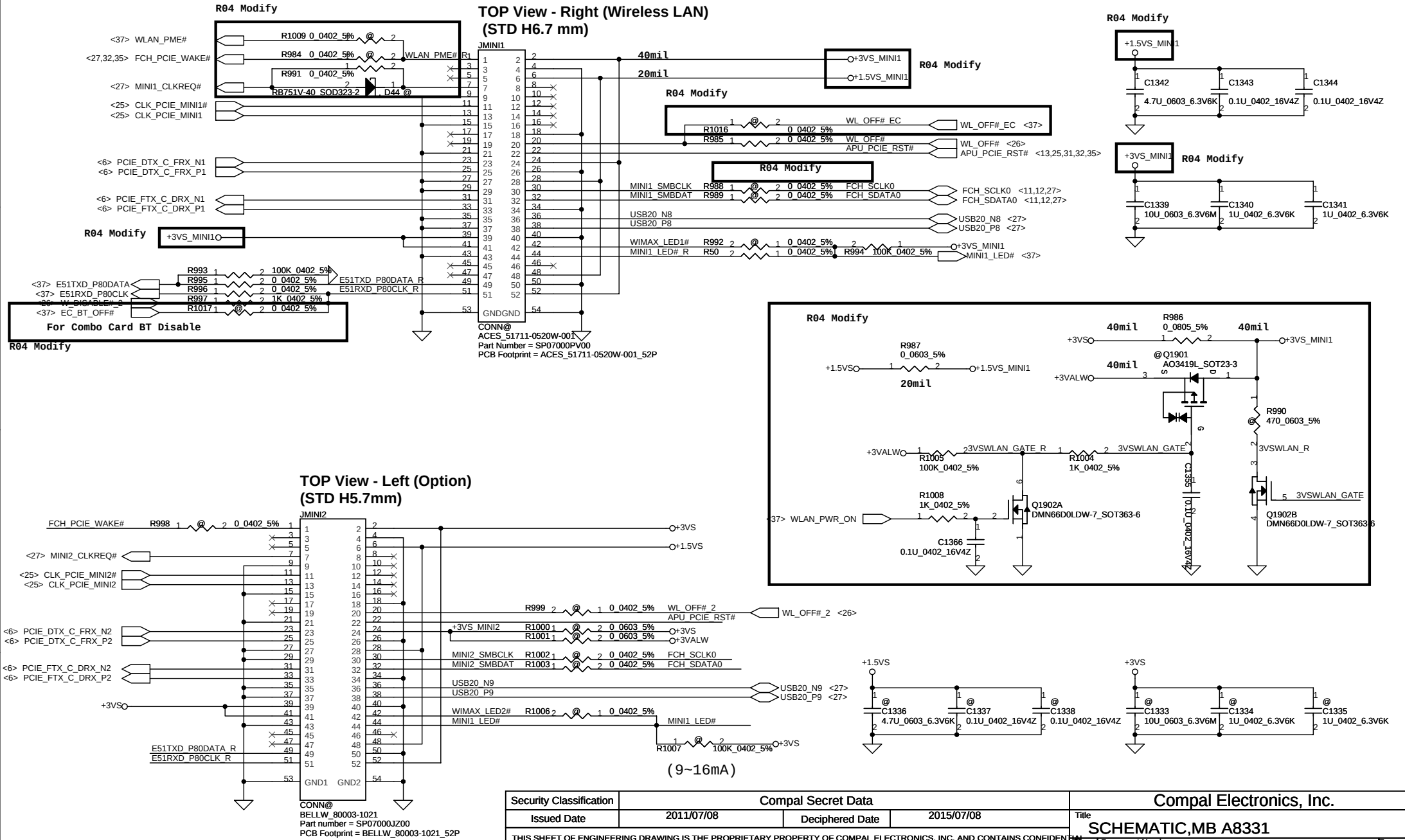

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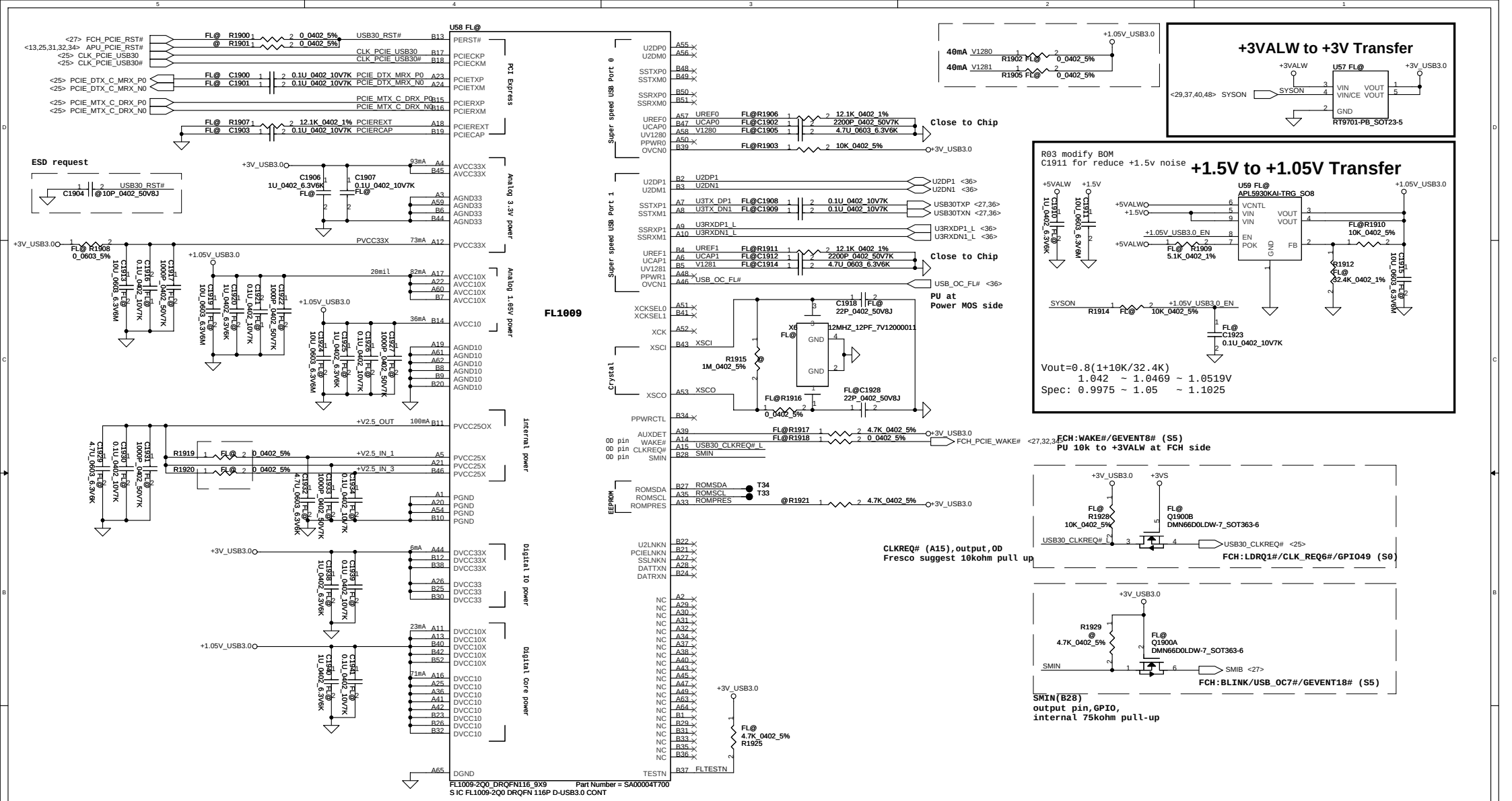

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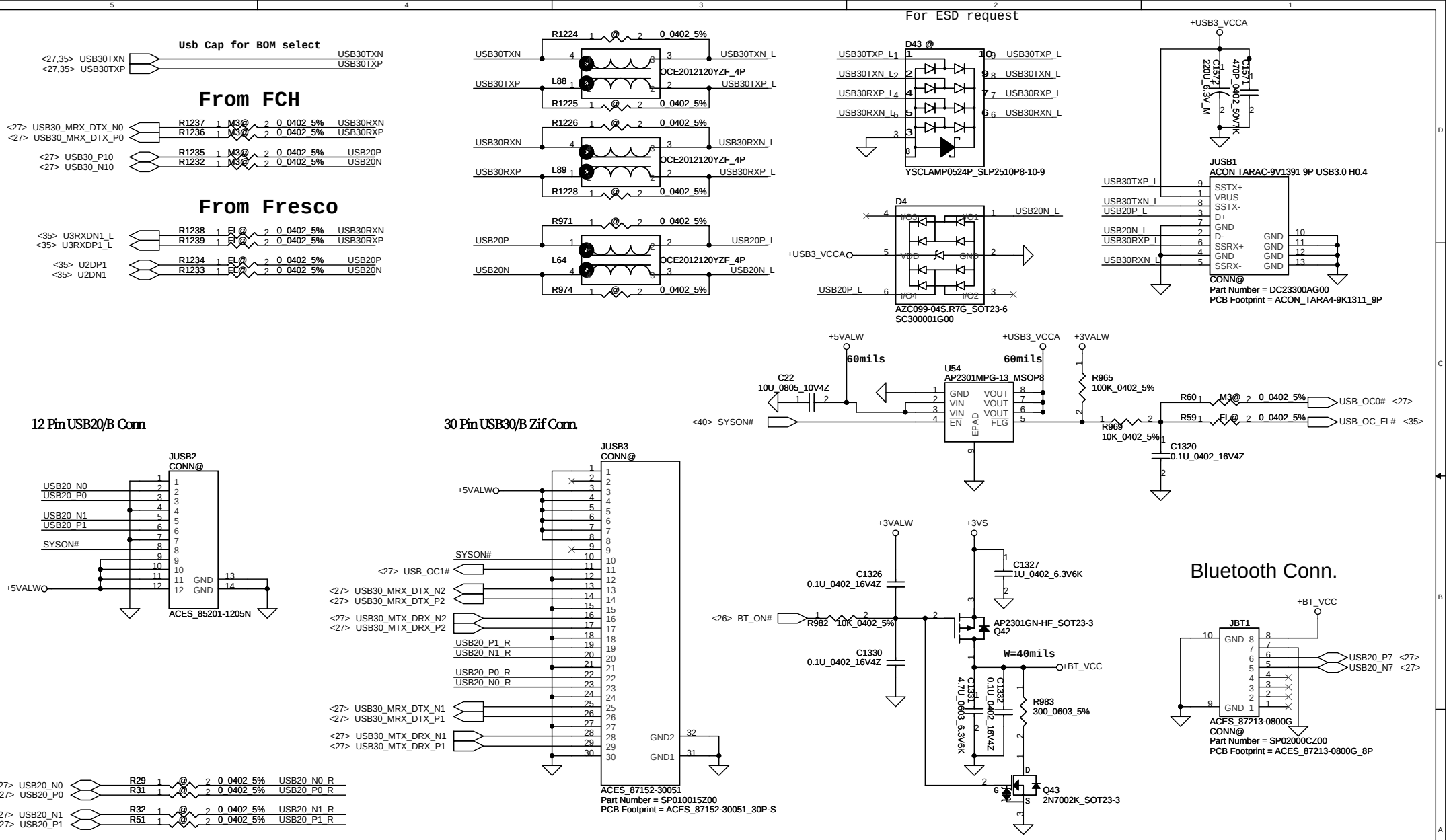

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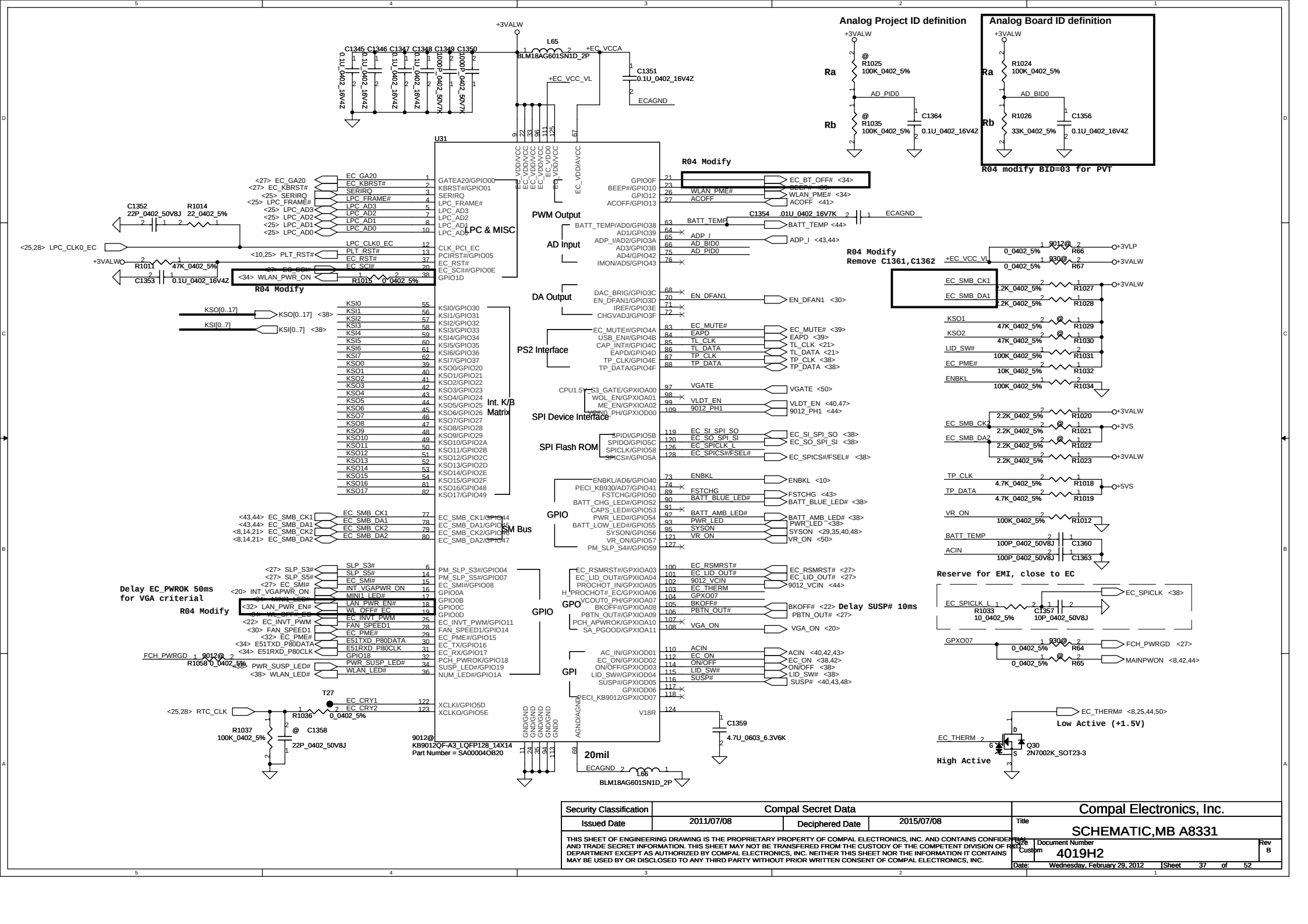

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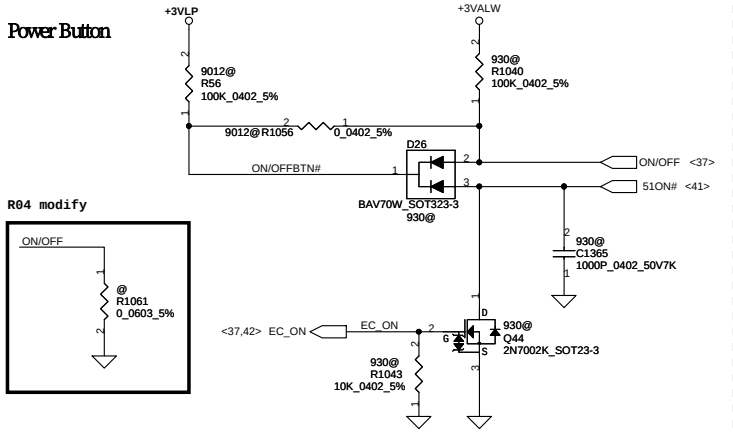
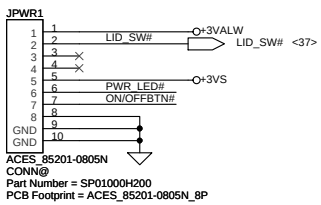
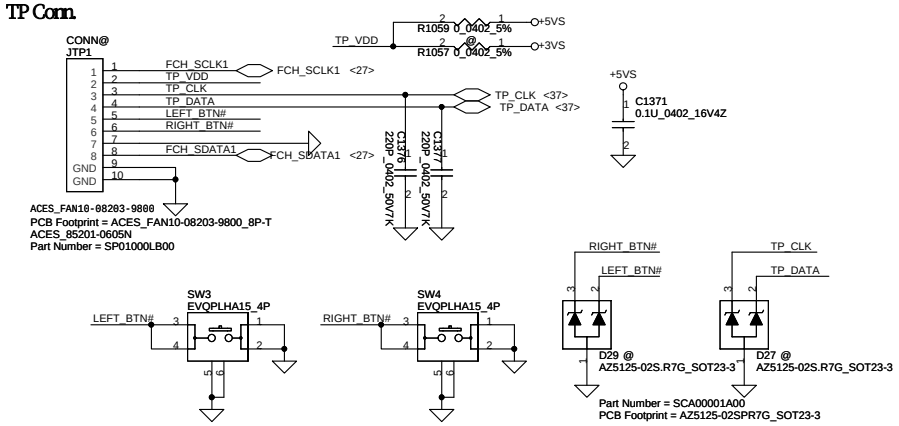
Power Button



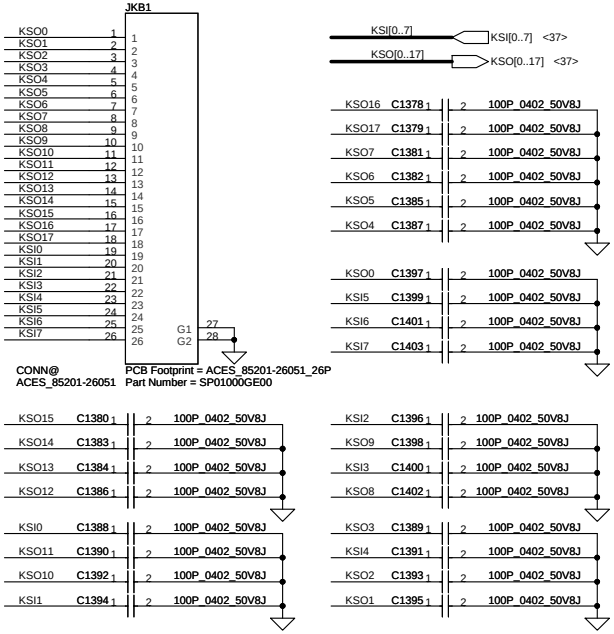
POWER/B



TP Conn.



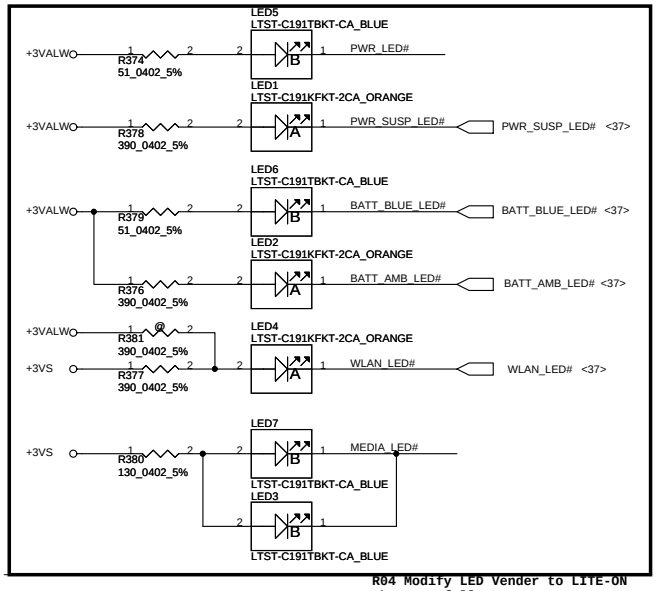
KB Conn.



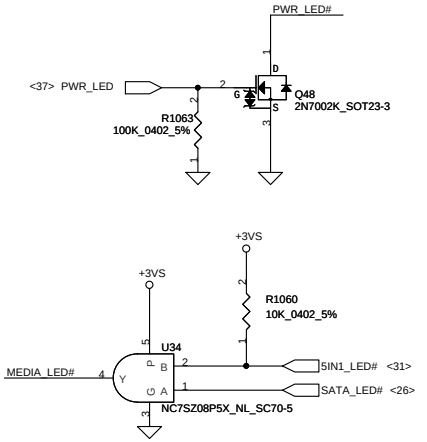
LED

LED Status	Power/SUS		Battery		3G / WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber		Amber		

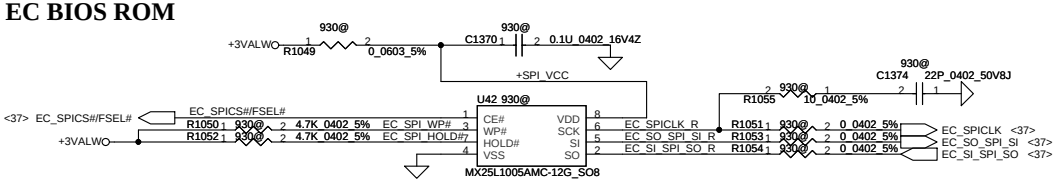
removed



R04 Modify LED Vender to LITE-ON
Change R follow Q5WVH



EC BIOS ROM



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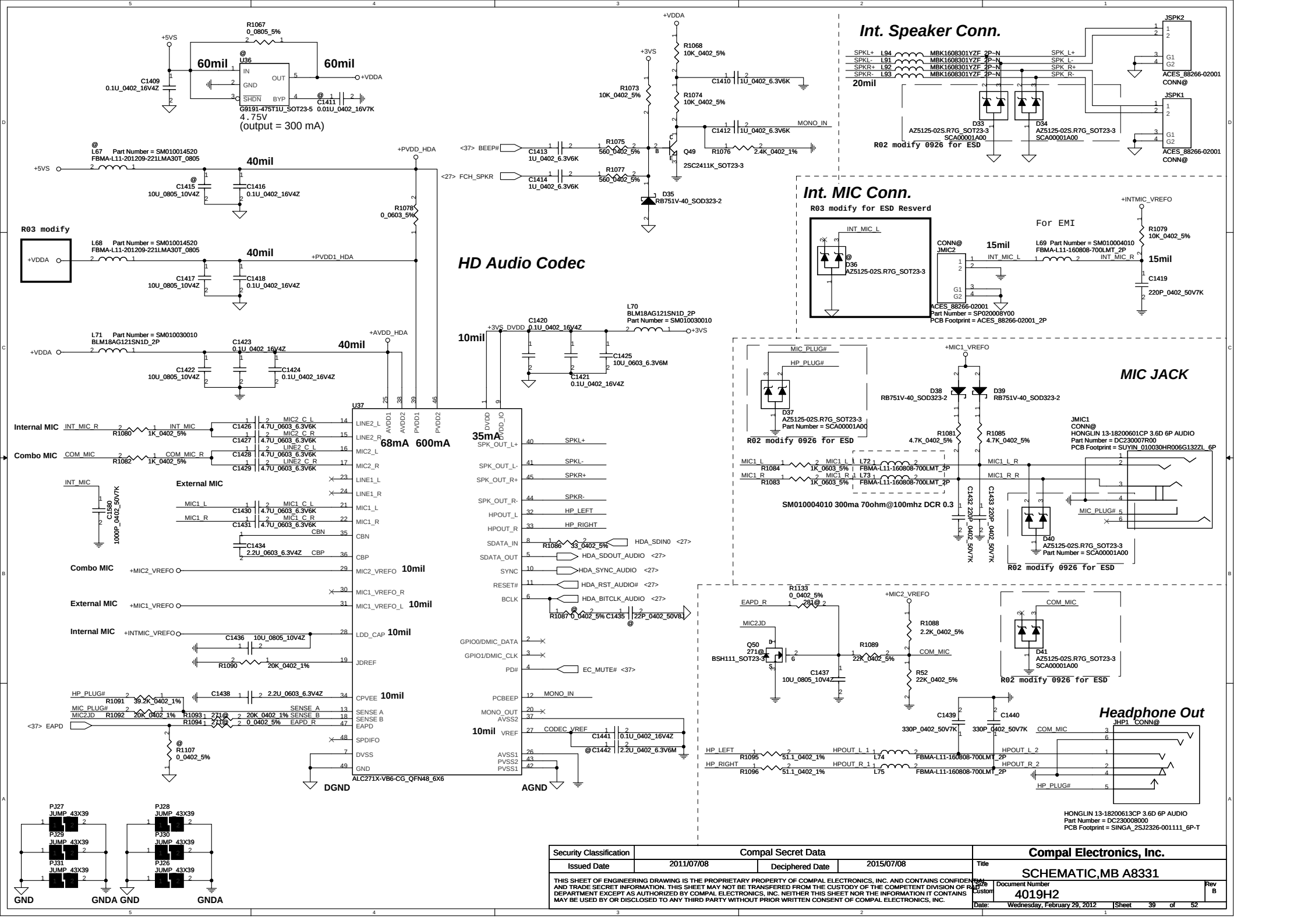

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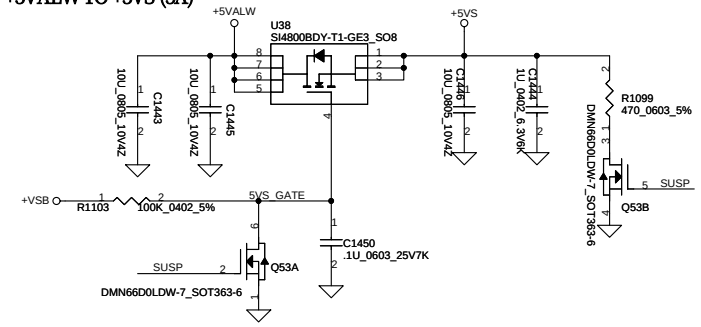
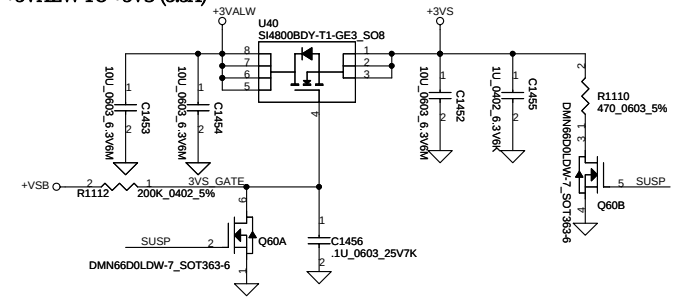
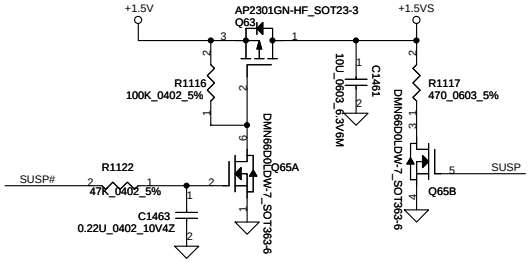
+5VALW TO +5VS (5A)

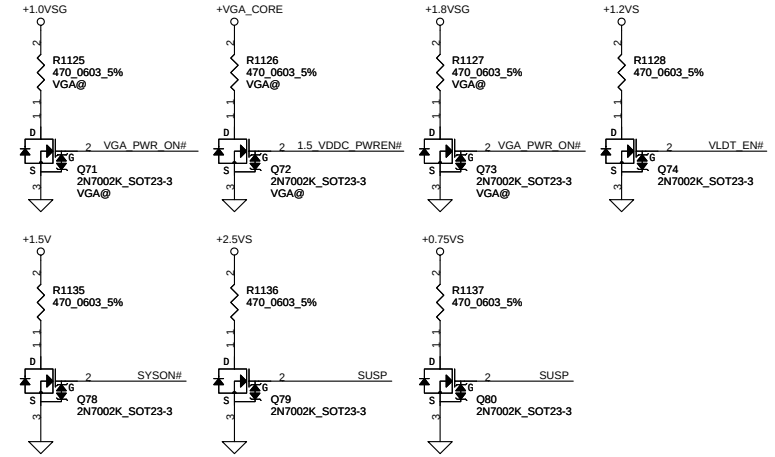


+3VALW TO +3VS (3.3A)

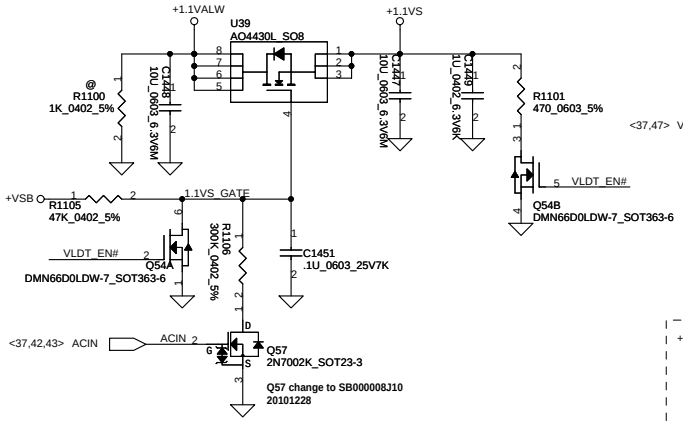


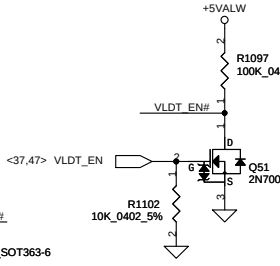
+1.5V TO +1.5VS (1.5A)

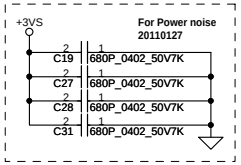


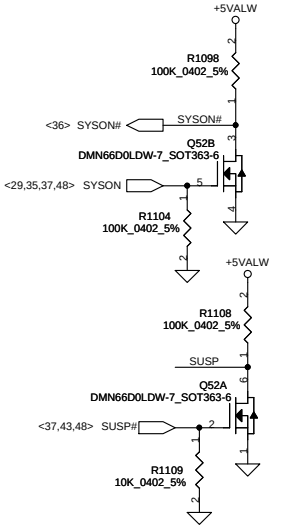


+1.1VALW TO +1.1VS (1.1A)

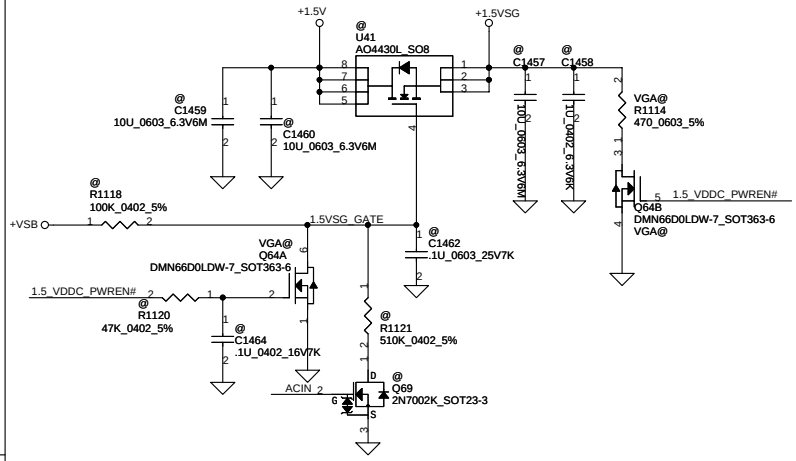


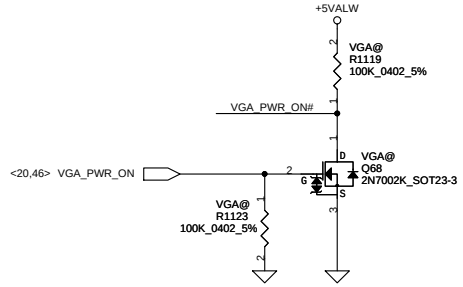


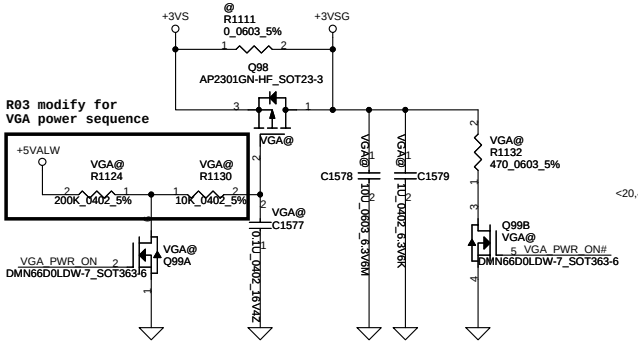


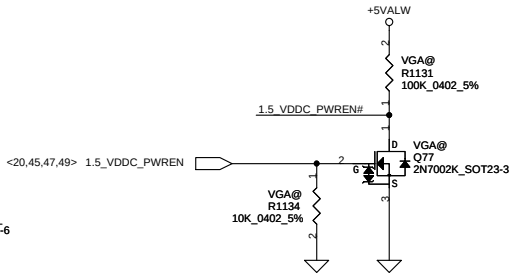


VGA Power *+1.5V to +1.5VSG (1.5A)*









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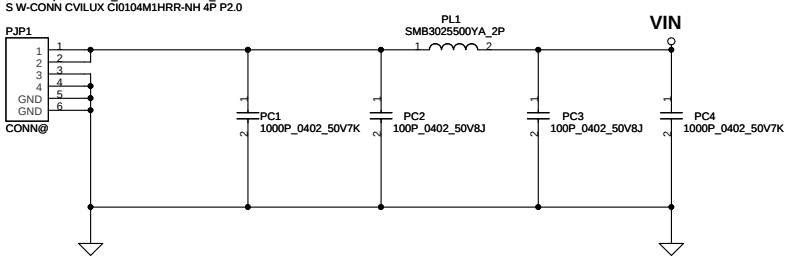
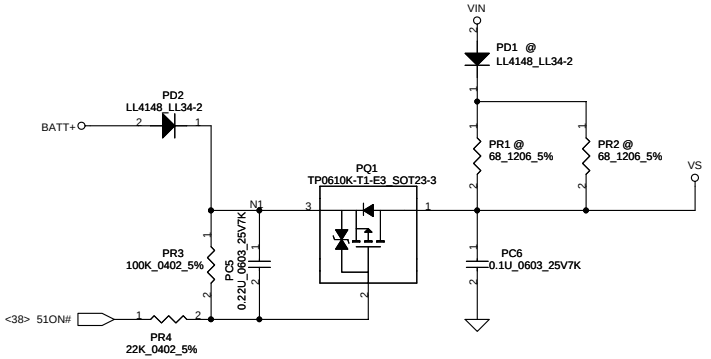
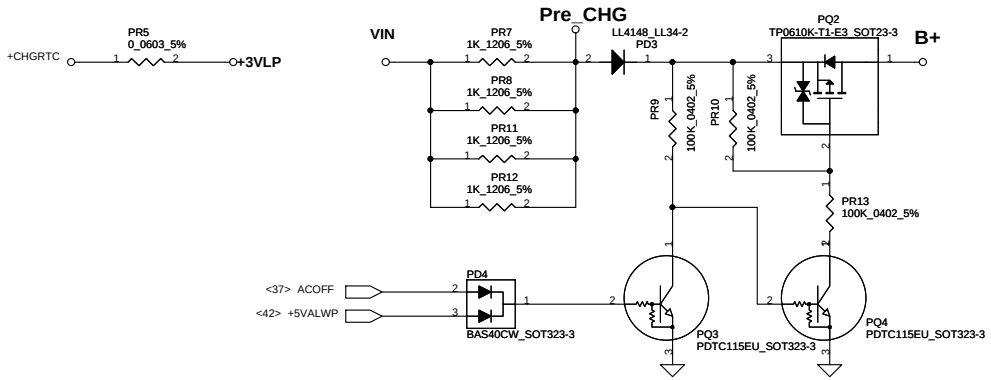
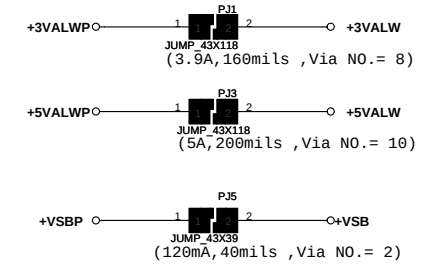
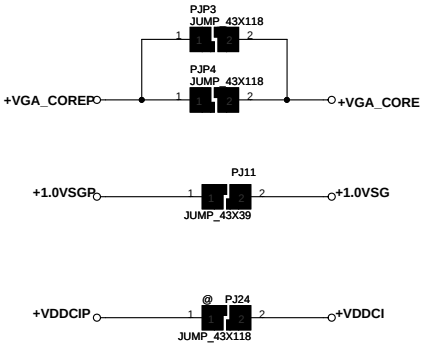
Part Number = SP02000VQ00
PCB Footprint = LIYO_309001-04301-031_4P
S W-CONN CVILUX CI0104M1HRR-NH 4P P2.0

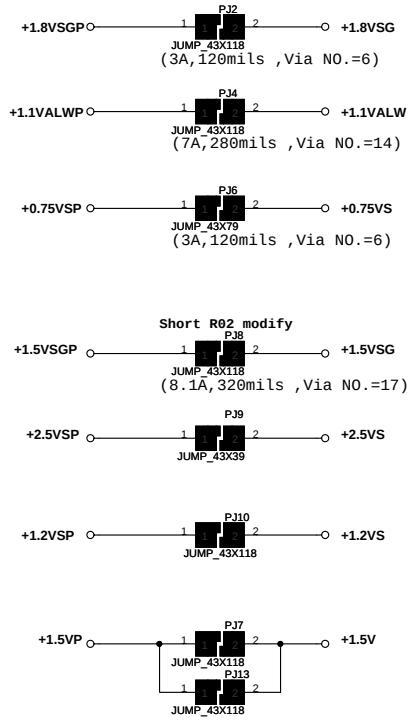












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Compal Electronics, Inc.

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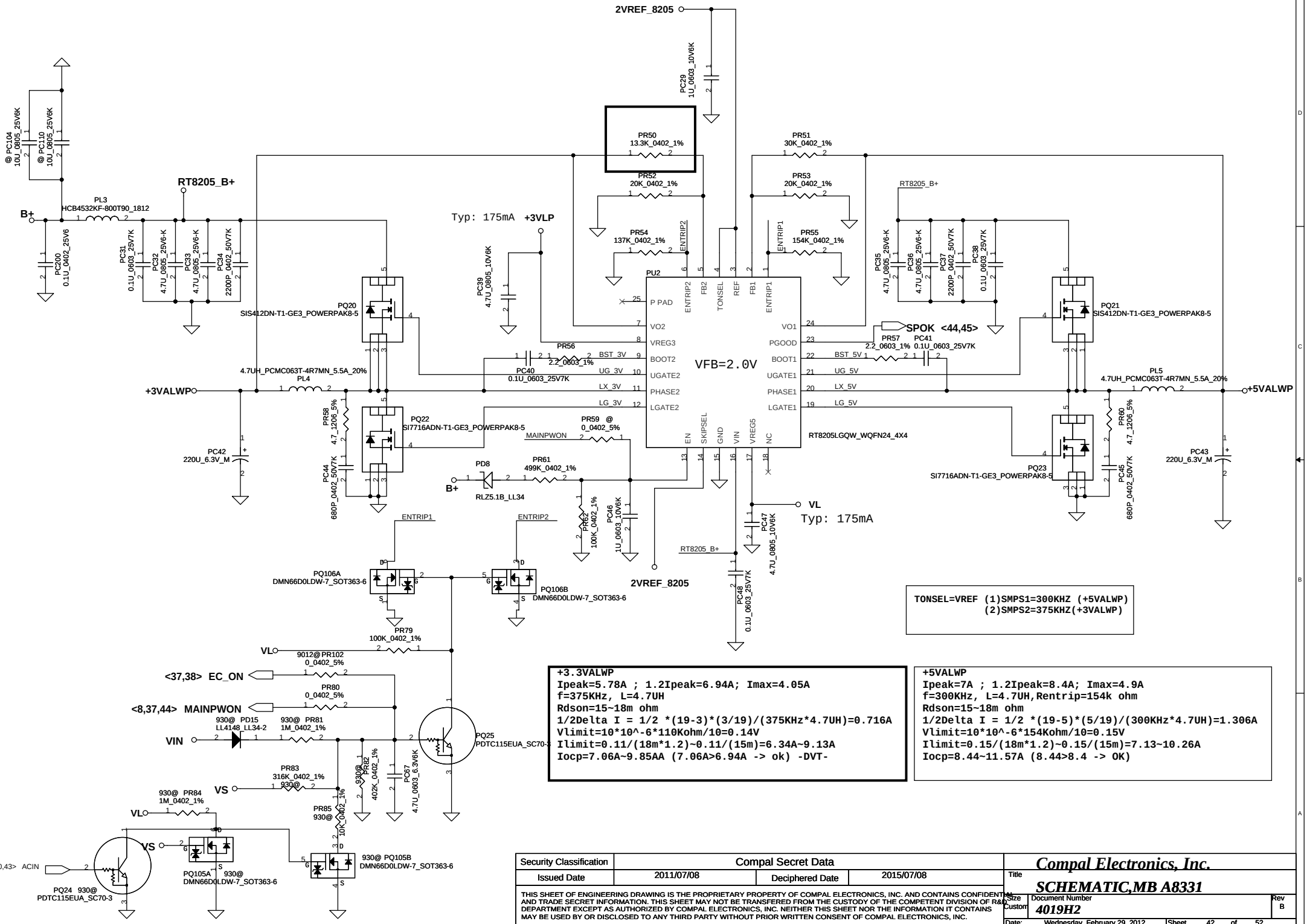

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Compal Electronics, Inc.			
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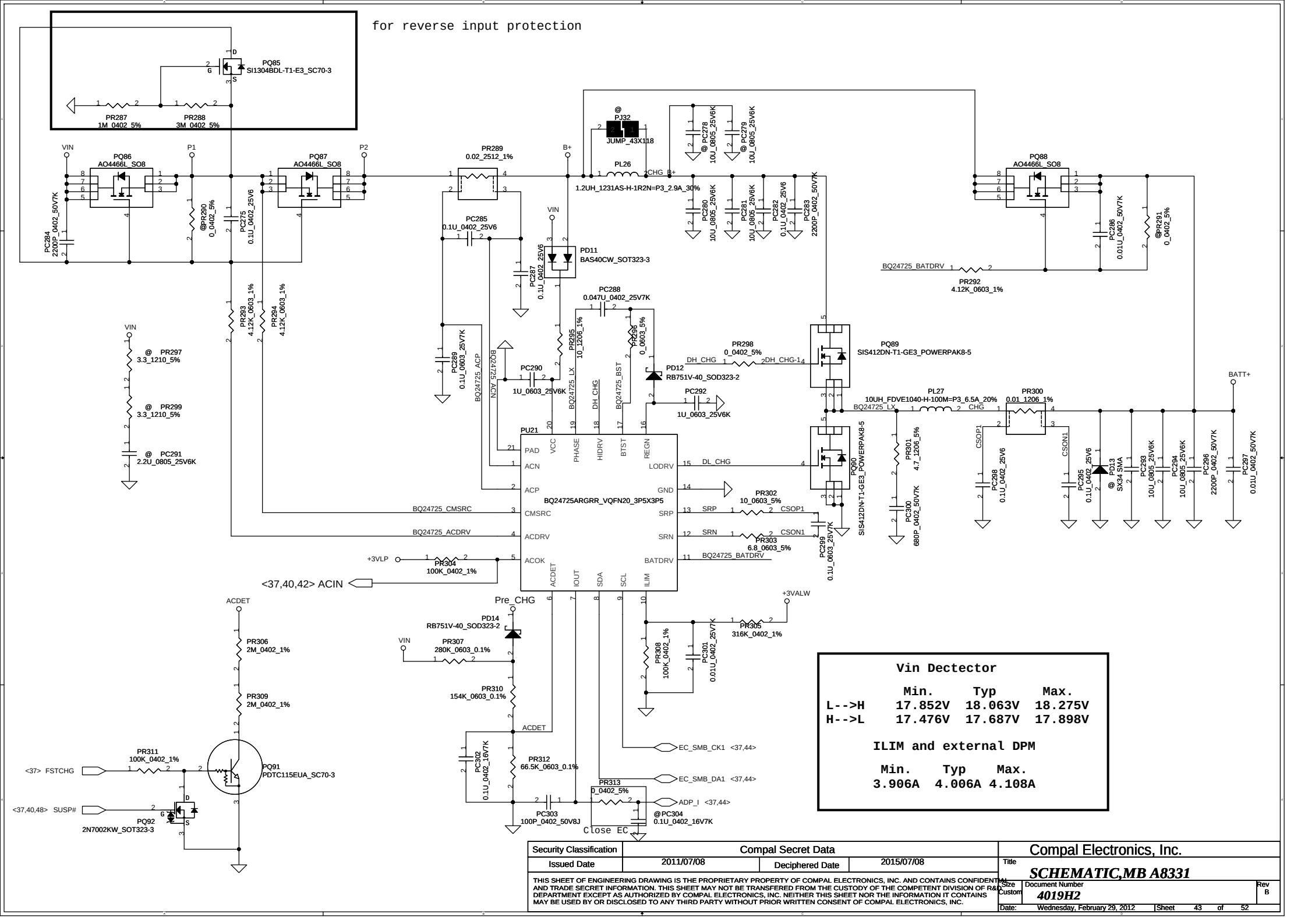

Vin Dectector

	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

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Part Number = DC040008G00
PCB Footprint = SUYIN_200275GR008G13GZR_8P-T

PJP2
SUYIN_200275GR008G16BZR 8P

CONN@

EC_SMDA
EC_SMCA
TH
PI

<40,41>
VMB

PL19
SMB3025500YA_2P

<40,41>
BATT+

PC234
1000P_0402_50V7K

PC235
0.01U_0402_25V7K

PR252
1K_0402_5%

PR250
100_0402_1%

PR251
100_0402_1%

EC_SMB_DA1 <37,43>

EC_SMB_CK1 <37,43>

PR255
6.49K_0402_1%

+3VALWP

PR258
1K_0402_1%

BATT_TEMP <37>

PH1 under CPU botten side :
CPU thermal protection at 92 +/- 3 degree C

+3VLP

PC233
0.1U_0603_25V7K

+3VLP

@PR256
100K_0402_1%

<8,37,42> MAINPWON

<8,25,37,50> EC_THERM#

+3VLP

PR257
100K_0402_1%

PQ65
2N7002W-T/R7_SOT323-3

PU17
VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2
G718TM1U_SOT23-8

PR254
21K_0402_1%

PR259
9.53K_0402_1%

PH1
100K_0402_1%_NCP15WF104F03RC

ADP_I <37,43>

UMA@PR34
3.92K_0402_1%

+3VLP

VGA@PR34
8.87K_0402_1%

PR267 @
100K_0402_1%

9012_PH1 <37>

PR266
0_0402_5%

9012_VCIN <37>

VGA@PR36
16.2K_0402_1%

UMA@PR36
10.5K_0402_1%

PR261
0_0402_5%

PR253 @
100K_0402_1%

PR38
10K_0402_1%

PQ77
TP0610K-T1-E3_SOT23-3

B+

+VSBP

PR260
100K_0402_1%

@PC236
0.22U_0603_25V7K

PC237
0.1U_0603_25V7K

PR263
22K_0402_1%

VL

PR264
100K_0402_1%

PR265
1K_0402_5%

<42,45> SPOK

PQ78
2N7002W-T/R7_SOT323-3

PC238
1U_0402_6.3V6K

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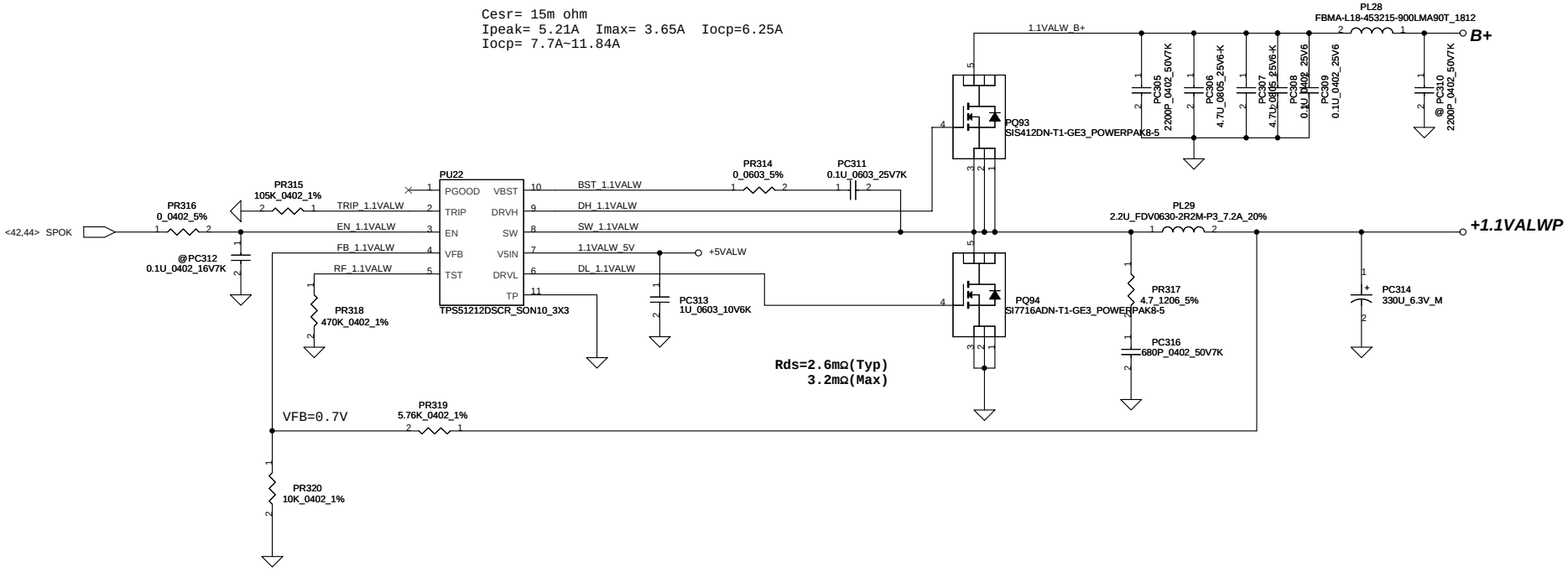
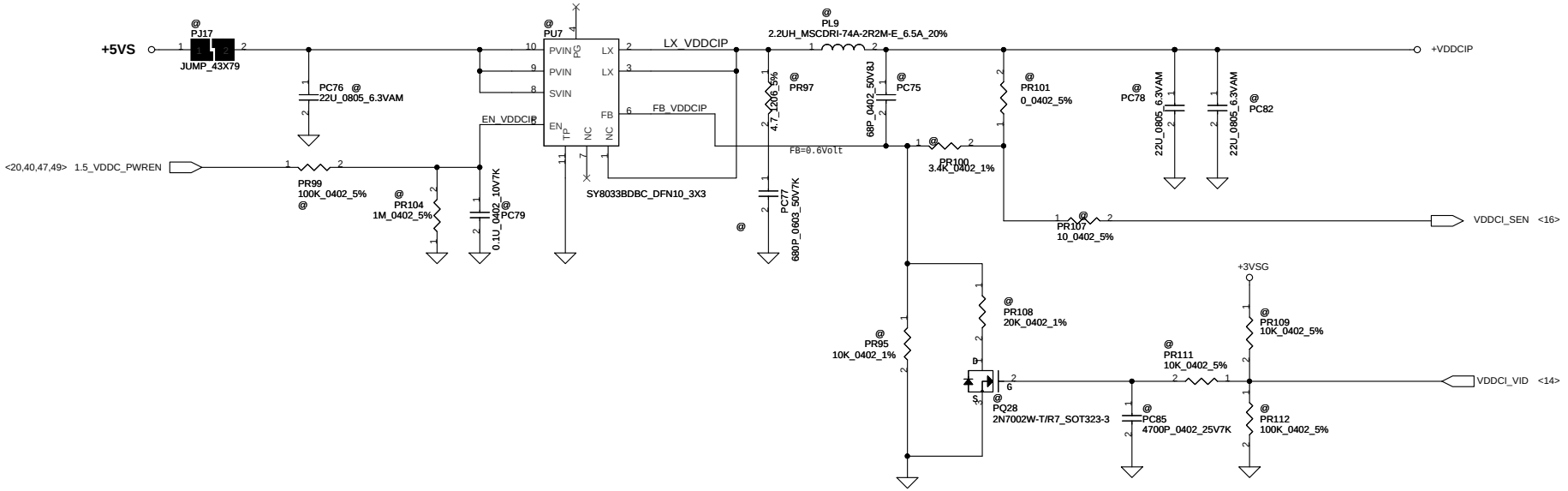
VFB= 0.7V
Vo=VFB*(1+5.76K/10K)= 1.1V
Freq= 266~314KHz , 290KHz(typ)

Cesr= 15m ohm
Ipeak= 5.21A Imax= 3.65A Iocp=6.25A
Iocp= 7.7A~11.84A





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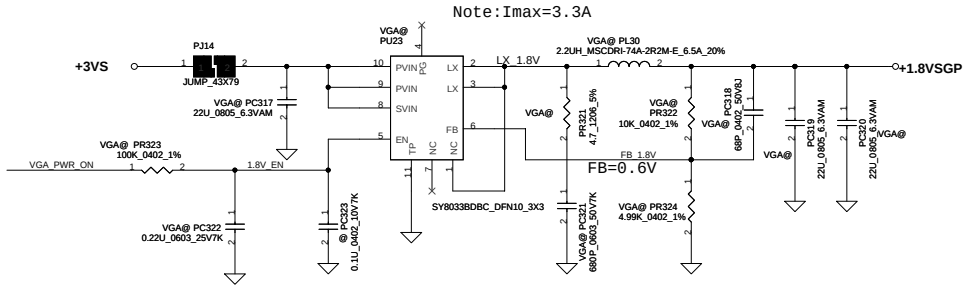

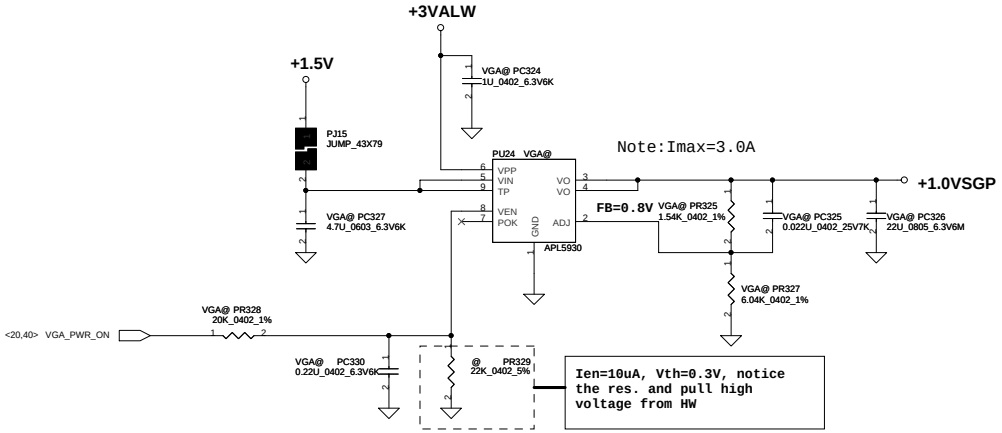

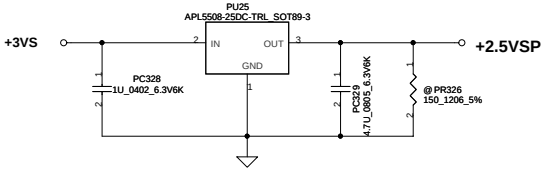

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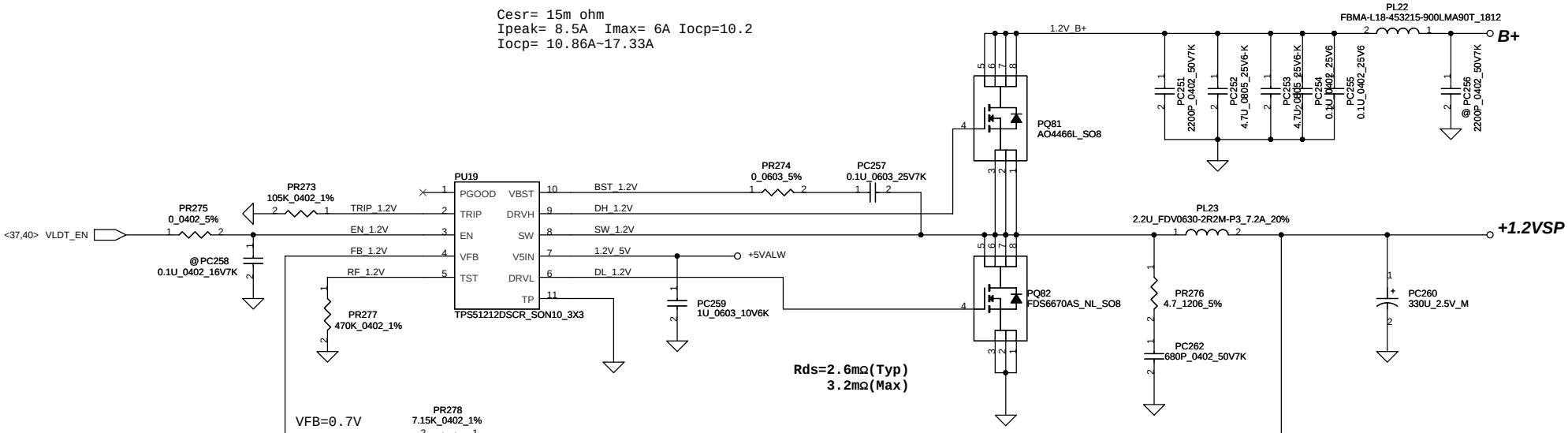
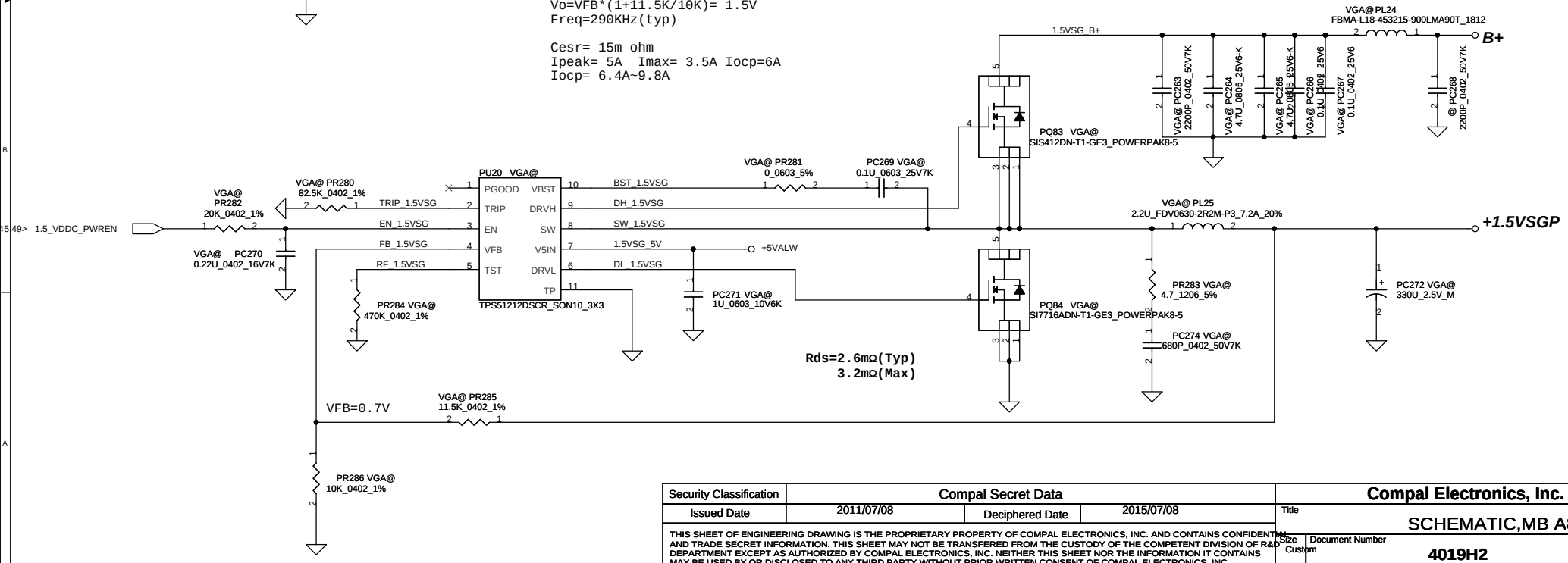
VFB= 0.7V
Vo=VFB*(1+7.15K/10K)= 1.2V
Freq= 266~314KHz , 290KHz(typ)

Cesr= 15m ohm
Ipeak= 8.5A Imax= 6A Iocp=10.2
Iocp= 10.86A~17.33A



VFB= 0.704V
Vo=VFB*(1+11.5K/10K)= 1.5V
Freq=290KHz(typ)

Cesr= 15m ohm
Ipeak= 5A Imax= 3.5A Iocp=6A
Iocp= 6.4A~9.8A



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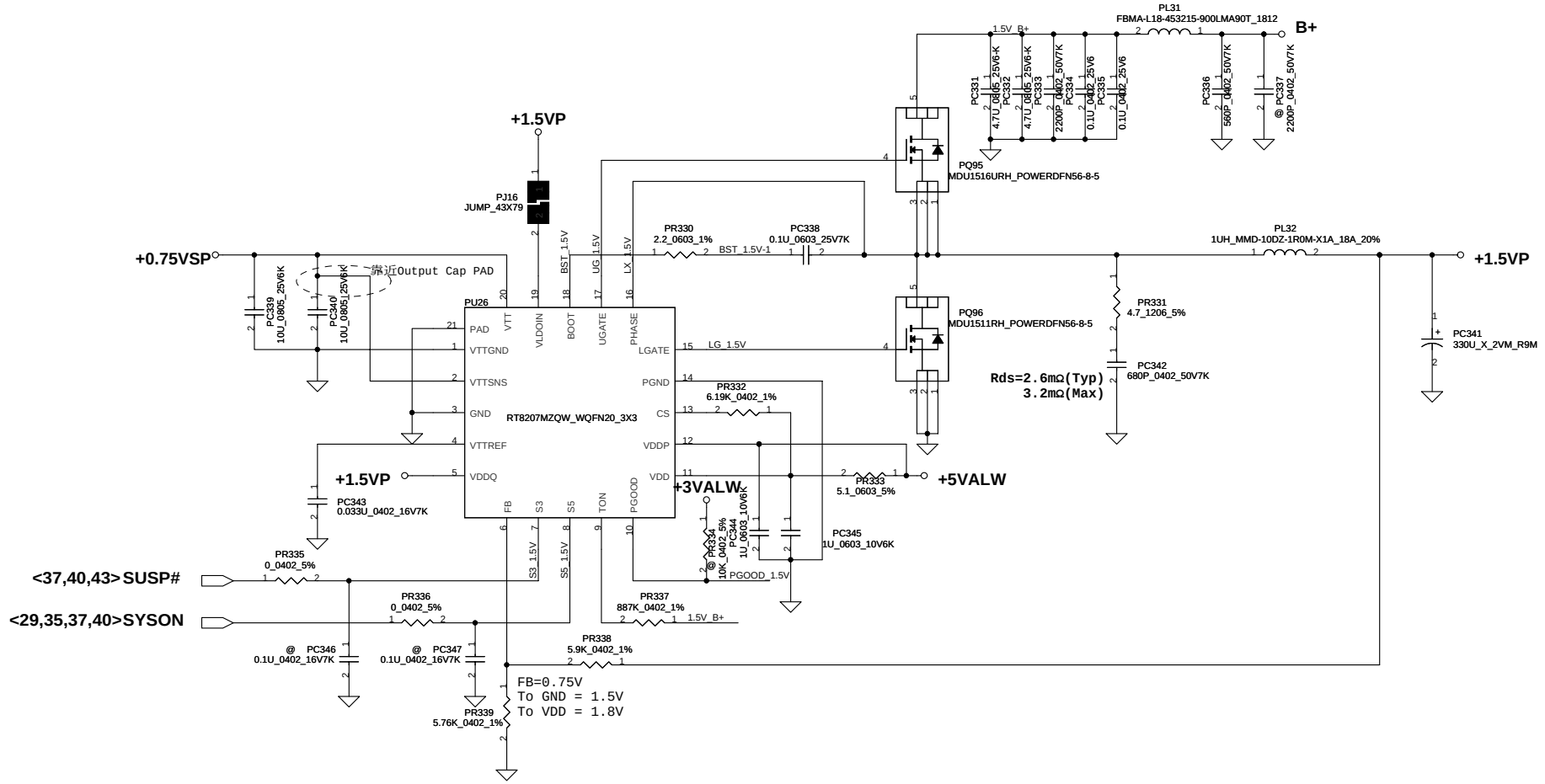

STATE	S3	S5	1.5VP	0.75VSP
S0	Hi	Hi	On	On
S3	Lo	Hi	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off				

VFB= 0.75V
Ipeak= 15A Imax= 10.5A Iocp=18A
Iocp= 17.24A~25.47A

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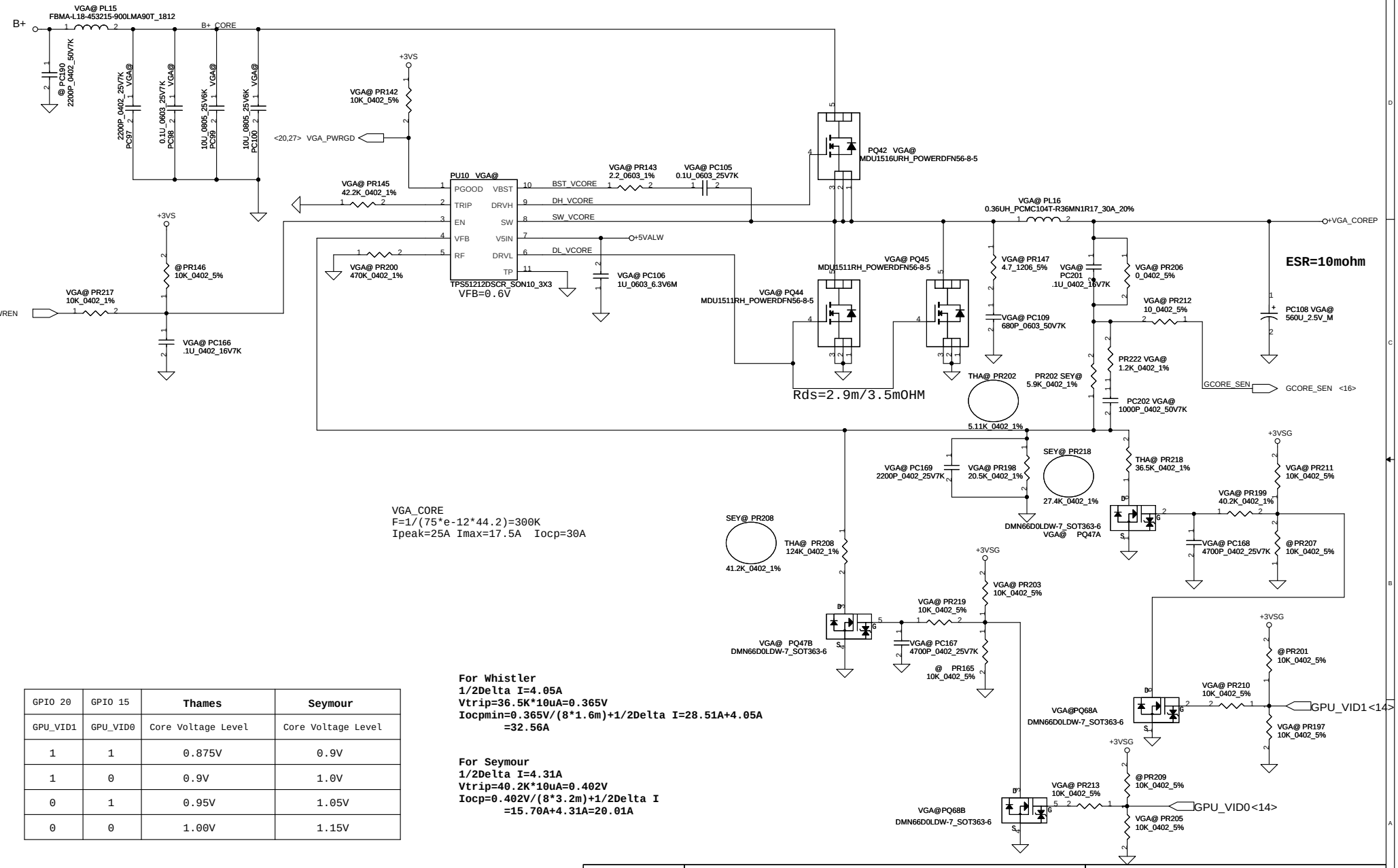

GPIO 20	GPIO 15	Thames	Seymour
GPU_VID1	GPU_VID0	Core Voltage Level	Core Voltage Level
1	1	0.875V	0.9V
1	0	0.9V	1.0V
0	1	0.95V	1.05V
0	0	1.00V	1.15V

For Whistler
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

For Seymour
1/2Delta I=4.31A
Vtrip=40.2K*10uA=0.402V
Iocp=0.402V/(8*3.2m)+1/2Delta I
=15.70A+4.31A=20.01A

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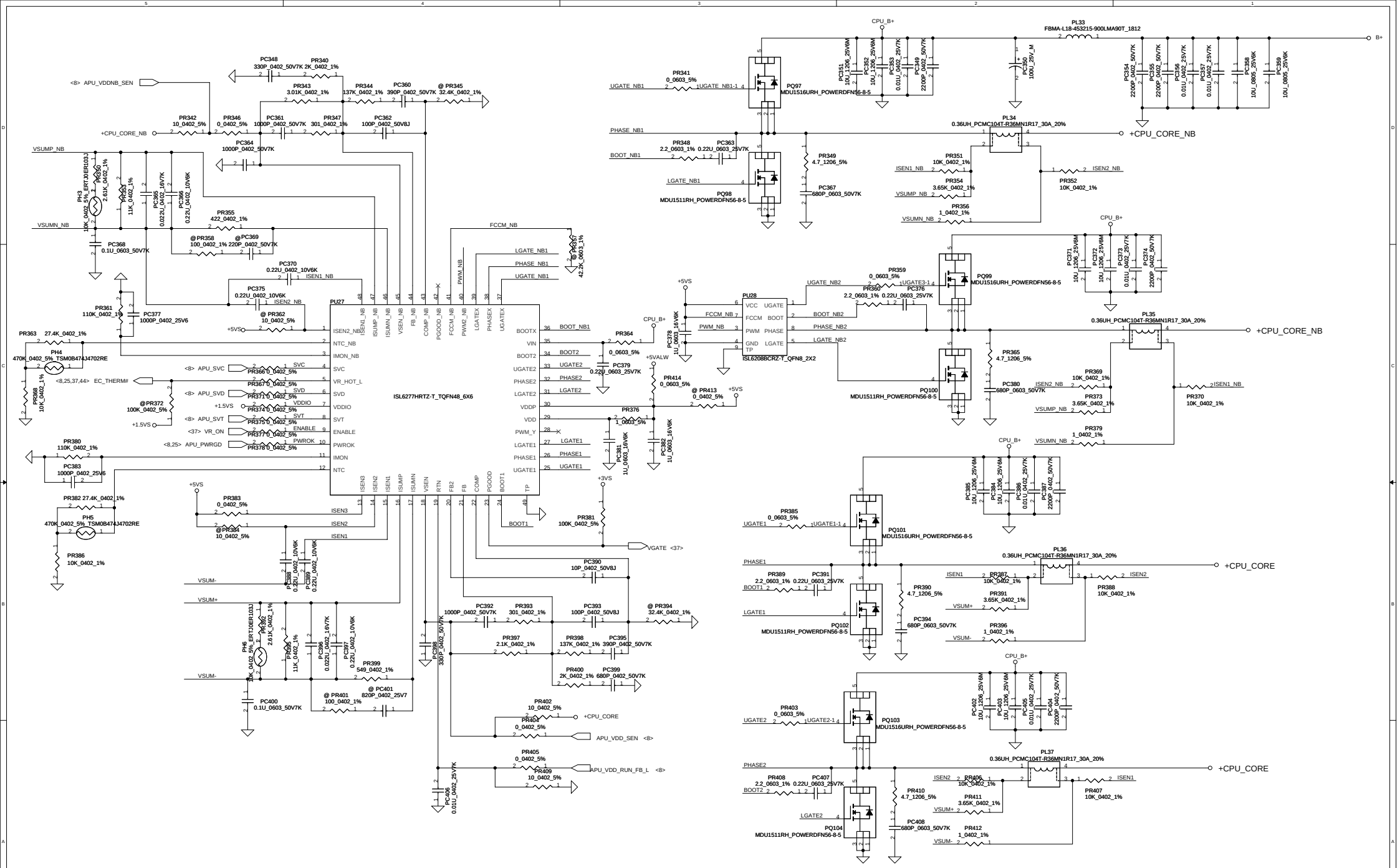

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
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Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

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Version change list (P.I.R. List)

EVT Stage (0.1~0.2)

0817 Pop C1025 180p for VDDIO (SCL v1.02)
Change D16,D17 to SCS00000Z00

0818 Change Q50 from BSH138 to BSH111
Unpop R1100 for +1.1VALW
Add D26 BOM Structure for 930@
unpop D4 for USB issue

0903 1.Change Card Reader Controller to RTS5209
2.Change LAN to Atheros AR8151
3.Removed D17

0904 Add Mini2 Debug Port

0905 1.Add Fresco FL1009 USB3.0 Controller
P20. BACO BIFVDDC update
P25. remove Q25 APU power ok

0915 1.Remove EC X2

0916 1.Add C1361/C1362 10pF for EMI
2.Change D27/D29 footprint to AZ5125
3.Add R402 10k for reserved
4.Add R469/R527 for VGA Internal Thermal Senser

0926 1.Change D4 to SC300001G00 for ESD request
2.Change D33/D34/D37/D40/D41 to SCA00001A00 for ESD request

DVT Stage (0.2~0.3)

1.Unpop C954, C955 for Mini2 reserved.
2.Remove R587, R588, Q11 for no need level shift.
3.Pop R469, R527
Unpop U9, R391, C352, C324
for VGA Internal Thermal Interface.
4.Unpop C374 330uF for Use discrete +1.5VSG circuit.
5.Add R1169 1k for RTS2132 Vender suggestion.
6.Reserved R1177 for option EEPROM.
7.Add R1178 for RTS2132 discrete +1.2VS power.
8.Reserved SMBUS(TL_CLK/TL_DATA) to EC for EEEPROM option.
9.Reserved BACO circuit and pop C1105.
10.Change D4, D6 to AZC099 for ESD reserved.
11.Change D20, D21 to AZC199-02SPR7G for ESD reserved.
12.Remove D44, D45 for no need.
13.Change C1211, R837 BOM to TL@.
14.Change JTP1 to 6P/8P co-lay footprint for WIN8.
15.Add SMBUS(FCH_SCLK1/FCH_SDATA1) for JTP1.
16.Reserved GPIO166 for future used.
17.Add H29 for ME update.
18.Add C1719, C1720 10pF for RTD5209 EMI request.
19.Change L1801 footprint.
20.Pop D42 and change to SCA00001A00 for ESD.
21.Change C1537 to 10pF 2KV for EMI/ESD.
22.Unpop C1336, C1337, C1338, C1333, C1334, C1335
for MINI2 Reserved.
23.Modify C1911 always pop for noise reduce.
24.Modify R60 to M3@.
25.Change Board ID to "02" for DVT.
26.Add Q30 for EC_THERM reverse for EC common code.
27.Change 9012_PH2 netname to 9012_VCIN for VC function.
28.Unpop R65 for External OTP.
29.Change L68 +5VS to +VDDA.
30.Chnage R1124 to 200k, R1130 to 10k for VGA Power Sequence.
31.Pop R997 for W/L BT combo card BT ON/OFF
32.Change U28 SPI ROM from MXIC to EON

PVT Stage

Security Classification	Compal Secret Data		
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