Compal Confidential

Huayra DIS (QCL51) Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Thames XT M2

Muxless/UMA / PX 5.0

2012-01-04

LA-8712P REV: 0.3

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/08	Deciphered Date 2015/07/08	Title: SCHEMATICS, MB A8712
Size: B	Document Number: 4019I5		Rev: A
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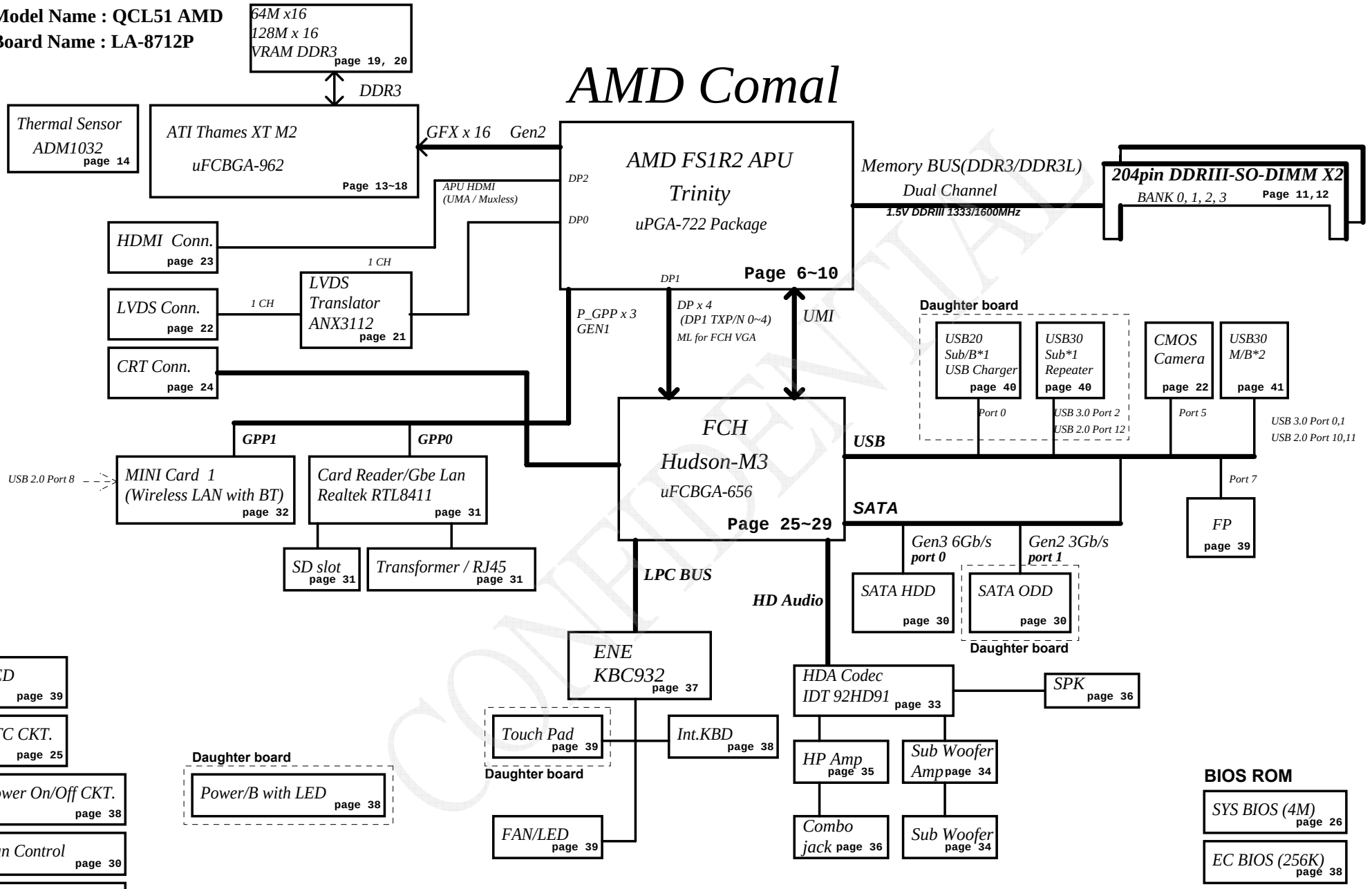
Compal Confidential

Model Name : QCL51 AMD
Board Name : LA-8712P

AMD Comal



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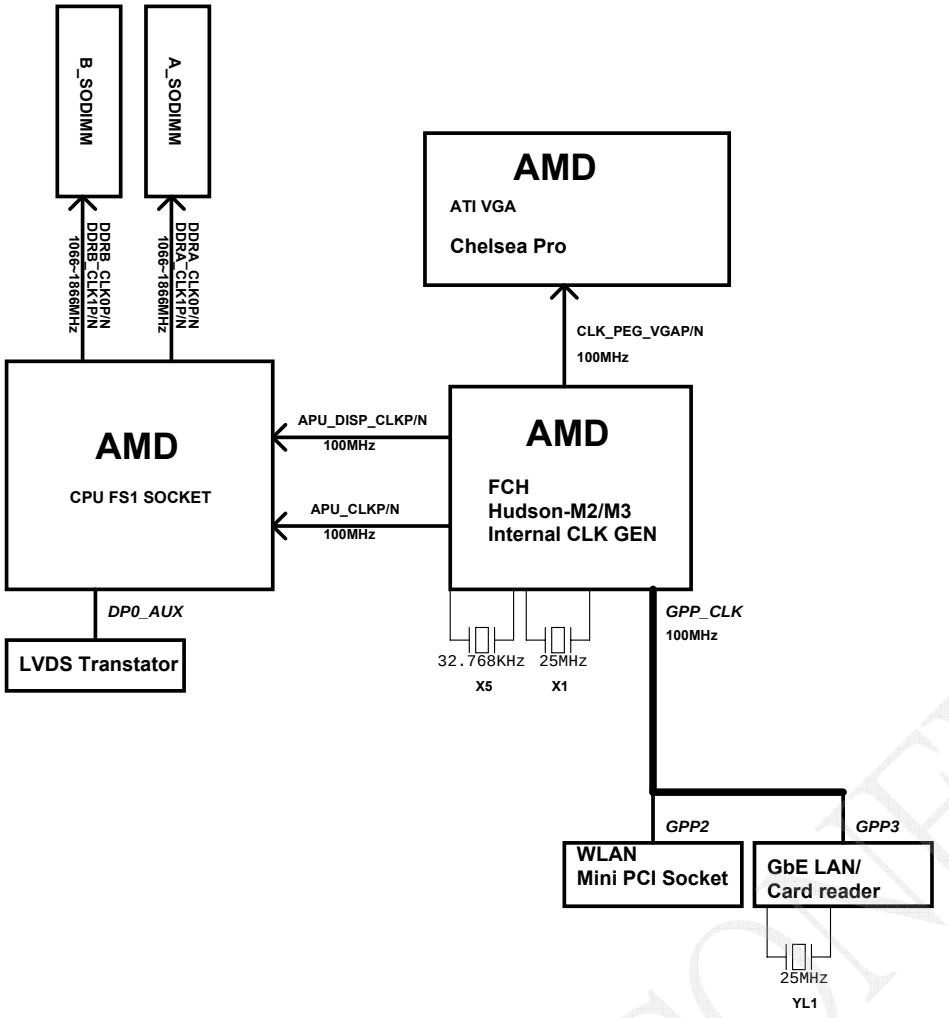
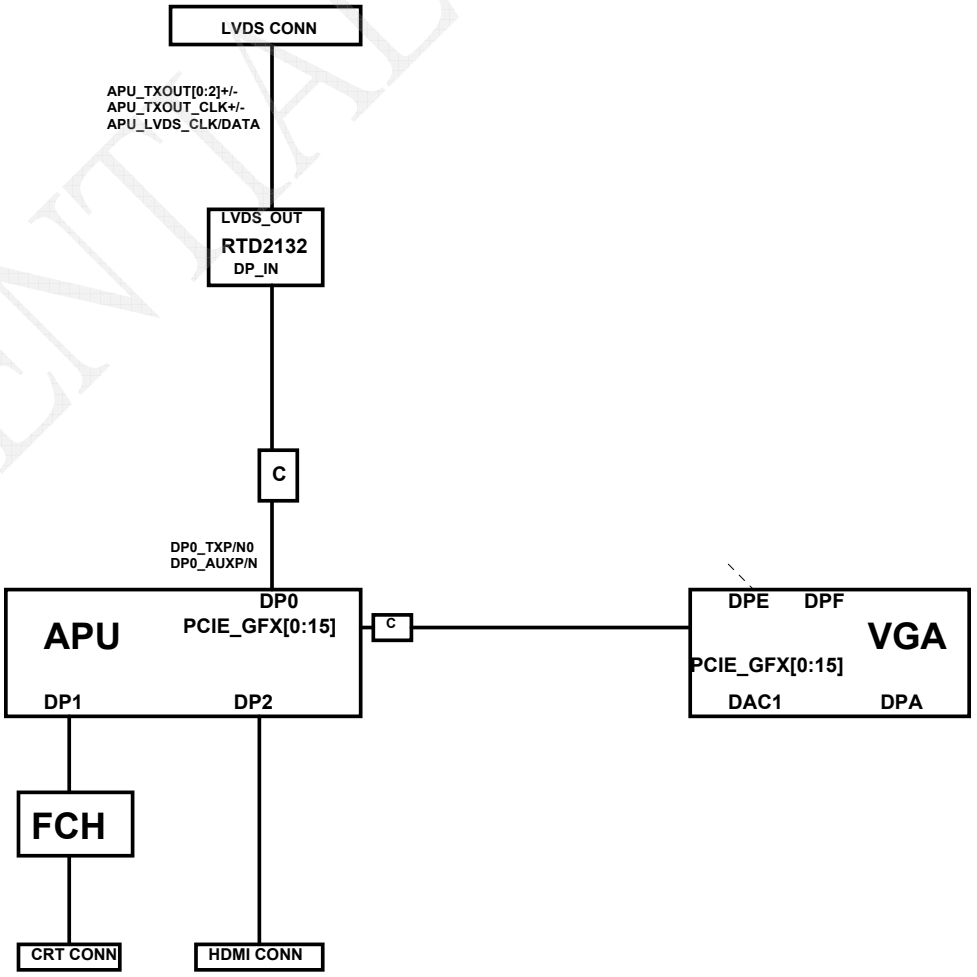
CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ZZZ1
DIS@
PCB
Part Number = DA80000SH00
PCB 0OH LA-8712P REV0 M/B

ZZZ2
UMA@
PCB
Part Number = DA60000T500
PCB 0OH LA-8712P REV0 M/B

ZZZ3
DIS@
X7638732L01
Part Number = X7638732L01

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rb	100K +/- 5%

Board ID	Ra / Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	DB
1	SI

BOM Option Table

BOM Structure	Description
PX@	PX function
DIS@	
UMA@	
Tha@	

BOM Config

DIS	PX@ DIS@ Tha@
UMA	UMA@

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (GPU)	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
LVDS TR	1010 100X b	A8H
VGA Internal Thermal	1000 001X b	82H

FCH (S0) SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1010 000X b	A0
DDR DIMM2	1010 001X b	A2
Amplifier		

FCH (S0~S5) SM Bus 1 address

Device	Address	HEX
Touch pad		

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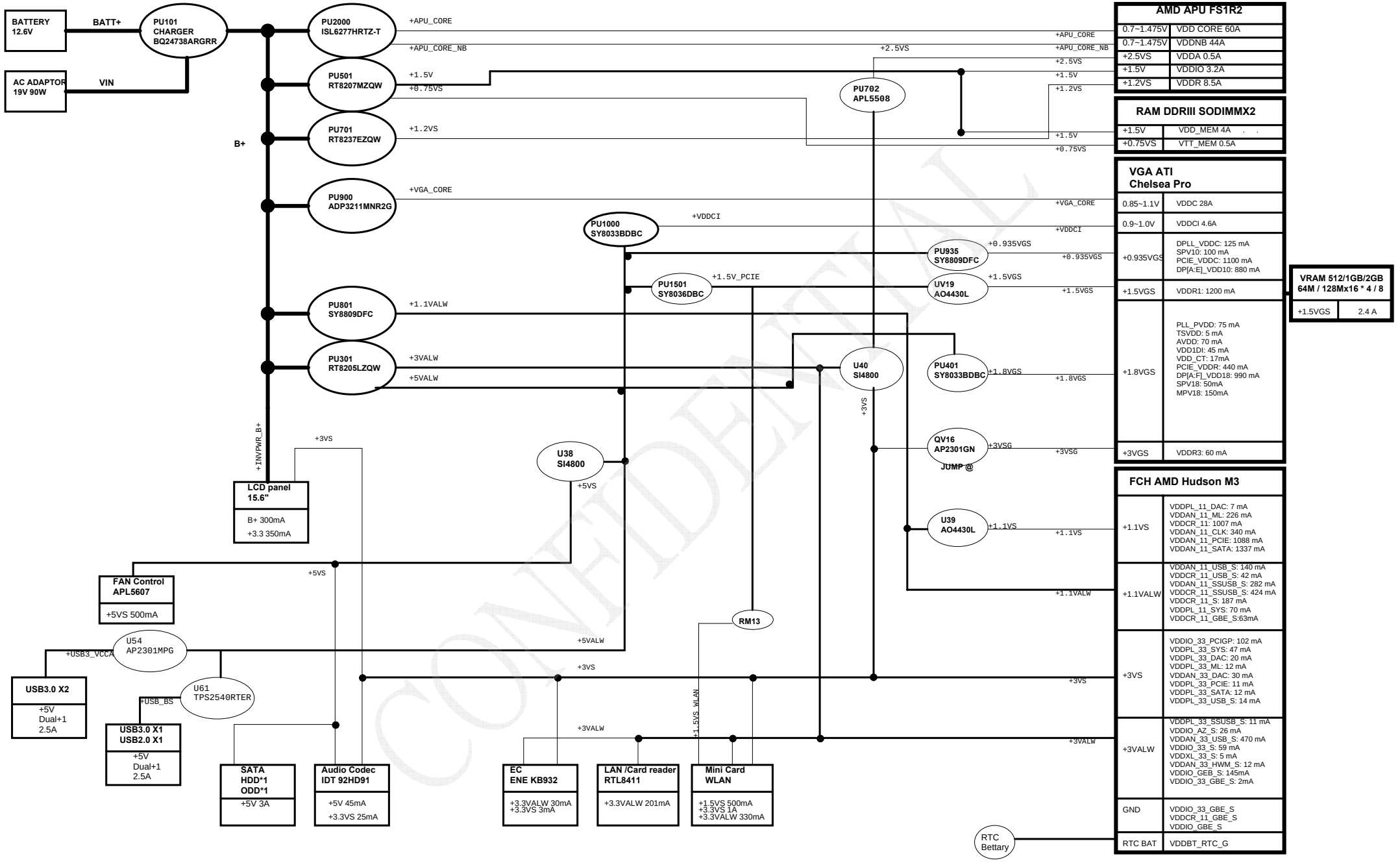

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13 PCIE_GTX_C_FRX_P[0..15]
13 PCIE_GTX_C_FRX_N[0..15]

PCIE_FTX_C_GRX_P[0..15] 13
PCIE_FTX_C_GRX_N[0..15] 13

JCPU1A

PCI EXPRESS

GRAPHICS

PCIE_GTX_C_FRX_P0	AB8	P_GFX_RXP0	P_GFX_TXP0
PCIE_GTX_C_FRX_N0	AB7	P_GFX_RXN0	P_GFX_TXN0
PCIE_GTX_C_FRX_P1	AA9	P_GFX_RXP1	P_GFX_TXP1
PCIE_GTX_C_FRX_N1	AA8	P_GFX_RXN1	P_GFX_TXN1
PCIE_GTX_C_FRX_P2	AA5	P_GFX_RXP2	P_GFX_TXP2
PCIE_GTX_C_FRX_N2	AA6	P_GFX_RXN2	P_GFX_TXN2
PCIE_GTX_C_FRX_P3	Y8	P_GFX_RXP3	P_GFX_TXP3
PCIE_GTX_C_FRX_N3	Y7	P_GFX_RXN3	P_GFX_TXN3
PCIE_GTX_C_FRX_P4	W9	P_GFX_RXP4	P_GFX_TXP4
PCIE_GTX_C_FRX_N4	W8	P_GFX_RXN4	P_GFX_TXN4
PCIE_GTX_C_FRX_P5	W5	P_GFX_RXP5	P_GFX_TXP5
PCIE_GTX_C_FRX_N5	W6	P_GFX_RXN5	P_GFX_TXN5
PCIE_GTX_C_FRX_P6	V8	P_GFX_RXP6	P_GFX_TXP6
PCIE_GTX_C_FRX_N6	V7	P_GFX_RXN6	P_GFX_TXN6
PCIE_GTX_C_FRX_P7	U9	P_GFX_RXP7	P_GFX_TXP7
PCIE_GTX_C_FRX_N7	U8	P_GFX_RXN7	P_GFX_TXN7
PCIE_GTX_C_FRX_P8	U5	P_GFX_RXP8	P_GFX_TXP8
PCIE_GTX_C_FRX_N8	U6	P_GFX_RXN8	P_GFX_TXN8
PCIE_GTX_C_FRX_P9	T8	P_GFX_RXP9	P_GFX_TXP9
PCIE_GTX_C_FRX_N9	T7	P_GFX_RXN9	P_GFX_TXN9
PCIE_GTX_C_FRX_P10	R9	P_GFX_RXP10	P_GFX_TXP10
PCIE_GTX_C_FRX_N10	R8	P_GFX_RXN10	P_GFX_TXN10
PCIE_GTX_C_FRX_P11	R5	P_GFX_RXP11	P_GFX_TXP11
PCIE_GTX_C_FRX_N11	R6	P_GFX_RXN11	P_GFX_TXN11
PCIE_GTX_C_FRX_P12	P8	P_GFX_RXP12	P_GFX_TXP12
PCIE_GTX_C_FRX_N12	P7	P_GFX_RXN12	P_GFX_TXN12
PCIE_GTX_C_FRX_P13	N9	P_GFX_RXP13	P_GFX_TXP13
PCIE_GTX_C_FRX_N13	N8	P_GFX_RXN13	P_GFX_TXN13
PCIE_GTX_C_FRX_P14	N5	P_GFX_RXP14	P_GFX_TXP14
PCIE_GTX_C_FRX_N14	N6	P_GFX_RXN14	P_GFX_TXN14
PCIE_GTX_C_FRX_P15	M8	P_GFX_RXP15	P_GFX_TXP15
PCIE_GTX_C_FRX_N15	M7	P_GFX_RXN15	P_GFX_TXN15

AB2	PCIE_FTX_GRX_P0	C917	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P0			
AB1	PCIE_FTX_GRX_N0	C918	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N0			
AA3	PCIE_FTX_GRX_P1	C919	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P1			
AA2	PCIE_FTX_GRX_N1	C920	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N1			
Y5	PCIE_FTX_GRX_P2	C921	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P2			
Y4	PCIE_FTX_GRX_N2	C922	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N2			
Y2	PCIE_FTX_GRX_P3	C923	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P3			
Y1	PCIE_FTX_GRX_N3	C924	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N3			
W3	PCIE_FTX_GRX_P4	C925	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P4			
W2	PCIE_FTX_GRX_N4	C926	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N4			
V5	PCIE_FTX_GRX_P5	C927	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P5			
V4	PCIE_FTX_GRX_N5	C928	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N5			
V2	PCIE_FTX_GRX_P6	C929	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P6			
V1	PCIE_FTX_GRX_N6	C930	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N6			
U3	PCIE_FTX_GRX_P7	C931	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P7			
U2	PCIE_FTX_GRX_N7	C932	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P8			
T5	PCIE_FTX_GRX_P8	C933	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P8			
T4	PCIE_FTX_GRX_N8	C934	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N8			
T2	PCIE_FTX_GRX_P9	C936	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P9			
T1	PCIE_FTX_GRX_N9	C937	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N9			
R3	PCIE_FTX_GRX_P10	C938	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P10			
R2	PCIE_FTX_GRX_N10	C939	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N10			
P5	PCIE_FTX_GRX_P11	C940	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P11			
P4	PCIE_FTX_GRX_N11	C941	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N11			
P2	PCIE_FTX_GRX_P12	C942	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P12			
P1	PCIE_FTX_GRX_N12	C943	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N12			
N3	PCIE_FTX_GRX_P13	C944	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P13			
N2	PCIE_FTX_GRX_N13	C945	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N13			
M5	PCIE_FTX_GRX_P14	C946	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P14			
M4	PCIE_FTX_GRX_N14	C947	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N14			
M2	PCIE_FTX_GRX_P15	C948	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P15			
M1	PCIE_FTX_GRX_N15	C949	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N15			

GPU

GPU

GPP

P_GPP_RXP0	P_GPP_TXP0	AD5	PCIE_FTX_DRX_P0
P_GPP_RXN0	P_GPP_TXN0	AD4	PCIE_FTX_DRX_N0
P_GPP_RXP1	P_GPP_TXP1	AD2	PCIE_FTX_DRX_P1
P_GPP_RXN1	P_GPP_TXN1	AD1	PCIE_FTX_DRX_N1
P_GPP_RXP2	P_GPP_TXP2	AC3	
P_GPP_RXN2	P_GPP_TXN2	AC2	
P_GPP_RXP3	P_GPP_TXP3	AB5	
P_GPP_RXN3	P_GPP_TXN3	AB4	

AD5	PCIE_FTX_DRX_P0	C950		1	2	.1U_0402_16V7K	PCIE_FTX_C_DRX_P0	31		
AD4	PCIE_FTX_DRX_N0	C951		1	2	.1U_0402_16V7K	PCIE_FTX_C_DRX_N0	31		
AD2	PCIE_FTX_DRX_P1	C952		1	2	.1U_0402_16V7K	PCIE_FTX_C_DRX_P1	32		
AD1	PCIE_FTX_DRX_N1	C953		1	2	.1U_0402_16V7K	PCIE_FTX_C_DRX_N1	32		

GLAN/Card reader
WLAN

GLAN/Card reader
WLAN

31 PCIE_DTX_C_FRX_P0 → AE5
31 PCIE_DTX_C_FRX_N0 → AE6
32 PCIE_DTX_C_FRX_P1 → AD8
32 PCIE_DTX_C_FRX_N1 → AD7

AC9
AC8
AC5
AC6

UMI

UMI

P_UMI_RXP0	P_UMI_TXP0	AG2	UMI_FTX_MRX_P0
P_UMI_RXN0	P_UMI_TXN0	AG3	UMI_FTX_MRX_N0
P_UMI_RXP1	P_UMI_TXP1	AF4	UMI_FTX_MRX_P1
P_UMI_RXN1	P_UMI_TXN1	AF5	UMI_FTX_MRX_N1
P_UMI_RXP2	P_UMI_TXP2	AF1	UMI_FTX_MRX_P2
P_UMI_RXN2	P_UMI_TXN2	AF2	UMI_FTX_MRX_N2
P_UMI_RXP3	P_UMI_TXP3	AE2	UMI_FTX_MRX_P3
P_UMI_RXN3	P_UMI_TXN3	AE3	UMI_FTX_MRX_N3

AG2	UMI_FTX_MRX_P0	C956		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_P0	25		
AG3	UMI_FTX_MRX_N0	C957		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_N0	25		
AF4	UMI_FTX_MRX_P1	C958		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_P1	25		
AF5	UMI_FTX_MRX_N1	C959		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_N1	25		
AF1	UMI_FTX_MRX_P2	C960		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_P2	25		
AF2	UMI_FTX_MRX_N2	C961		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_N2	25		
AE2	UMI_FTX_MRX_P3	C962		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_P3	25		
AE3	UMI_FTX_MRX_N3	C963		1	2	.1U_0402_16V7K	UMI_FTX_C_MRX_N3	25		

25 UMI_MTX_C_FRX_P0 → AG8
25 UMI_MTX_C_FRX_N0 → AG9
25 UMI_MTX_C_FRX_P1 → AG6
25 UMI_MTX_C_FRX_N1 → AG5
25 UMI_MTX_C_FRX_P2 → AF7
25 UMI_MTX_C_FRX_N2 → AF8
25 UMI_MTX_C_FRX_P3 → AF8
25 UMI_MTX_C_FRX_N3 → AE9

+1.2VS — R539 1 2 196_0402_1% — P_ZVDDP AG11

P_ZVDDP

P_ZVSS AH11 — R540 1 2 196_0402_1% — GND

LOTES_ACA-ZIF-109-P12-A_FS1R2
CONN@

P_ZVDDP W/S=8/12 mil, <3000mil

P_ZVSS W/S=8/12 mil, <3000mil

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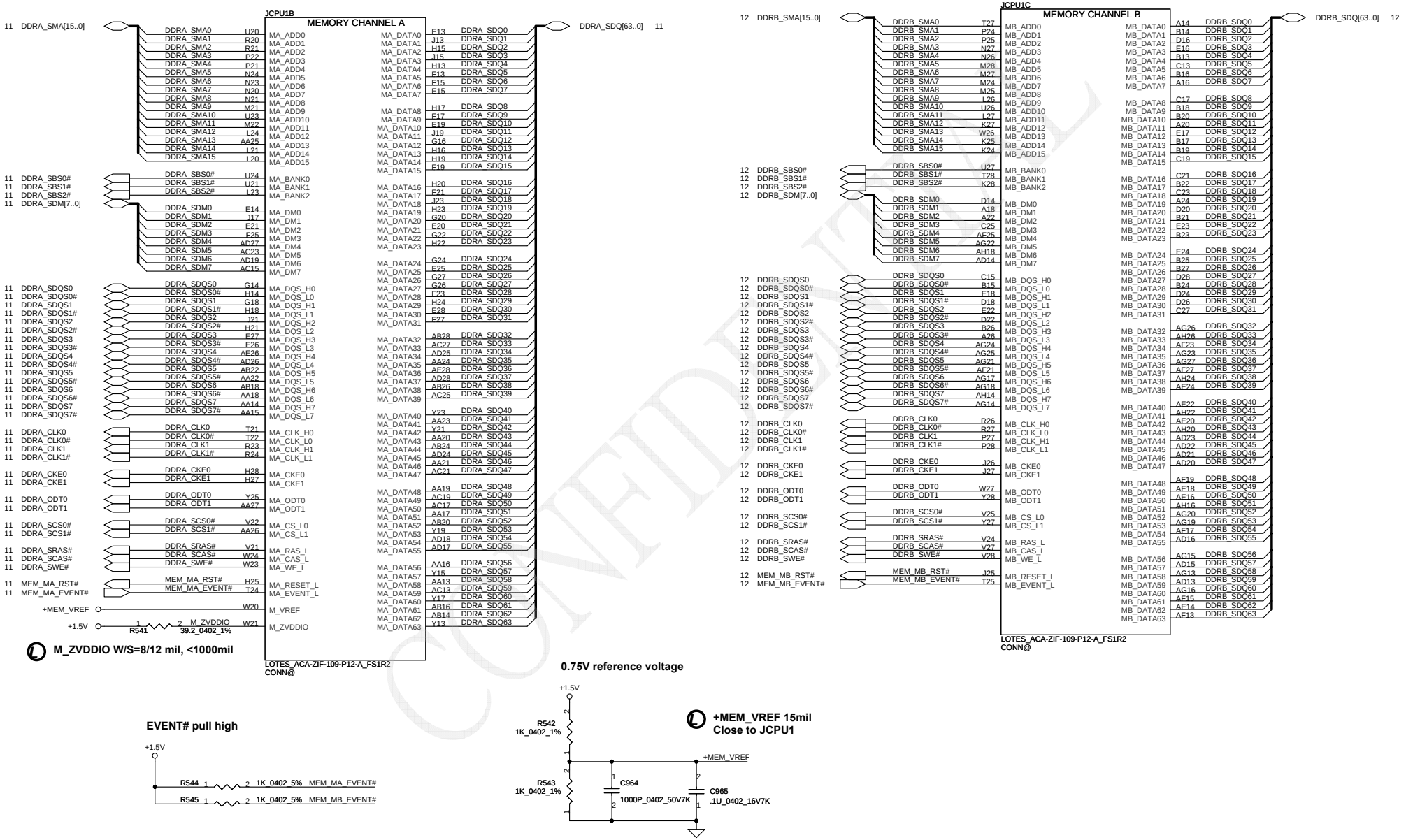

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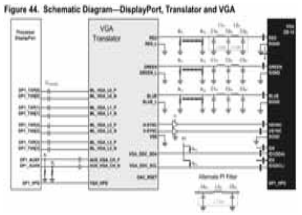

Close to APU (JCPU1)

Place near APU

JCPU1D

ANALOG/DISPLAY/MISC

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

DISPLAY PORT MISC.

CLK

SER.

CTRL

JTAG

SENSE

RSVD

TEST

To LVDS Translator

To FCH VGA ML

To HDMI

100MHz

100MHz NSS

SVI 2.0 (0 ohm at Power Side)

SB-TSI (S5 Domain)

Internal PU when no use HDT

Route as differential with APU_VDD_RUN_FB_L

LOTES_ACA-ZIF-109-P12-A_FS1R2 CONN@

To LVDS Translator

To FCH

To HDMI

LVDS/eDP
CRT
HDMI

VDDIO level
Need Level shift

DP_AUX_ZVSS W/S=8/12 mil, <3000mil

TEST35 change to PU for HDMI can not output
20110126

Allow_STOP leakage issue

For ESD request close APU side

11/15 RF

11/14 Change net name

Close to Header

10/27 300 ohm??

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

When APU High -> MOS OFF (Vgs < 0.4V)
APU Low -> MOS ON (Vgs > 1.3V)

Vg = 1.607 V

Asserted as an input to force processor into HTC-active state

THERMTRIP shutdown temperature: 115 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

HDT Debug conn

11/10 del debug connector

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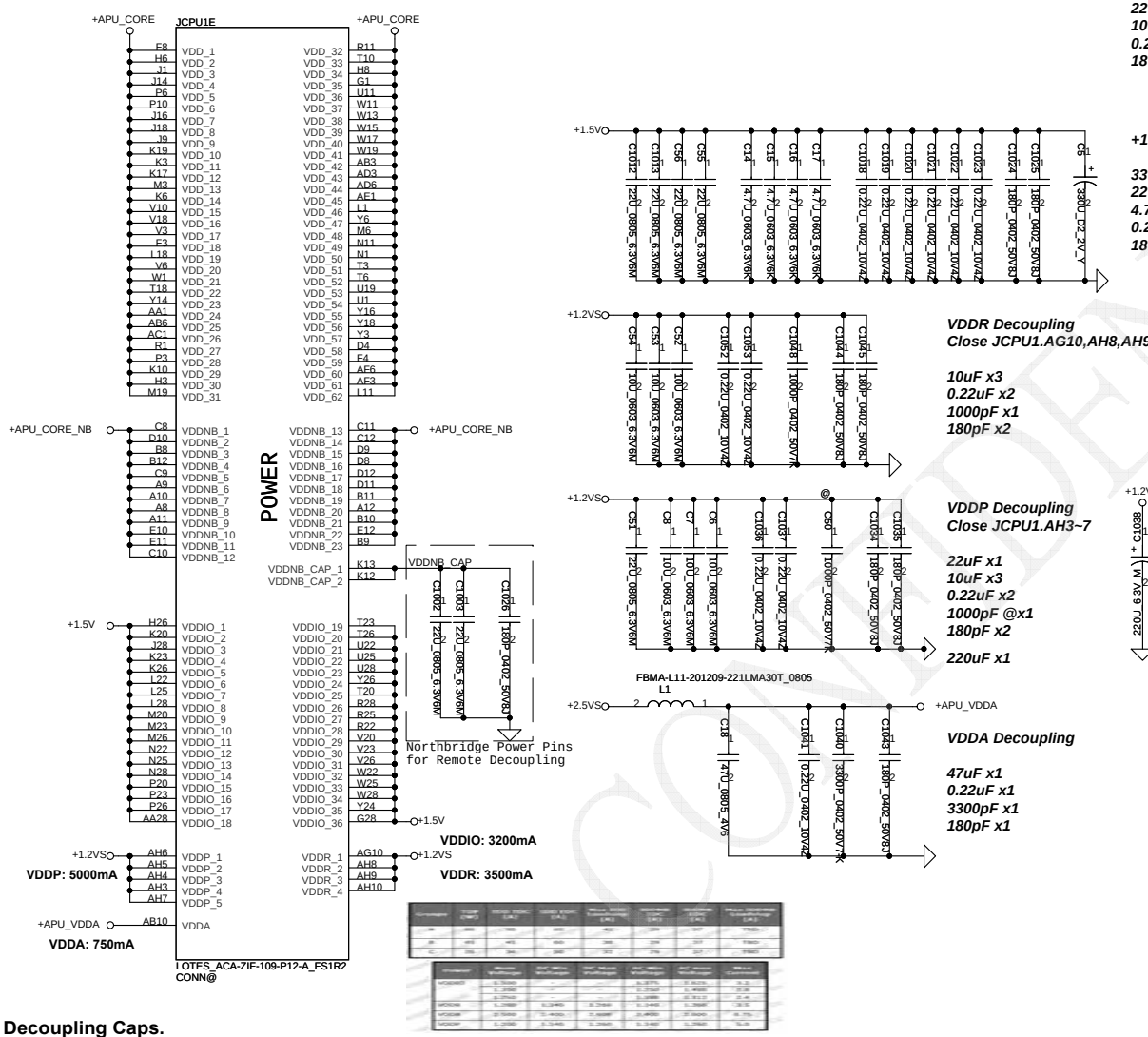
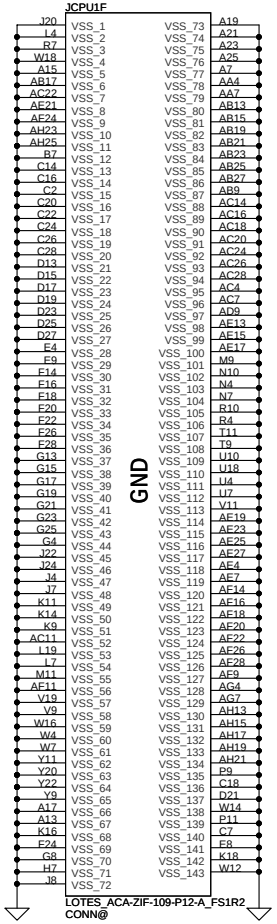
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A



+CPU_CORE Decoupling

330uF x 4 @ x1
22uF x 10
0.22uF x2
0.01uF x3
180pF x2 @ x1

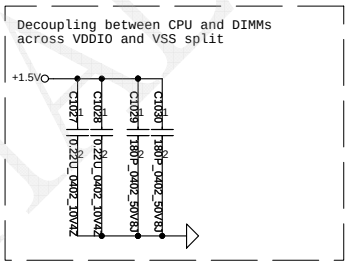


+CPU_CORE_NB Decoupling

330uF x2
22uF x2 @ x2
10uF x1
0.22uF x2
180pF x3

+1.5V / VDDIO Decoupling

330uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1



VDDR Decoupling
Close JCPU1.AG10,AH8,AH9,AH10

10uF x3
0.22uF x2
1000pF x1
180pF x2

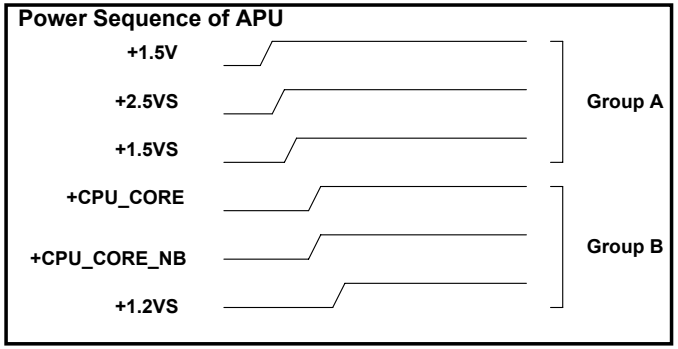
VDDP Decoupling
Close JCPU1.AH3~7

22uF x1
10uF x3
0.22uF x2
1000pF @x1
180pF x2
220uF x1

VDDA Decoupling

47uF x1
0.22uF x1
3300pF x1
180pF x1

Power Sequence of APU



Decoupling Caps.

Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0			0	19/11	7	5	17	3	1	1 / 1	13/3
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

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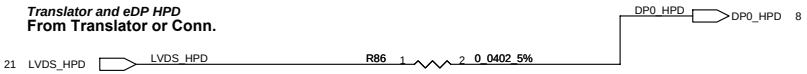
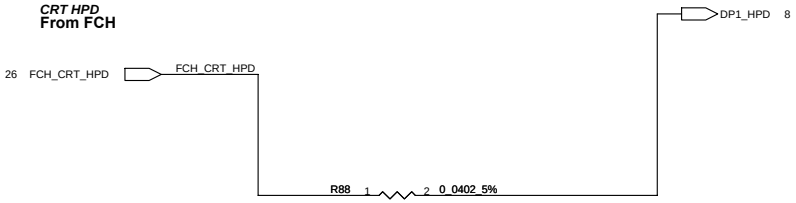
HPD

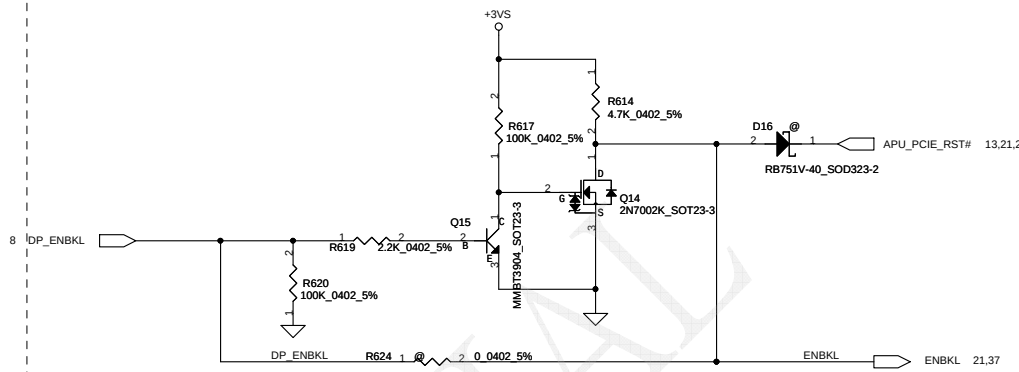
Translator and eDP HPD
From Translator or Conn.



CRT HPD
From FCH

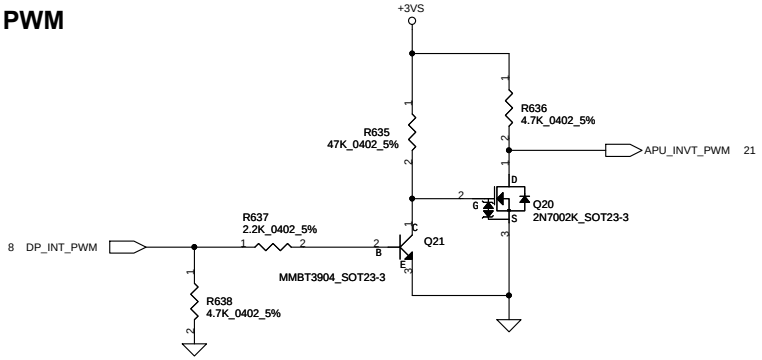


Panel ENBKL



eDP Panel ENVDD

Panel PWM



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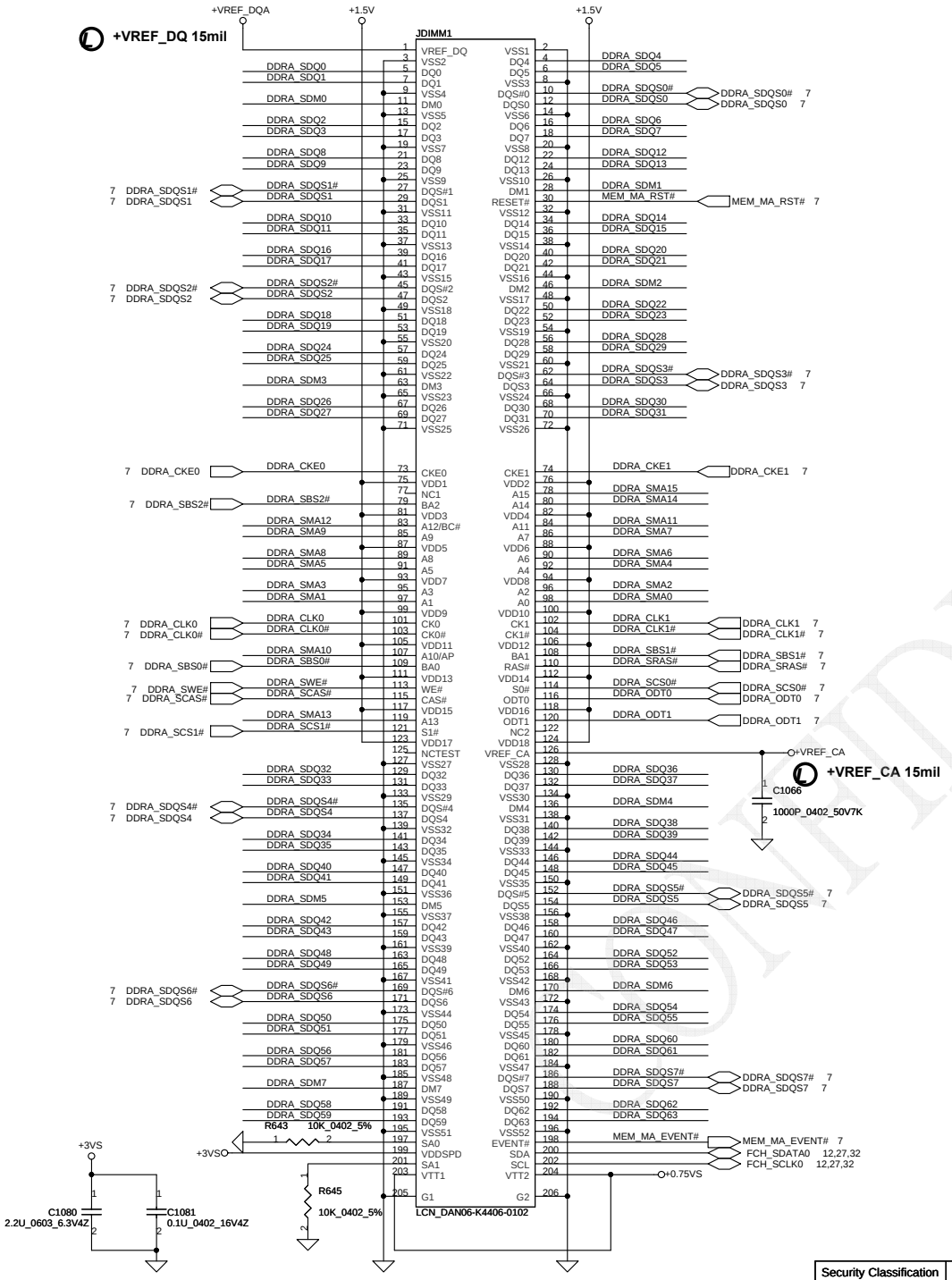

DIMM_A REV H:4mm

<Address: 00>

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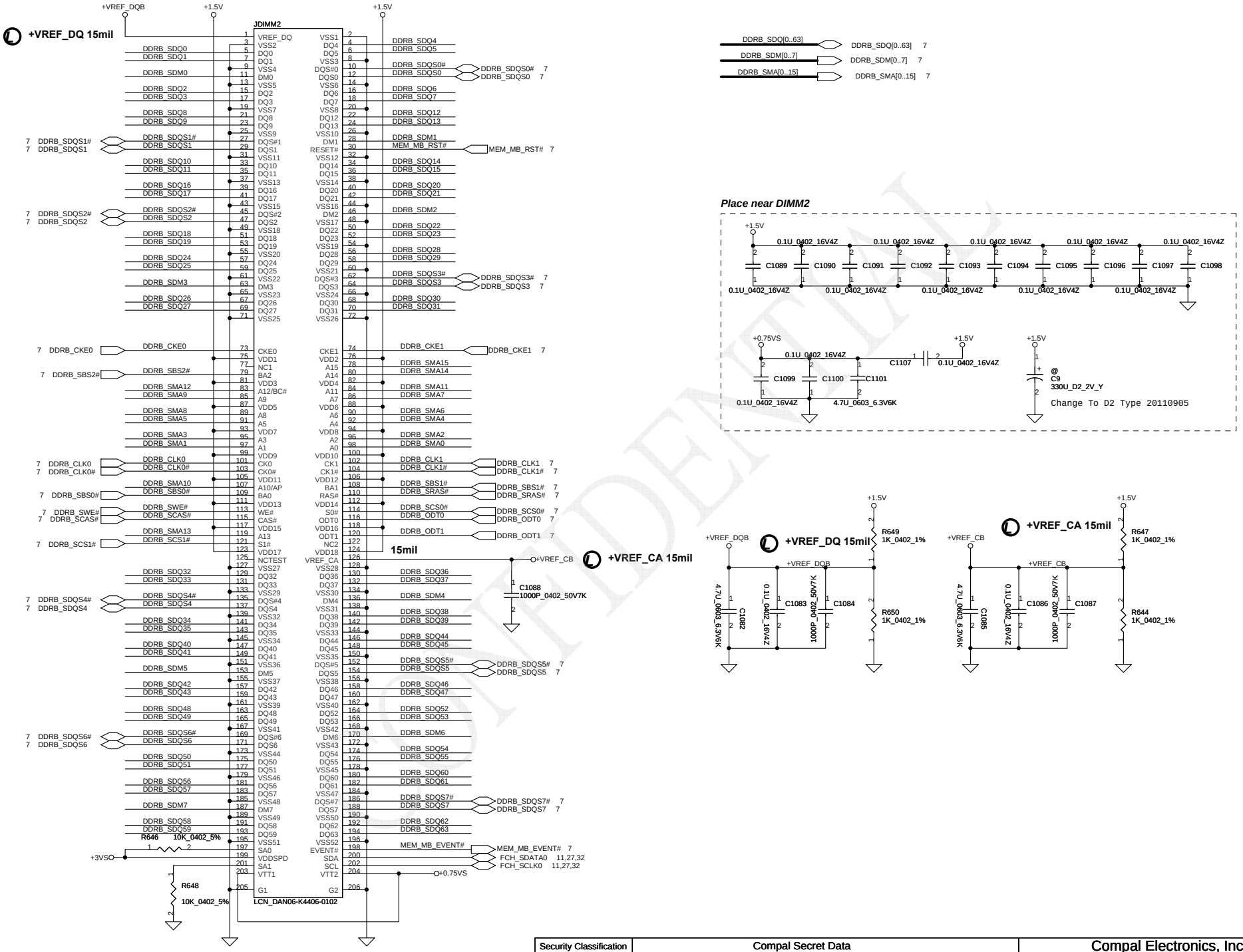

DIMM_B REV H:8mm

<Address: 01>

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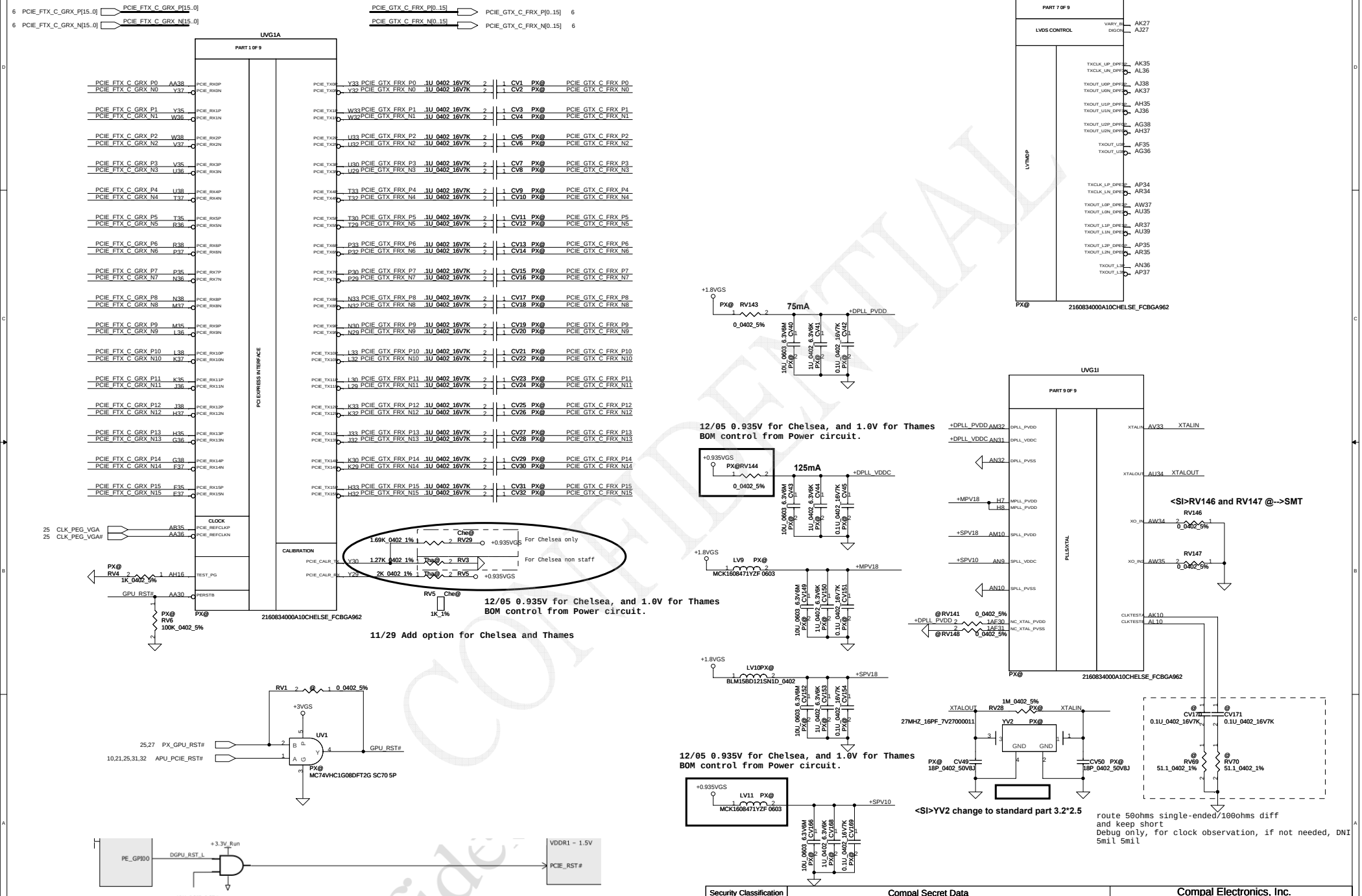
LVDS Interface



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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS <all internal PD>	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE TRANSMITTER Power Saving Enable 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	Internal use only.This Pad has an internal PD and Must be 0V at reset. The pad may be left unconnected.	0
RSVD	H2SYNC		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT GPIO13,12,11(config 2,1,0): internal PD. a)If BIOS_ROM_EN=1,the config[2:0] defines the ROM type. b)If BIOS_ROM_EN=0,the config[2:0] defines the primary aperture size.	XXX Memory apertures config[3:0] 128MB 000 256MB 001 64MB 010
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defalt setting for desktop)

STRAPS

PCIE1.0:RV9 SMT-->@
PCIE2.0:RV9 SMT-->PX@

VRAM ID

Internal VGA Thermal Sensor

Use Internal Thermal Sensor
External VGA Thermal Sensor: Need stuff

<SI> BOM thermal IC and part SMT-->@

<SI>BOM RV66 1K-->5.11K

12/05 Add PD for GPIO_28
Thames PH
Chelsea PD

12/5 Reserve for MLPS

<SI> add RV42 -->0 ohm

Base on AMD Check list
GPIO_23_CLKREQB should be reserve

UVG1B
PART 2 OF 9

2160834000A10CHELSE_FCBGA962

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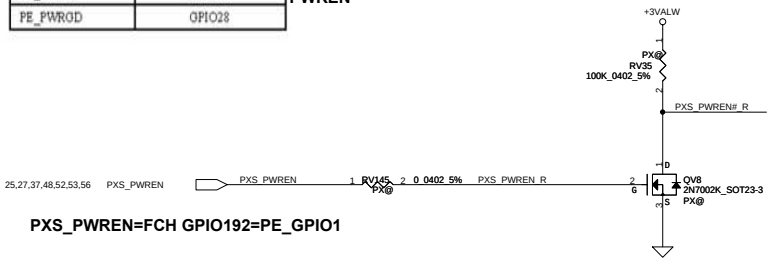
Name	FCH Pin Assignments
	Hudson-2 / Hudson-3
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192
PE_PWROD	GPIO28

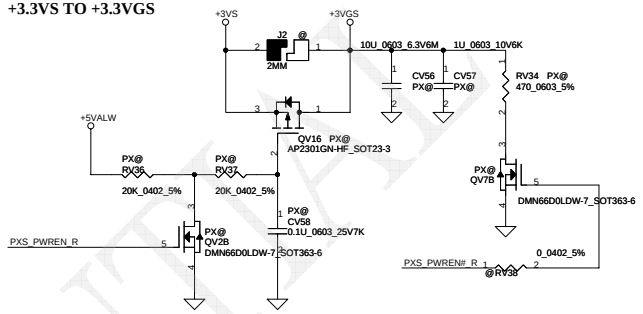
GPU_Reset

PWREN



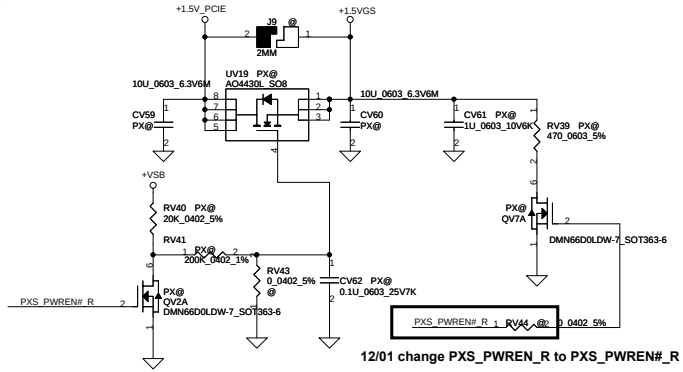
PXS_PWREN=FCH GPIO192=PE_GPIO1

+3.3VS TO +3.3VGS



+1.5V_PCIE TO +1.5VGS

Add +1.5VGS DC DC



12/01 change PXS_PWREN_R to PXS_PWREN#_R

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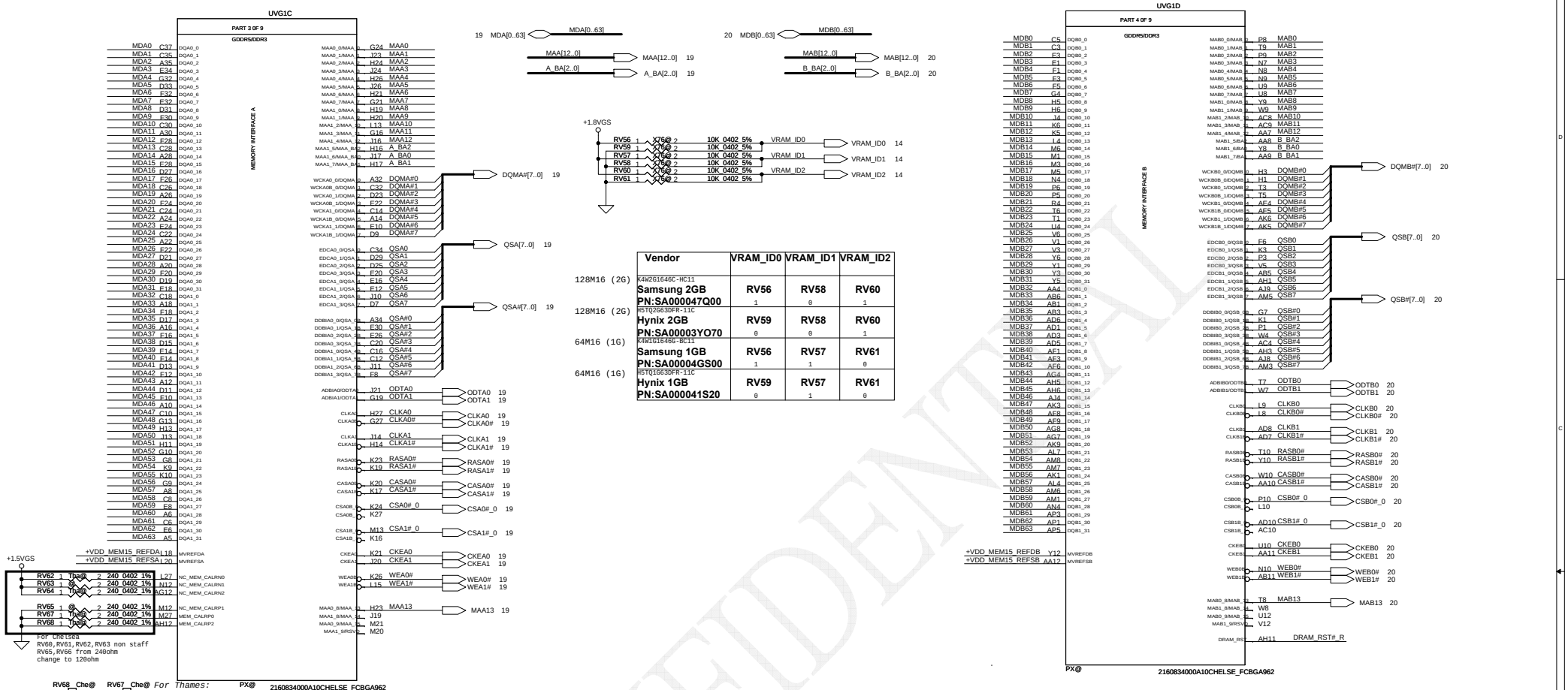

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
128M16 (2G) K4W2G1646C-HC11			
Samsung 2GB PN:SA000047Q00	RV56 1	RV58 0	RV60 1
128M16 (2G) H5TQ2G63DFR-11C			
Hynix 2GB PN:SA00003YO70	RV59 0	RV58 0	RV60 1
64M16 (1G) K4W1G1646G-BC11			
Samsung 1GB PN:SA00004GS00	RV56 1	RV57 1	RV61 0
64M16 (1G) H5TQ1G63DFR-11C			
Hynix 1GB PN:SA000041S20	RV59 0	RV57 1	RV61 0

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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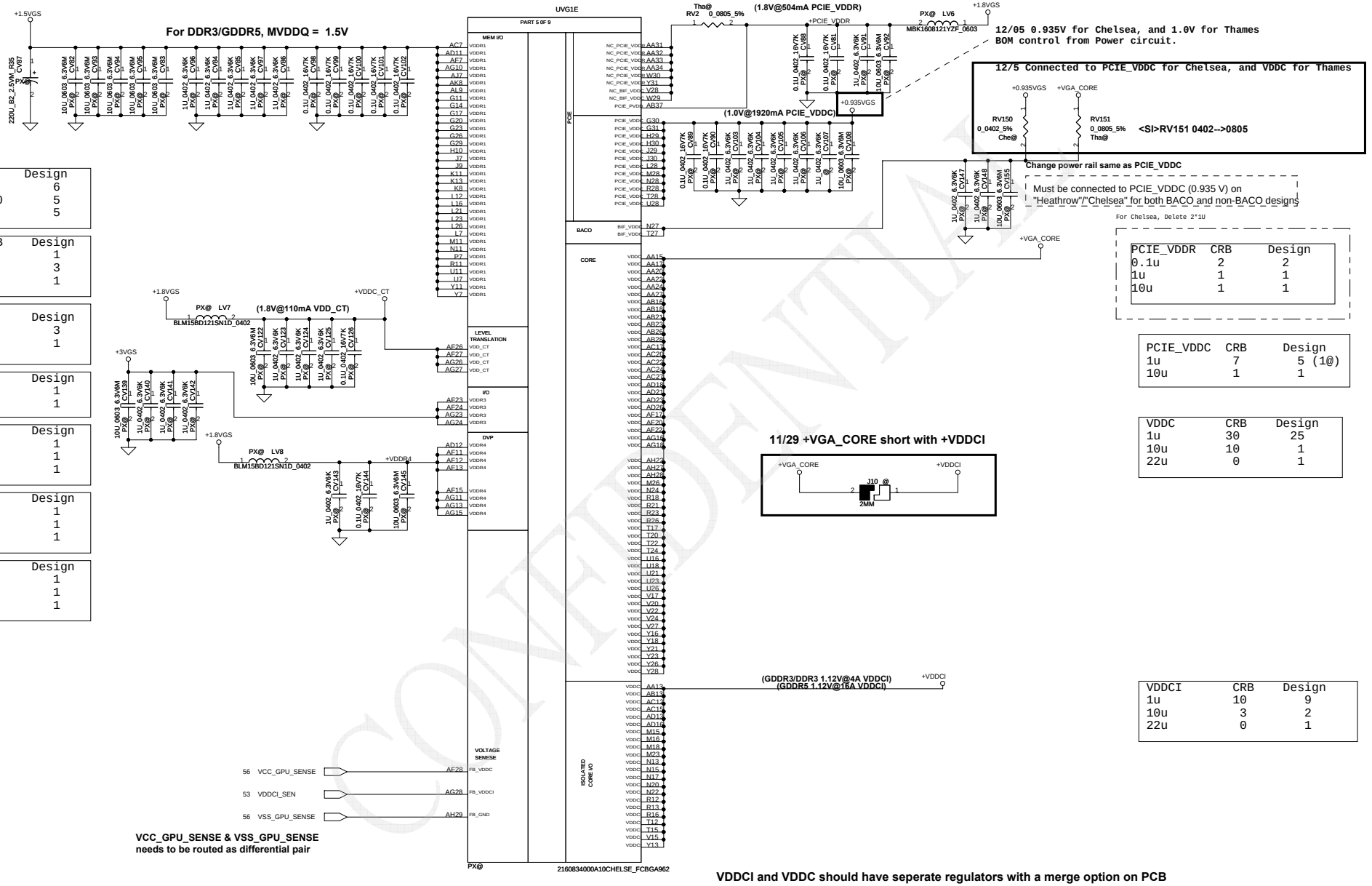

VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

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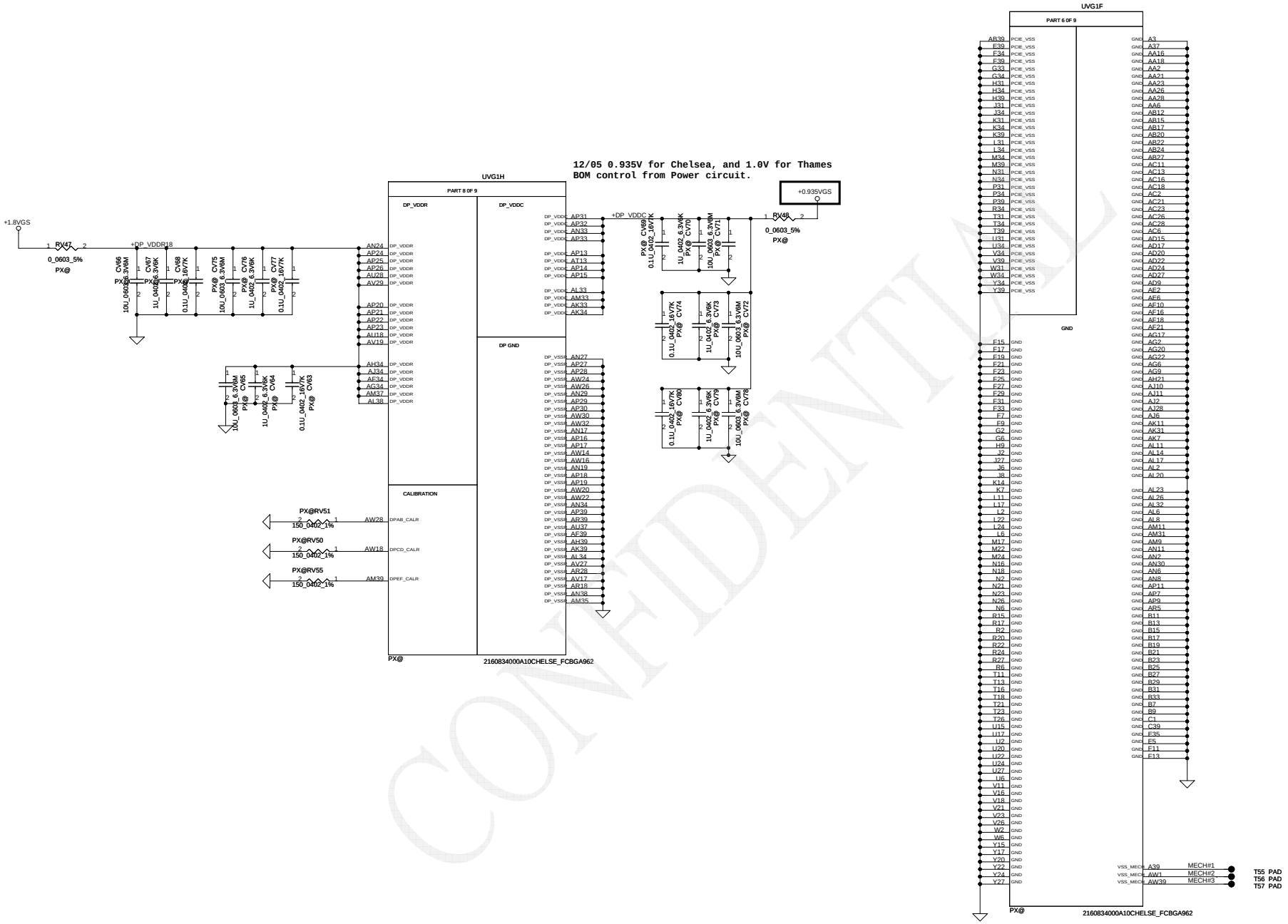

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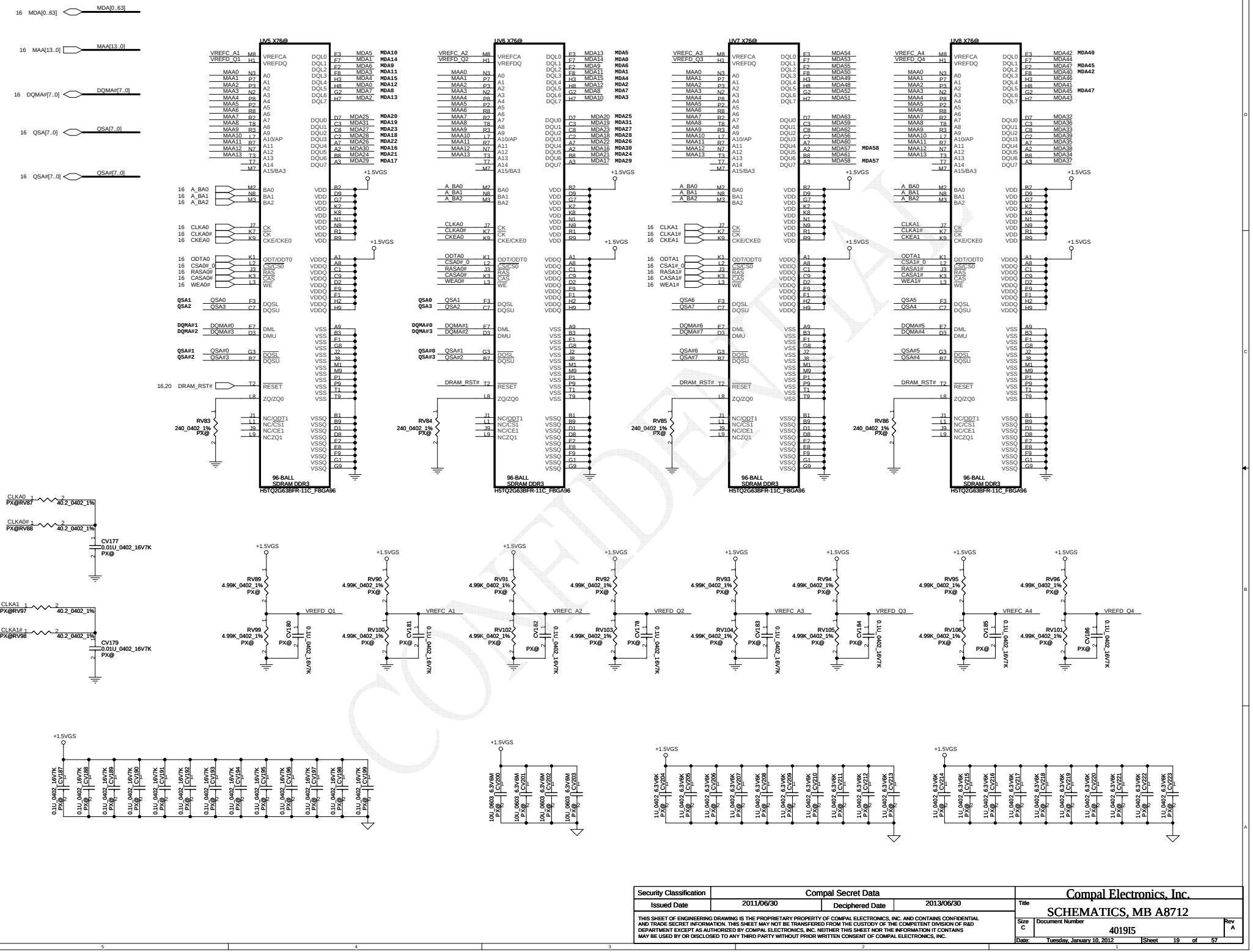

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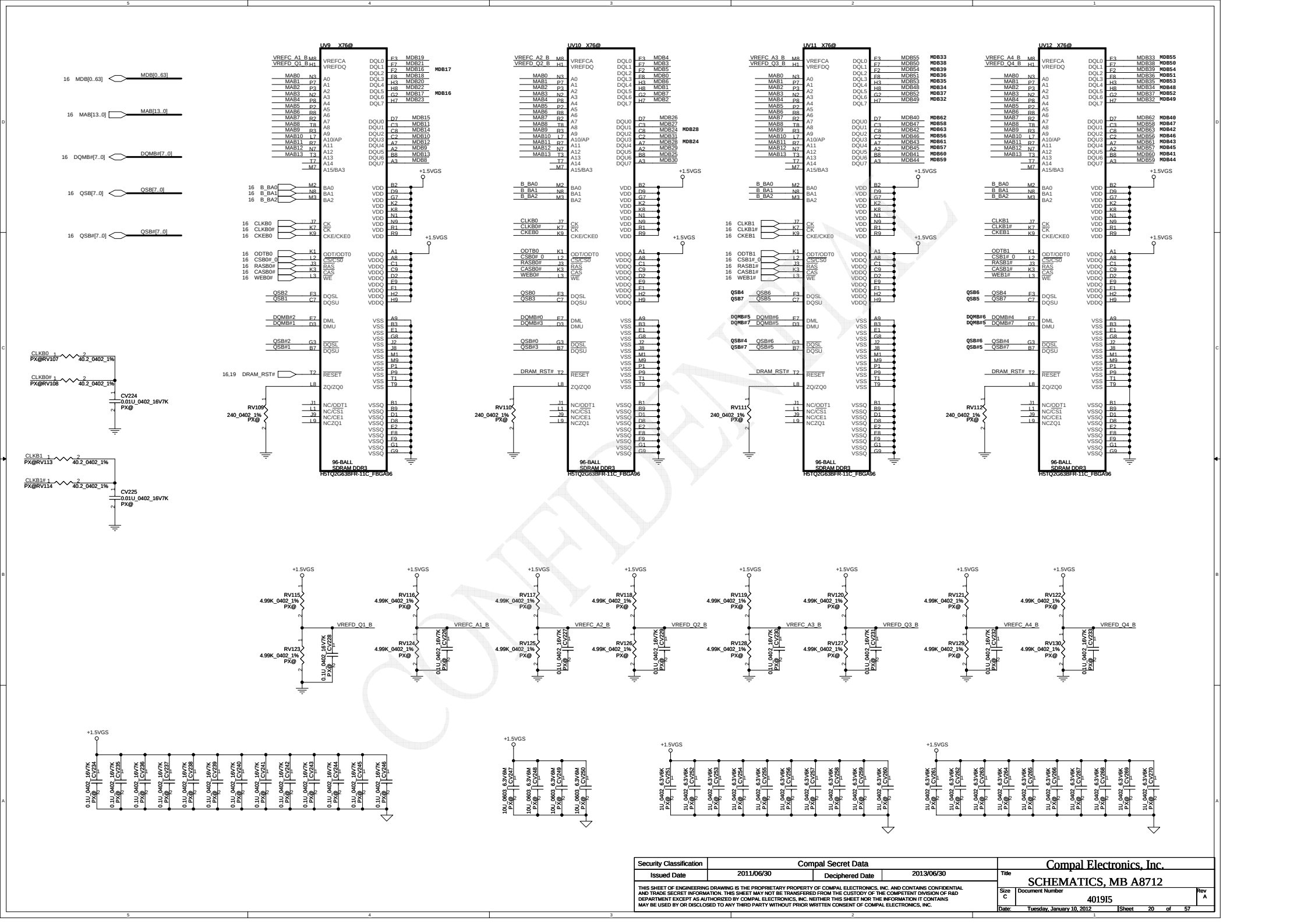

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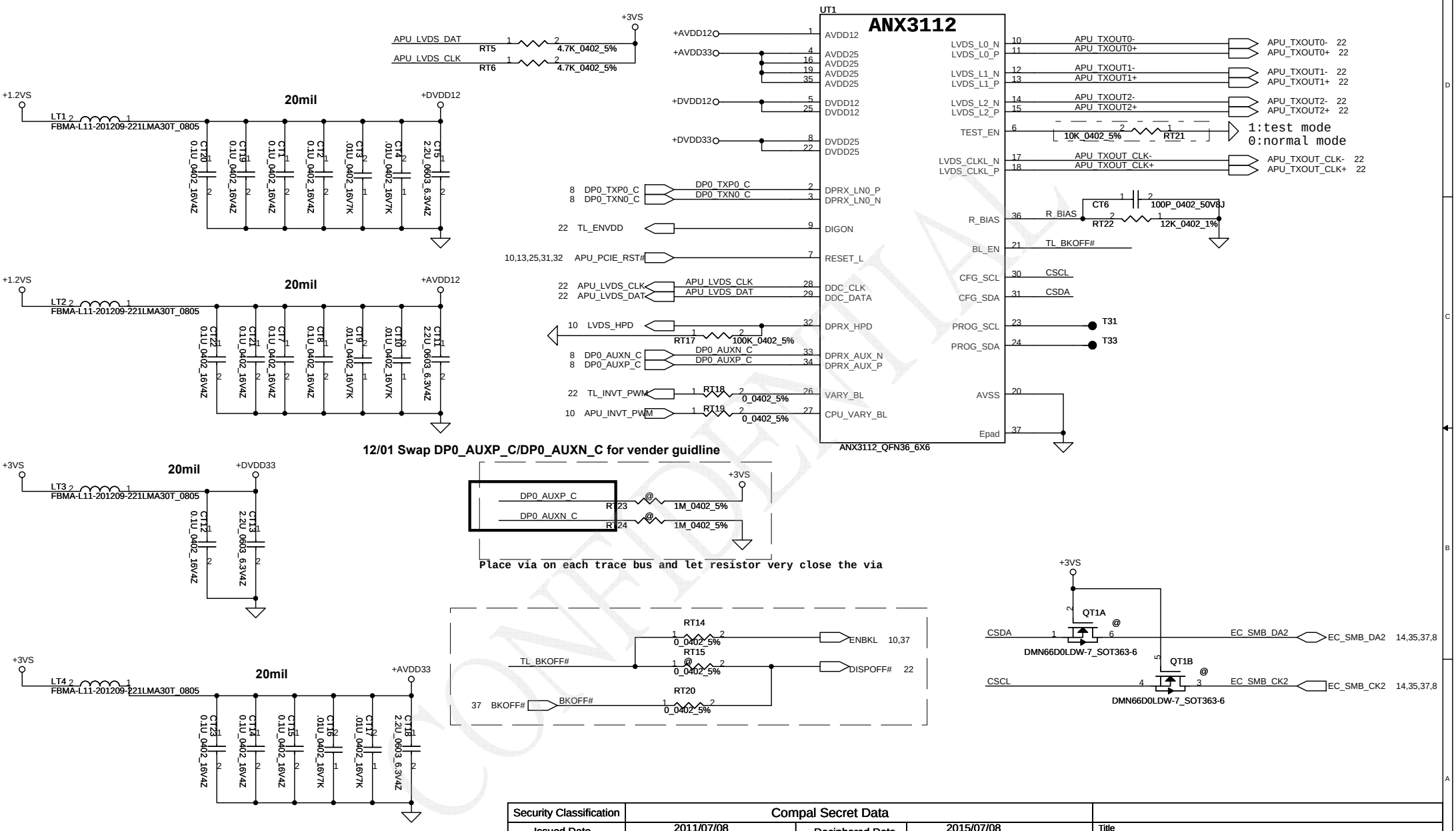

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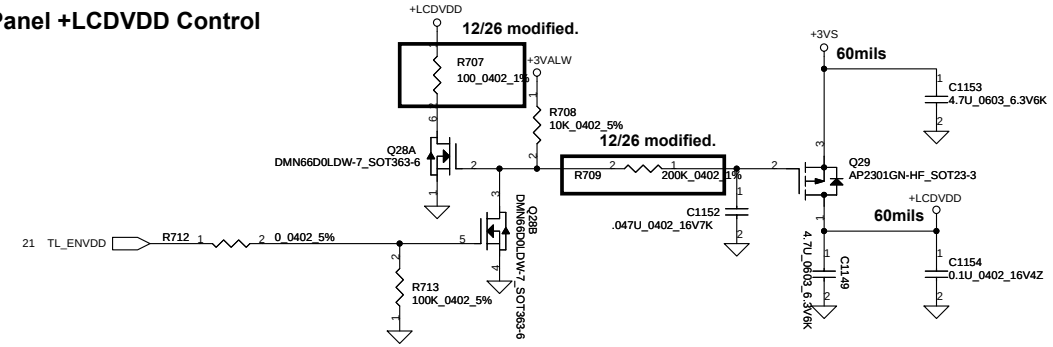
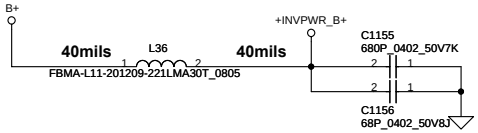
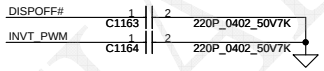
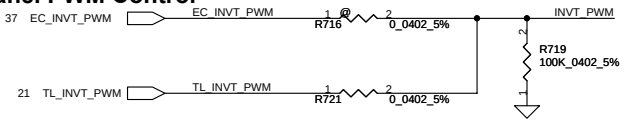
Panel +LCDVDD Control

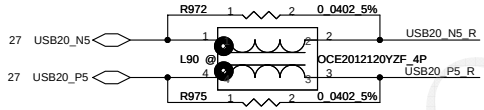


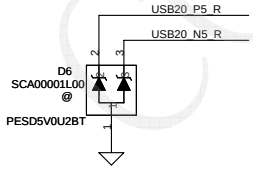




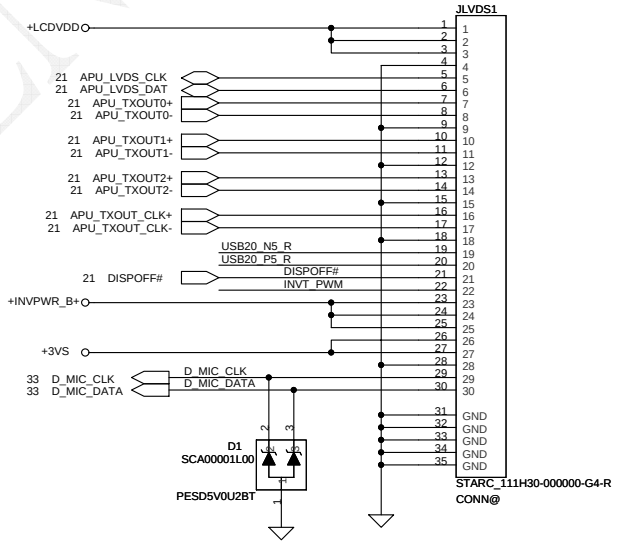
Panel PWM Control







LVDS Connector



<Translator LVDS Output>

no updated.

11/10 follow QCL50

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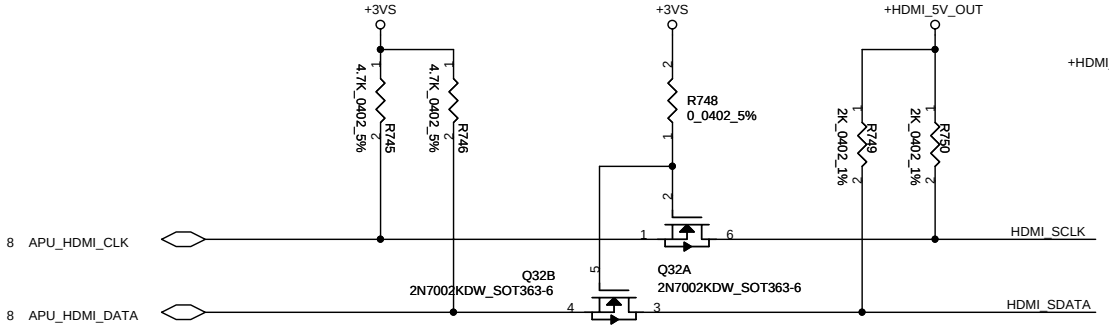
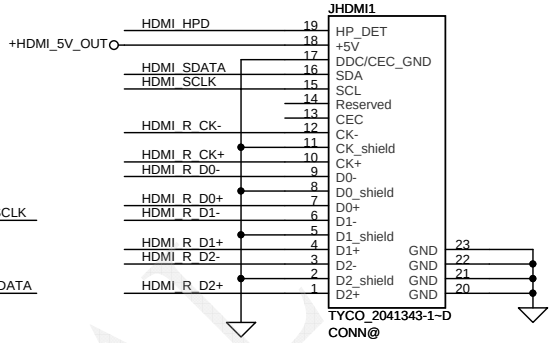
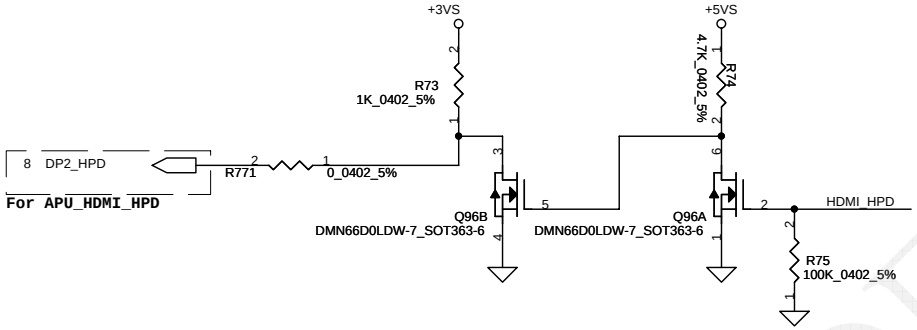
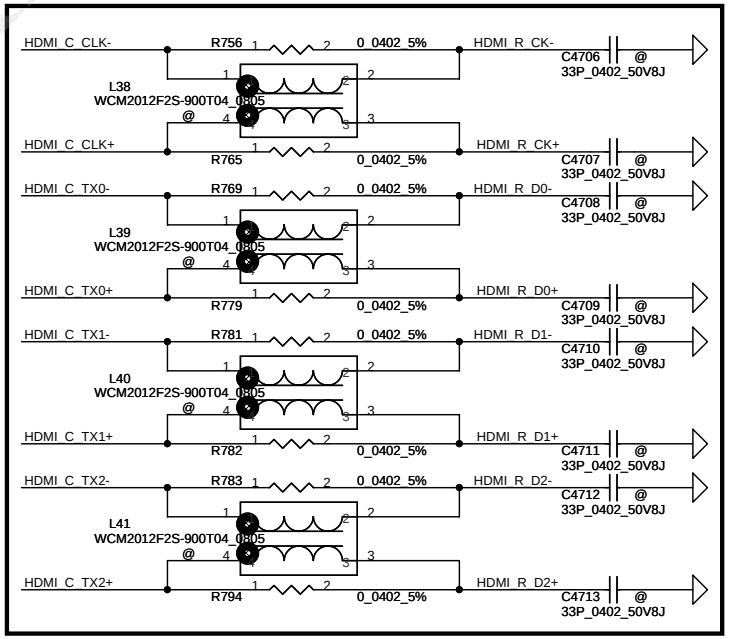




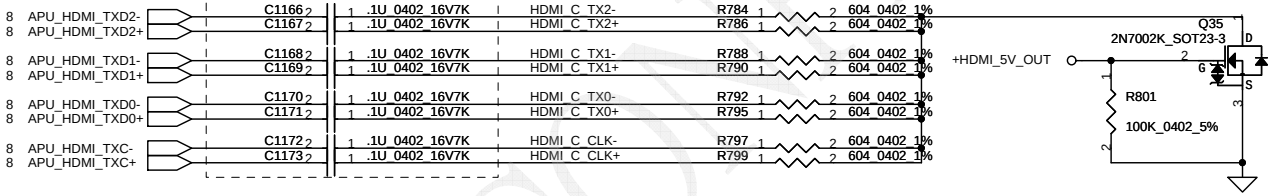


12/7 Swap signlas for routing smoothly



From APU

Close to HDMI conn



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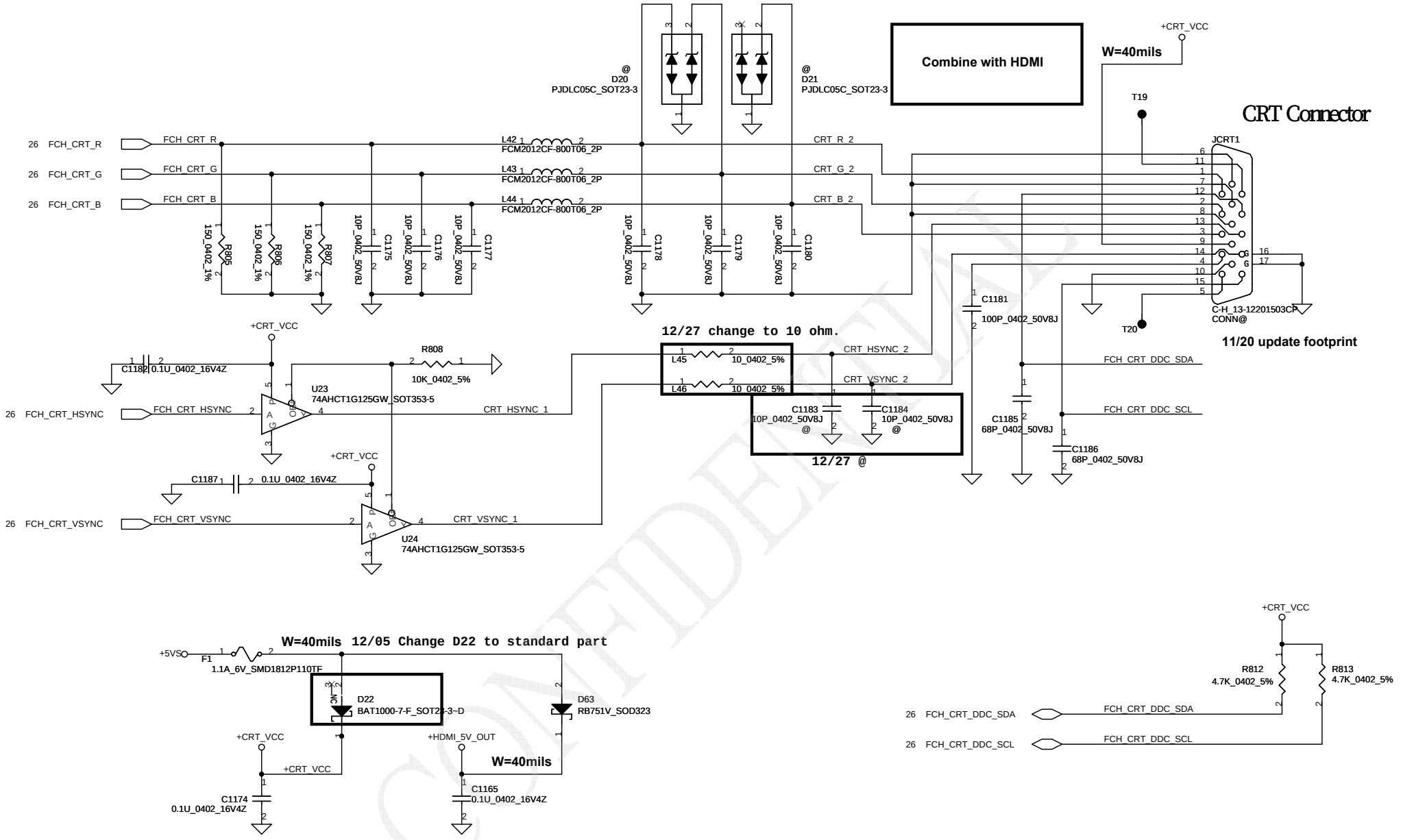

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Issued Date	2011/07/08	Deciphered Date	2015/07/08

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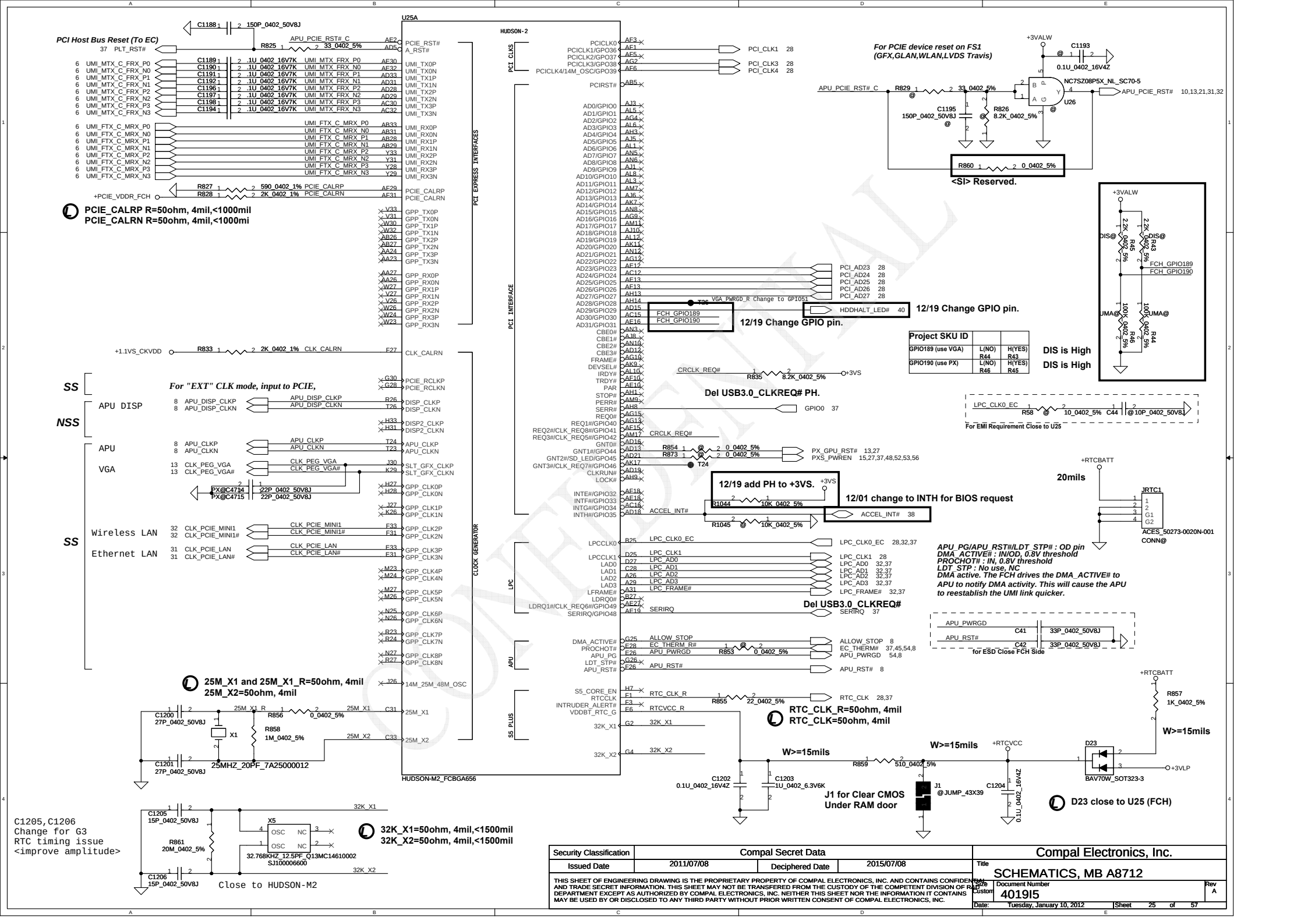

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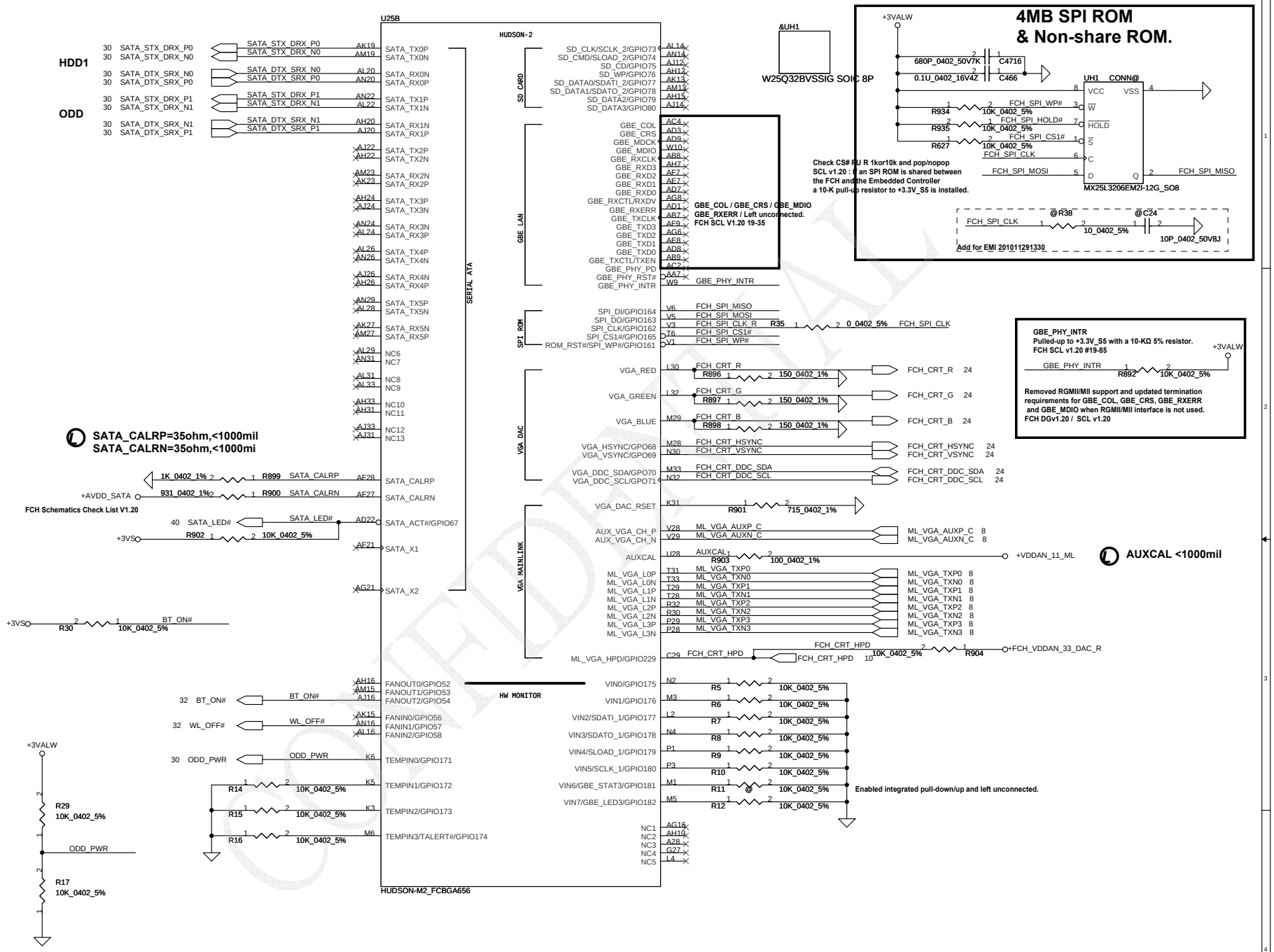

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Issued Date	2011/07/08	Deciphered Date	2015/07/08

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FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

FCH GEVENT (S5 domain)
with isolation circuit to avoid leakage

Del Card det

33ohm termination resistor at CODEC side

Change GPIO fellow Pumori

12/19 Change GPIO pin.

12/26 Reserved.

For FCH internal debug use

U25D

HUDSON-2

HUDSON-M2_FCBGA656

Hudson-M2/M3 OHCI CTL DEV 20, Fn 5 <Disable CTL>

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

USB 2.0 port(Right-1)
USB 2.0 port(Left-2)
USB 2.0 port(Left-1)

Hudson-M2/M3 EHCI CTL DEV 19, Fn 2

Mini1-WLAN
FP
Camera

12/01 change port 1 to port 7

Hudson-M2/M3 EHCI CTL DEV 18, Fn 2 <Support Wakeup>

USB 2.0 port(Right-2)

USBSS_CALRP=35ohm,<1000mil
USBSS_CALRN=35ohm,<1000mi

Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

USB 3.0 port(Right-1)
USB 3.0 port(Left-2)
USB 3.0 port(Left-1)

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

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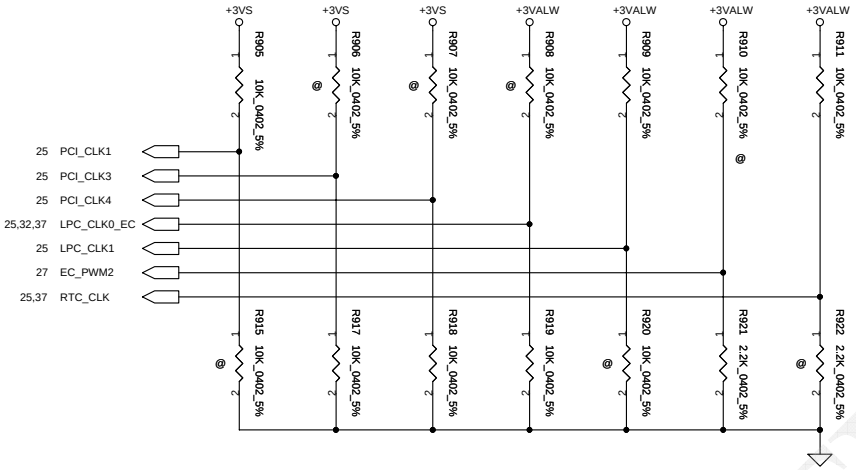
Change to SPI

STRAP PINS

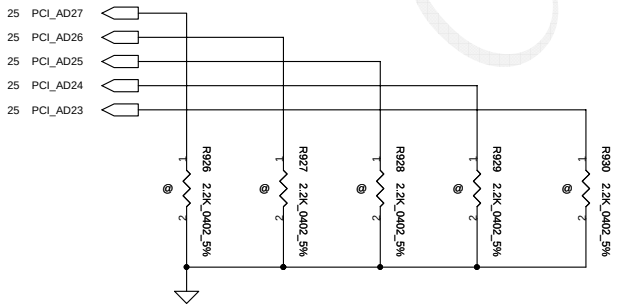
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

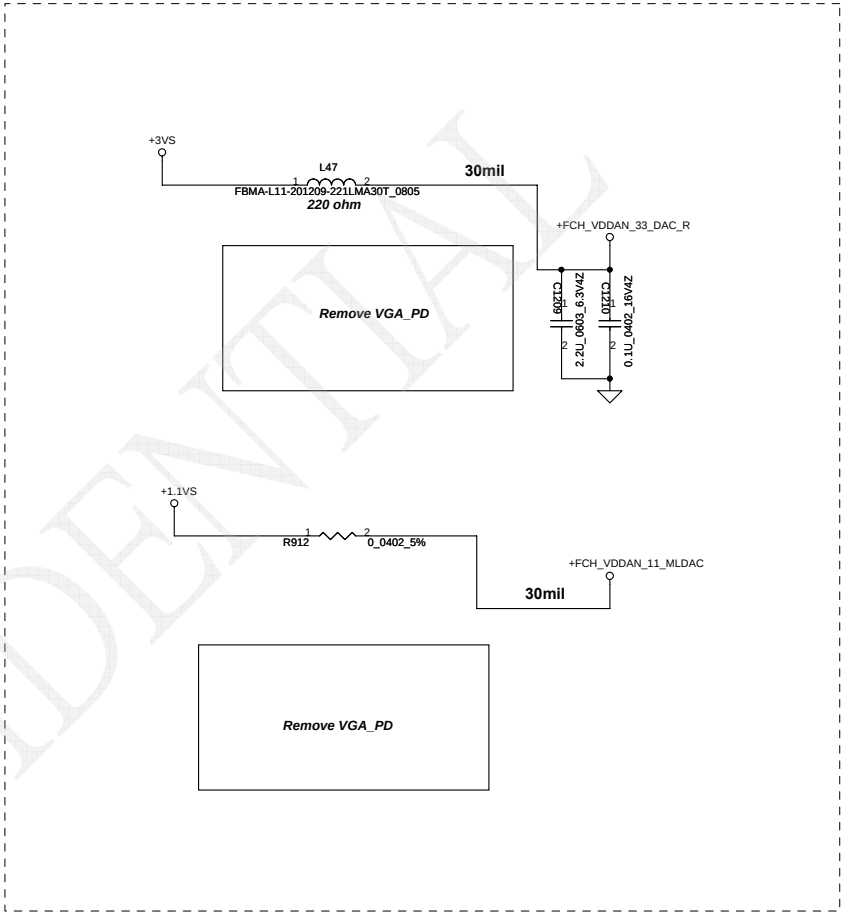


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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Compal Electronics, Inc.

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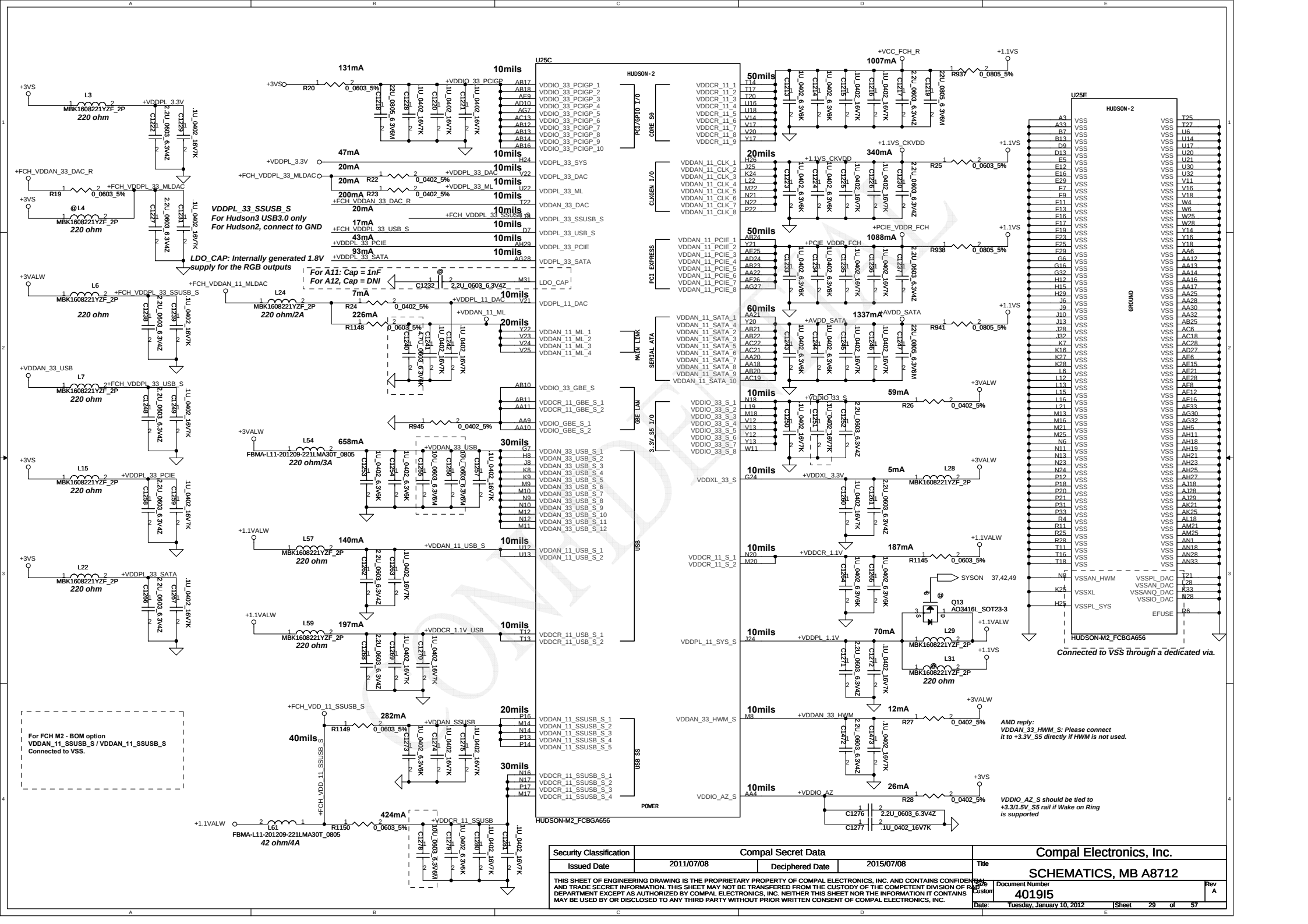

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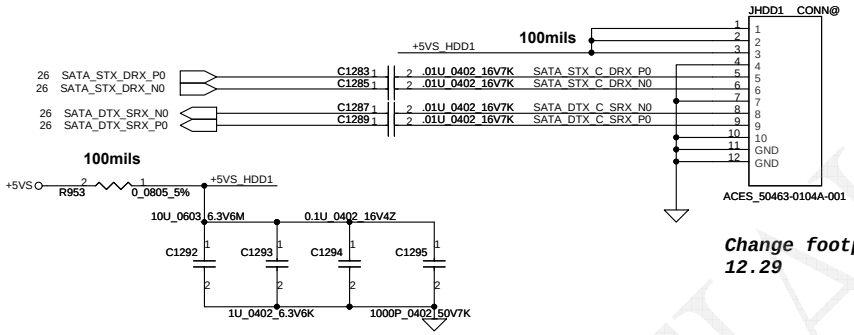
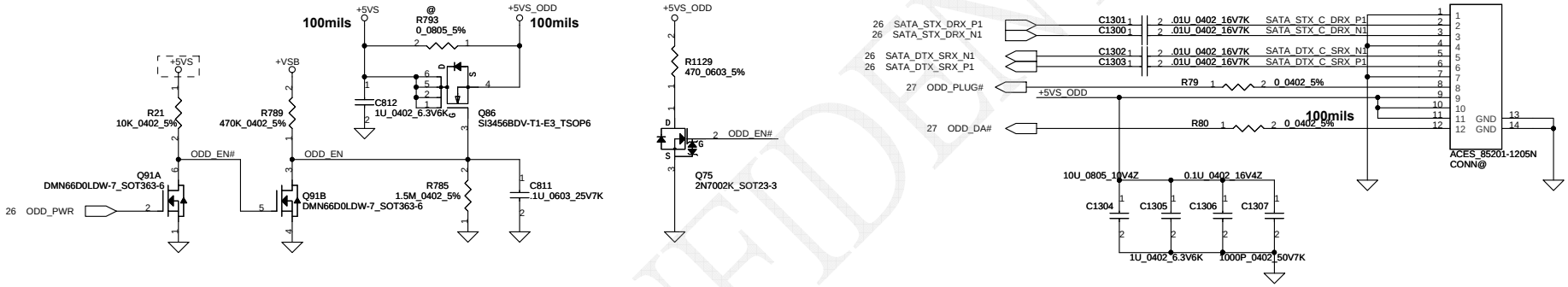
SATA HDD1 Conn.

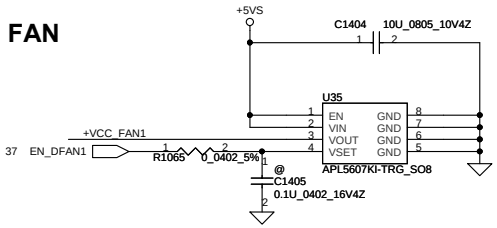


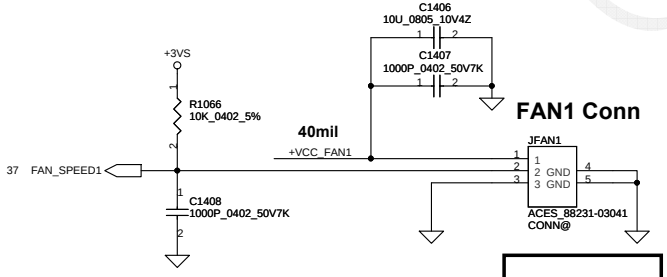
Change footprint to Starconn (PAD is bigger) 12.29

ODD conn



FAN

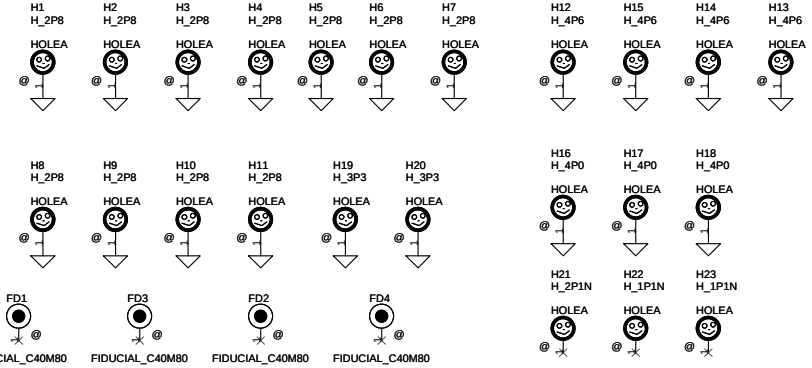




FAN1 Conn

<SI>Update JFAN1

Screw Hole



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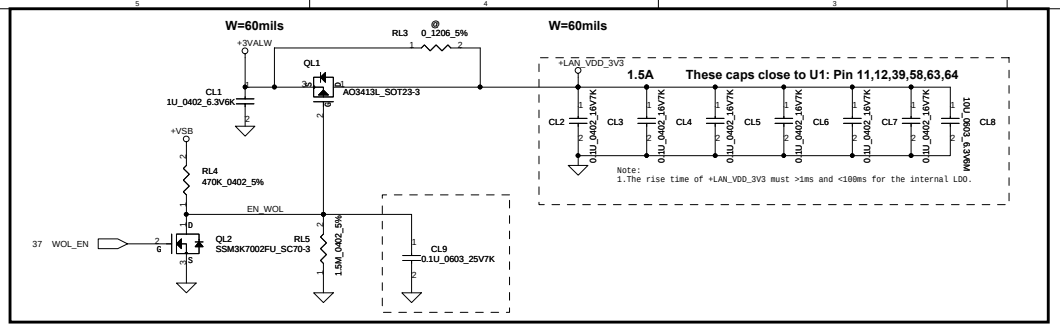
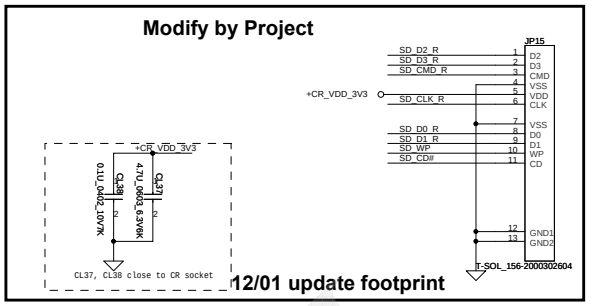
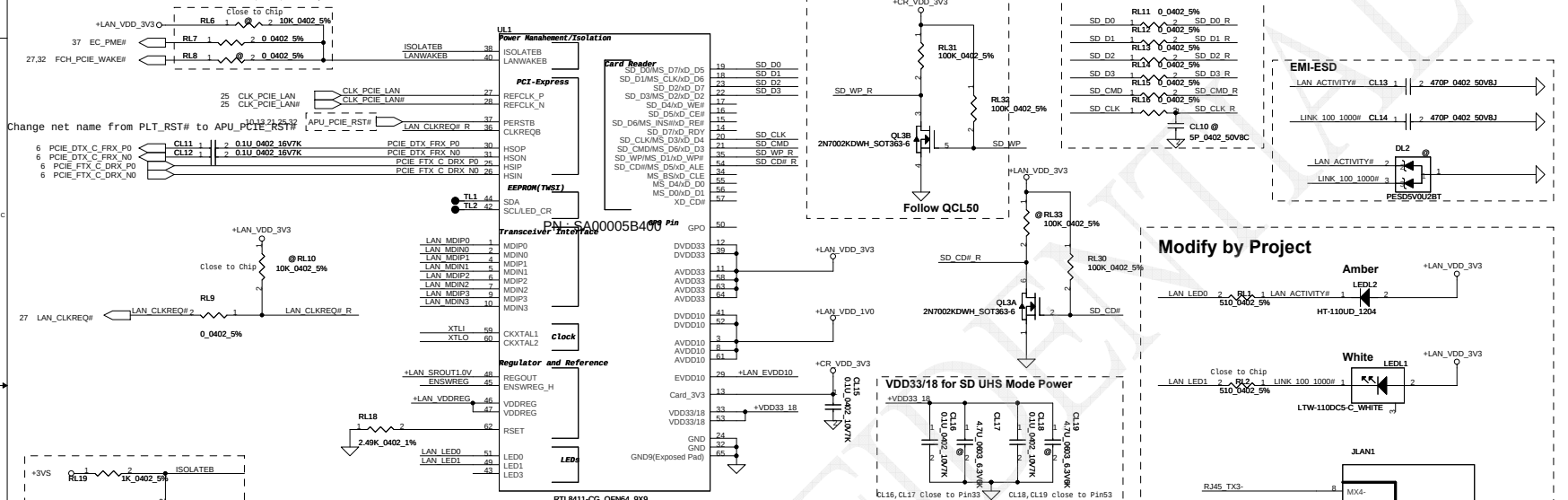
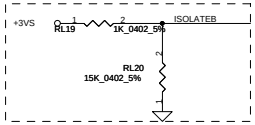
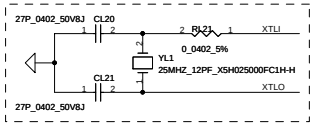


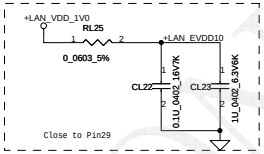


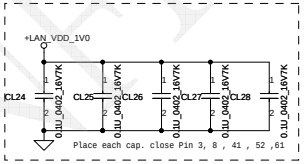
Need to check RL6,RL7,RL8 Option

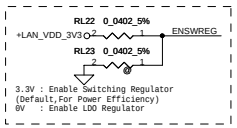


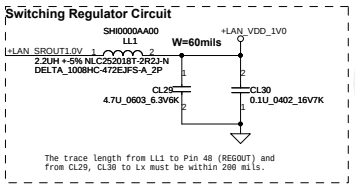


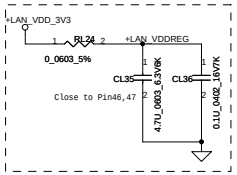


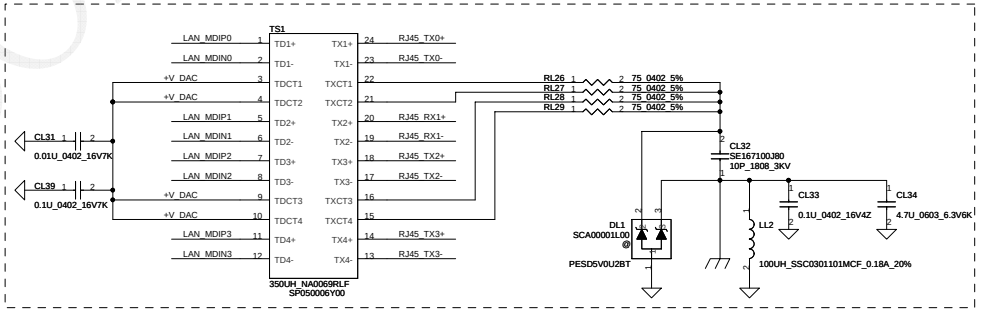












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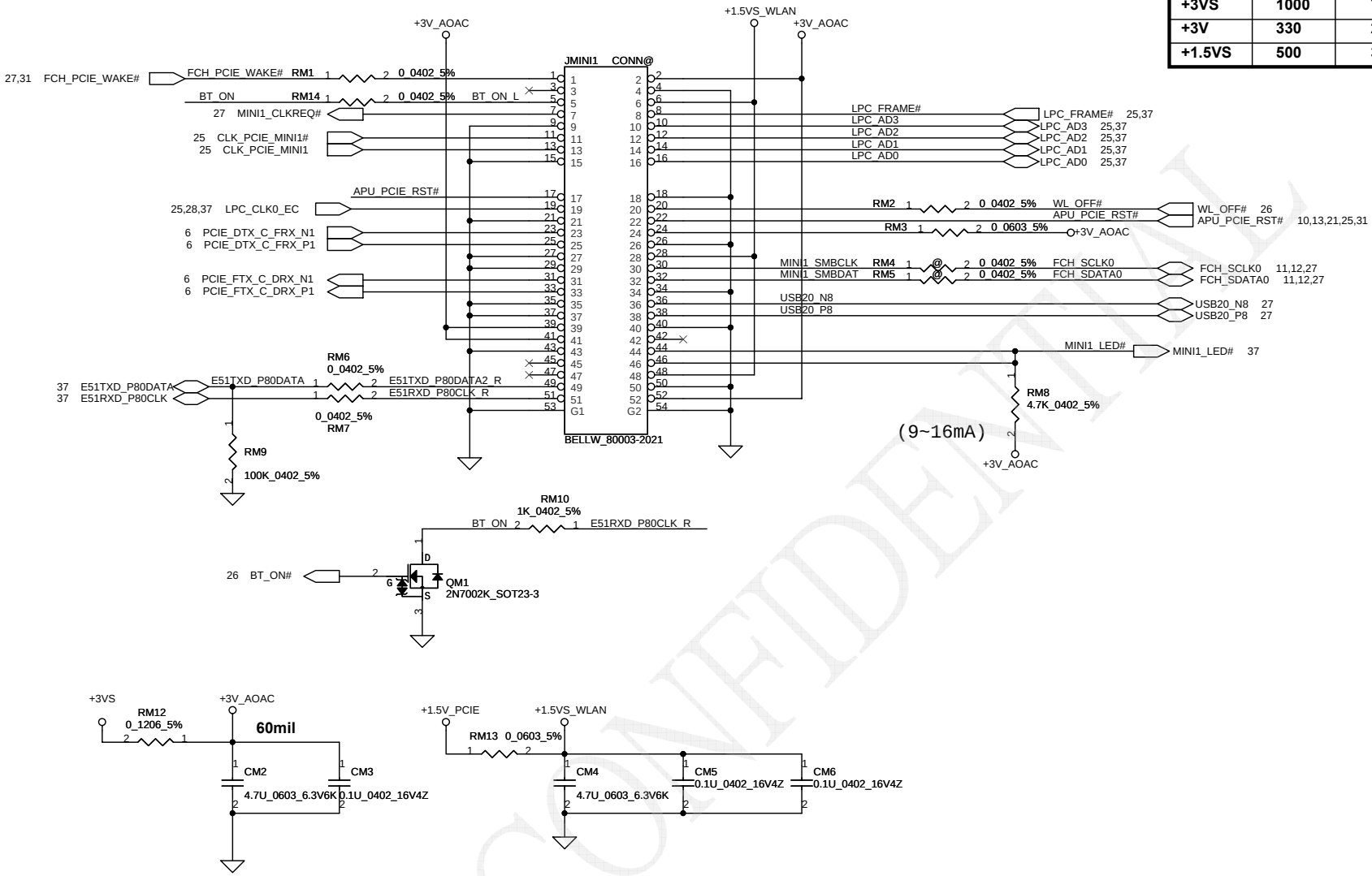
WLAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place AVDD ,PVDD,and DVDD cap close to Codec (UA5)

1/3 EMI add

Place C208 close to Codec

CA8,CA10 near UA5 PIN45
CA9,CA21 near UA5 PIN39

C209,C210,CA87,CA89 close to Codec (UA5)

PLACE CLOSE TO UA5 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

PLACE CLOSE TO UA5 PIN 14

External MIC
Combo jack
Headphone

SPK

12/5 Audio jack change to normal open, so remove MOS

Del AOAC

Close to Audio Codec (UA5)

Need confirmed.

12/7 Change to single package

RA53 need under or near UA5

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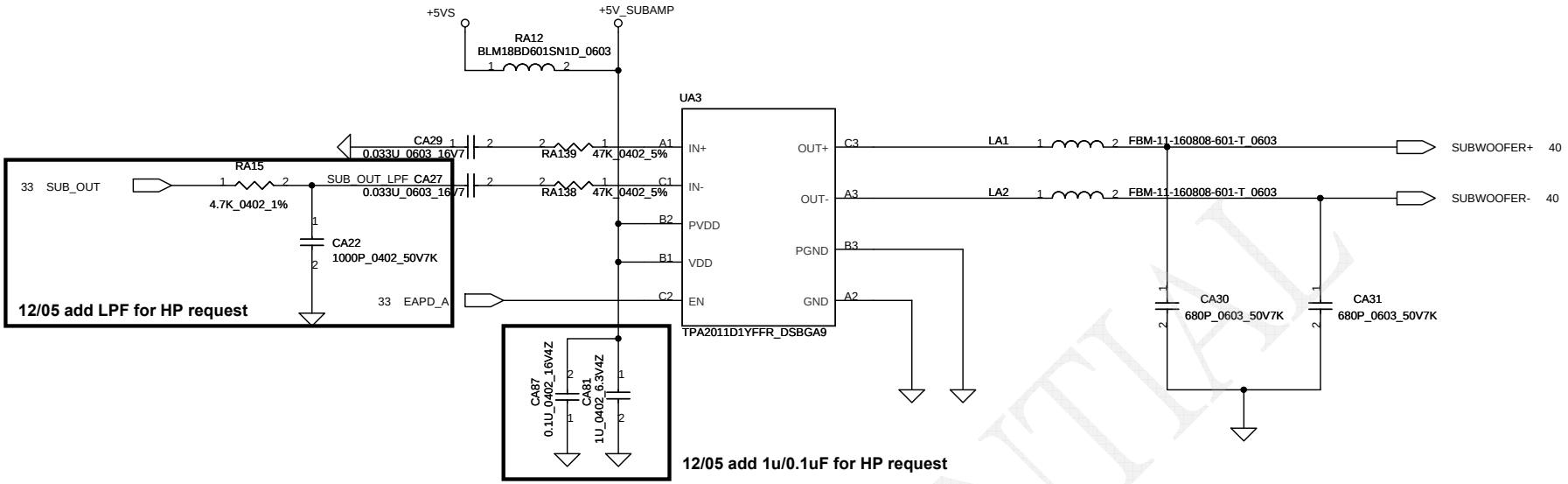

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8712

Size	Document Number	Rev
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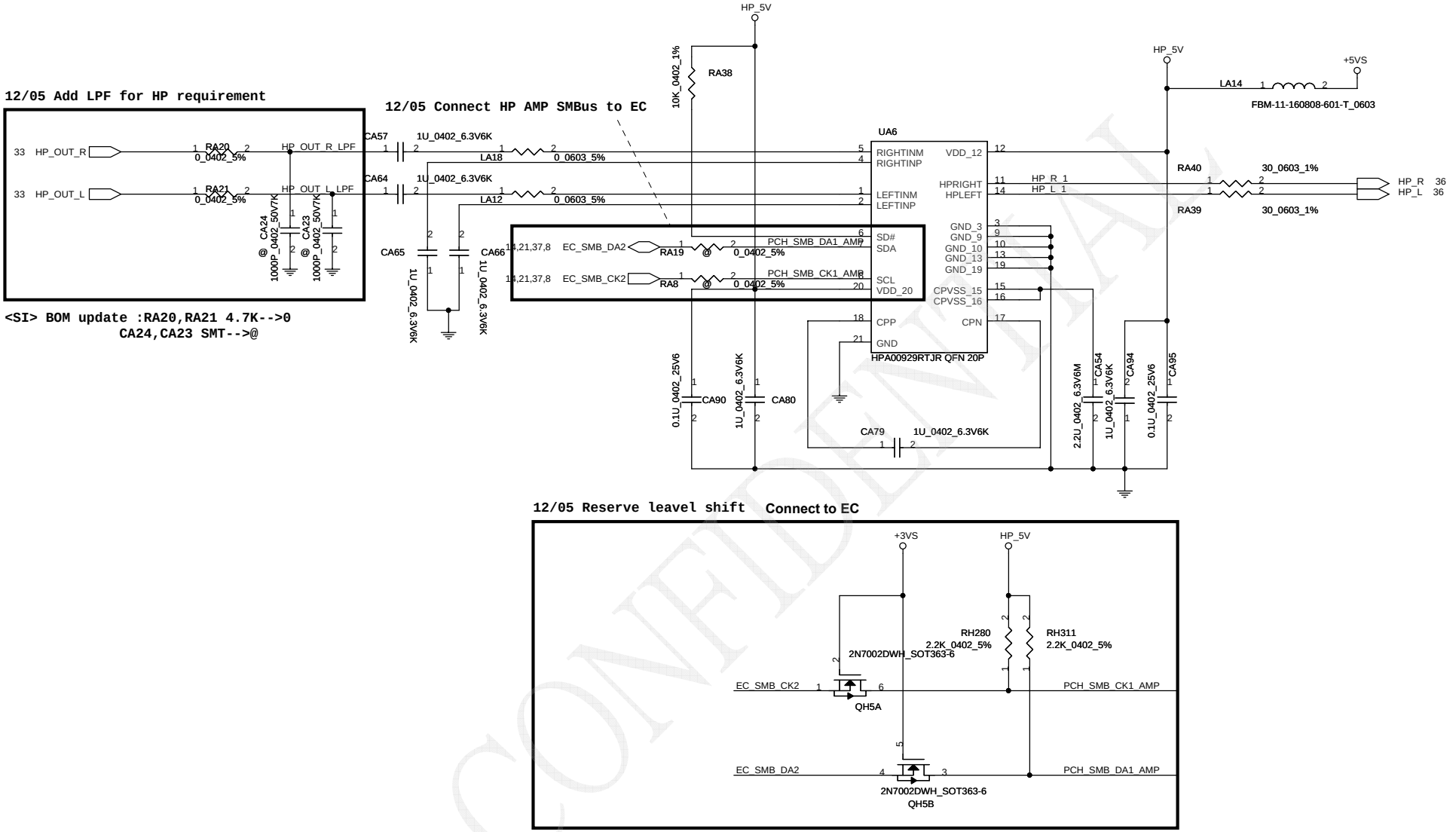
Headphone amplifier



Security Classification	Compal Secret Data		
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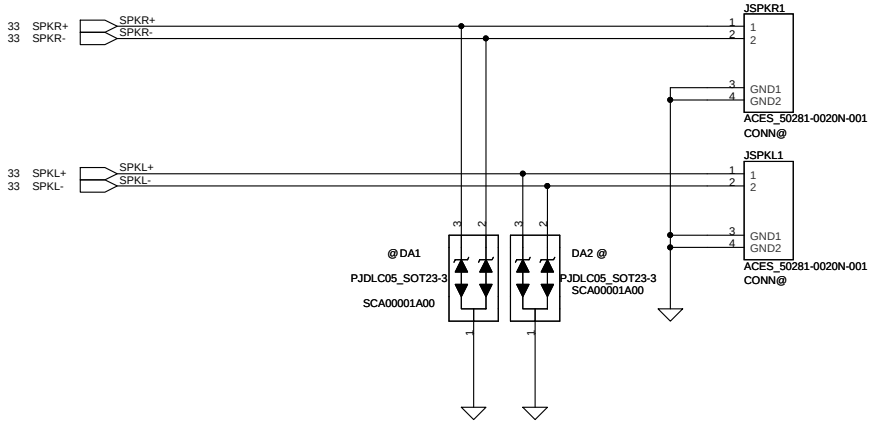
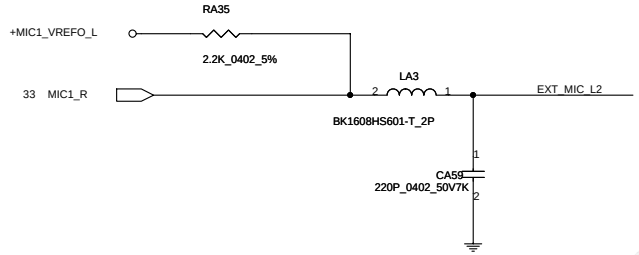
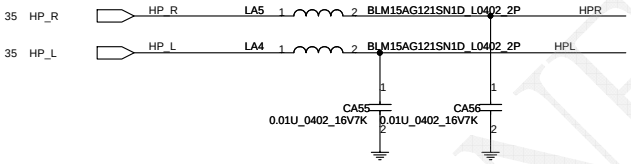
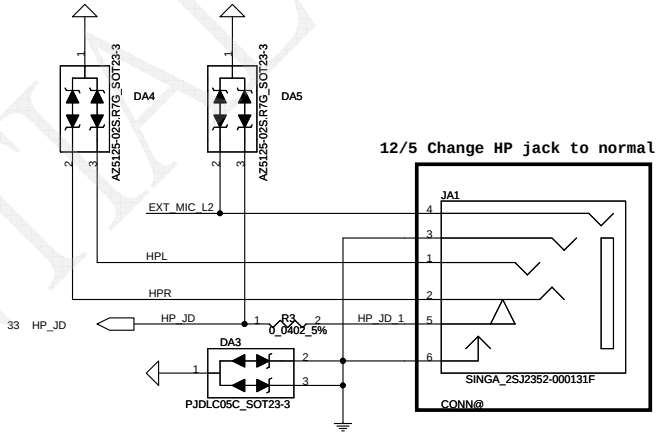
SPK conn

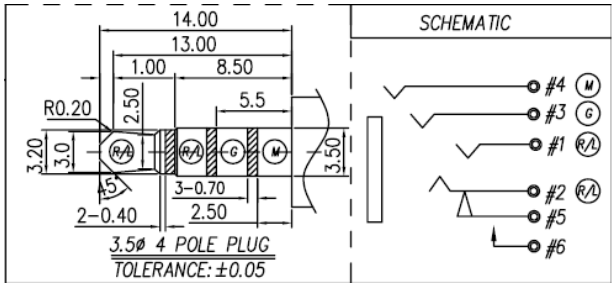








AGND



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Issued Date	2009/04/07	Deciphered Date	2012/10/21

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8712		
Size: Custom	Document Number: 401915		Rev: A
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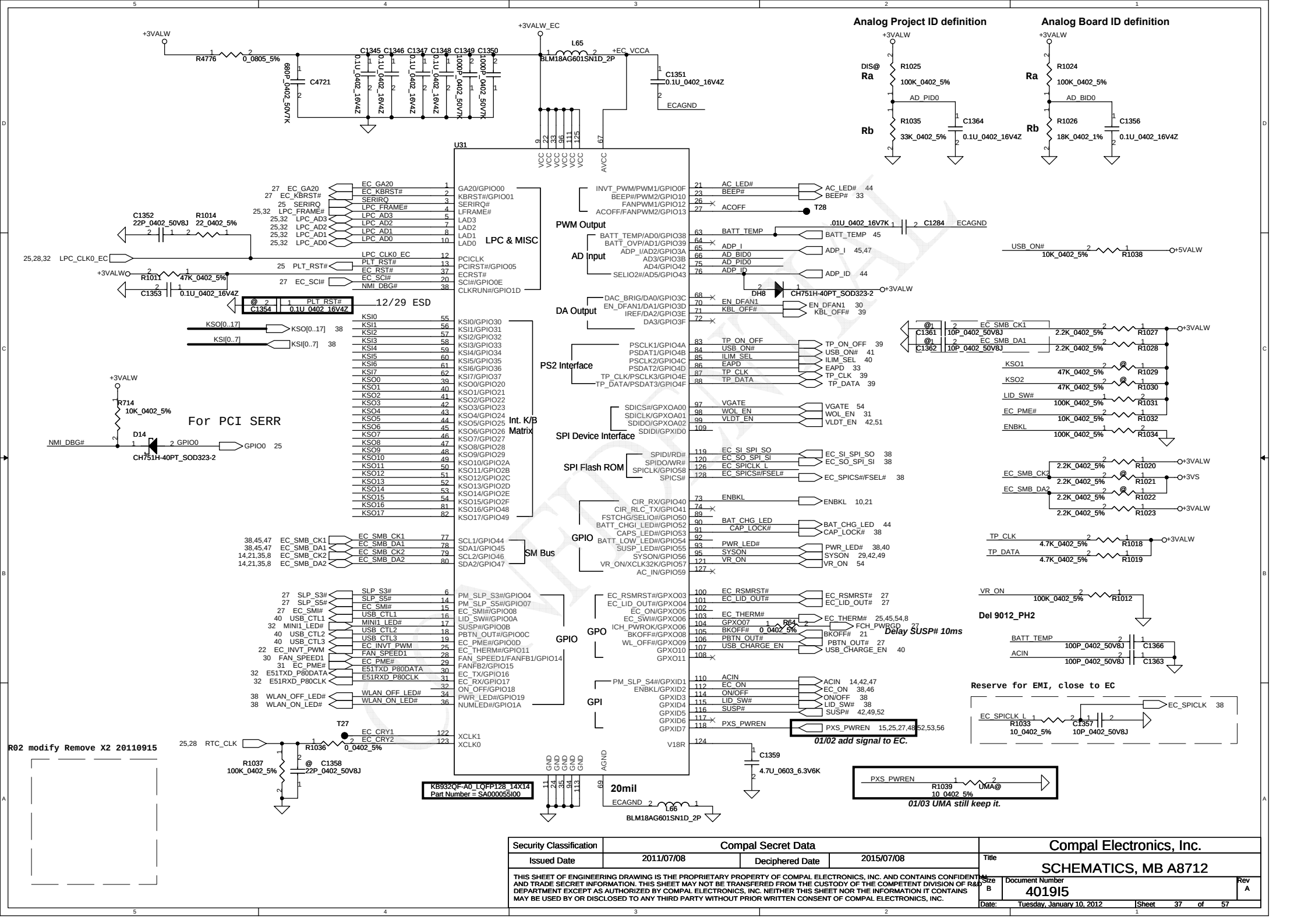

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Issued Date	2011/07/08	Deciphered Date	2015/07/08

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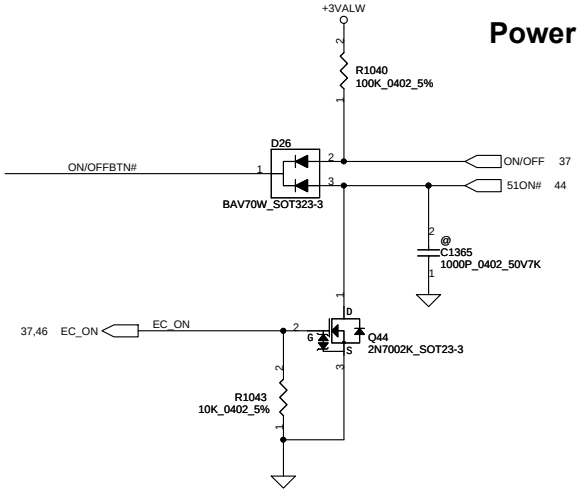
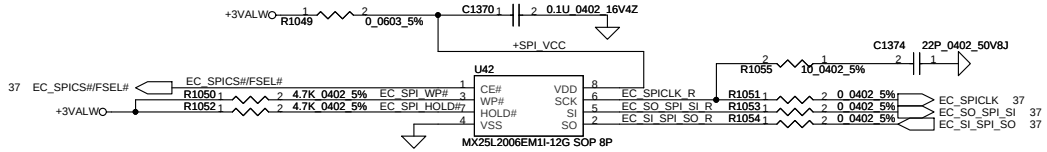
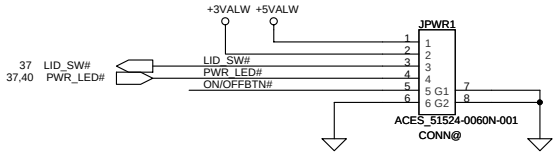
Power Button



EC BIOS ROM

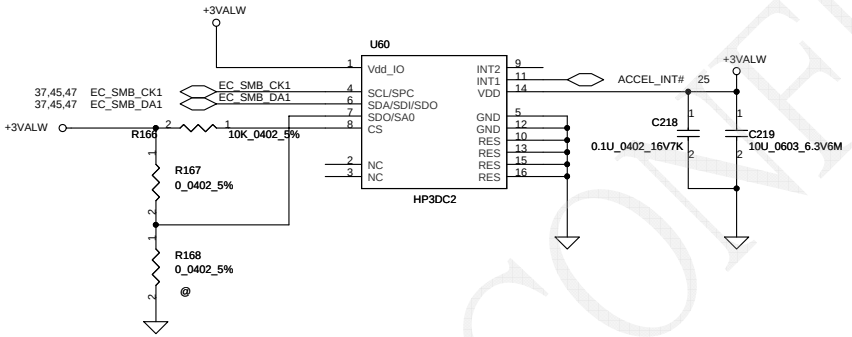


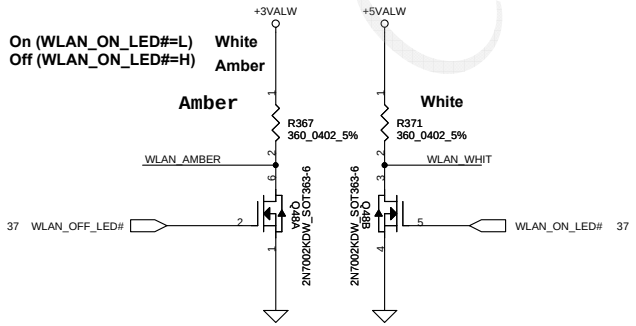
POWER/B

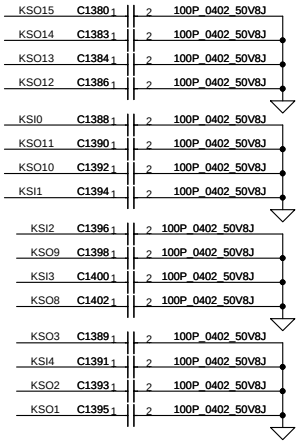


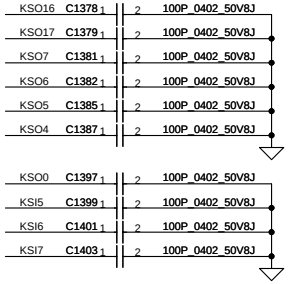
KB conn

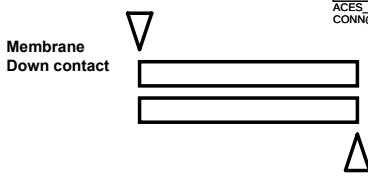
ACCELEROMETER











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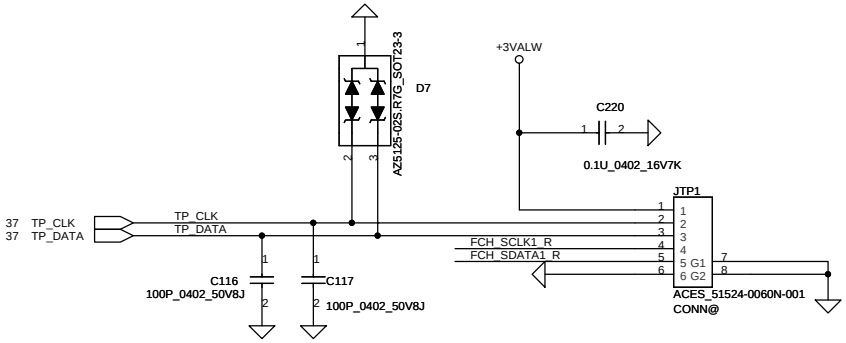
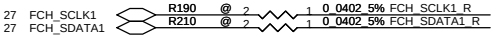
TP Conn

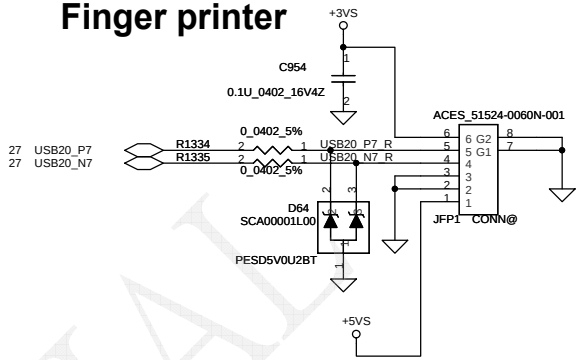




For multi-touch function

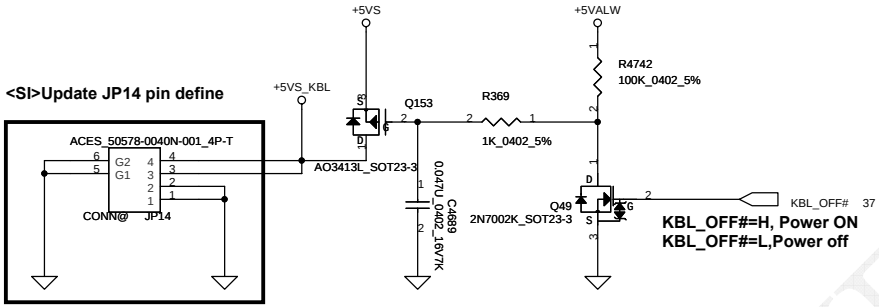
Finger printer

12/06 Change FPR pin define

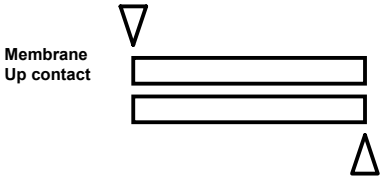


Keyboard backlight Conn

<SI>Update JP14 pin define

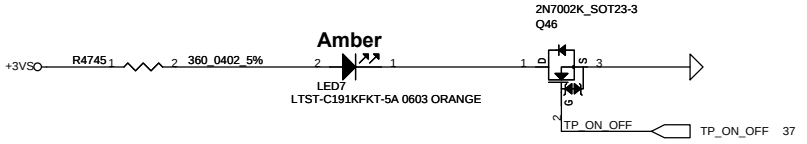


12/06 Change keyboard back light conn



The JP14 pin define must opposite

T/P On/Off LED



EC pin

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

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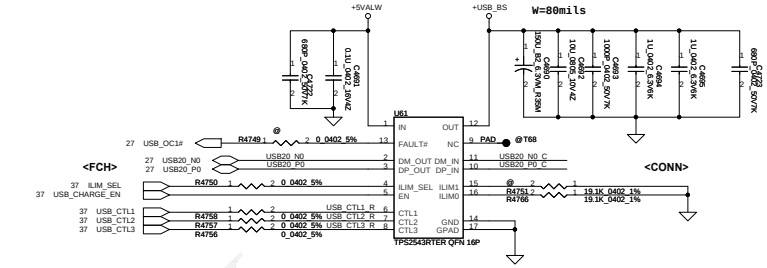
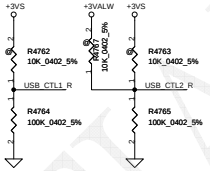
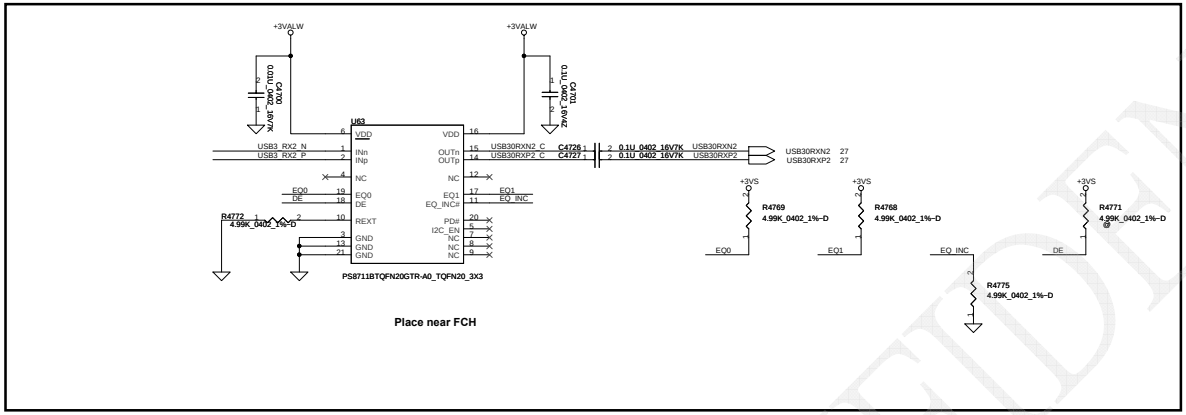
USB Charger

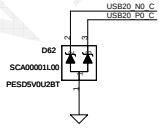


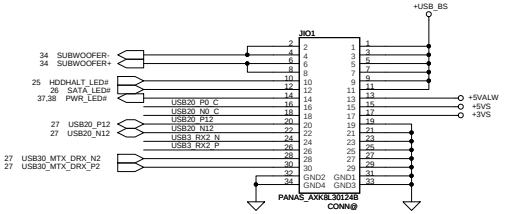


State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	1	0	0	1	1

USB3.0 Repeater







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Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title	SCHEMATICS, MB A8712		
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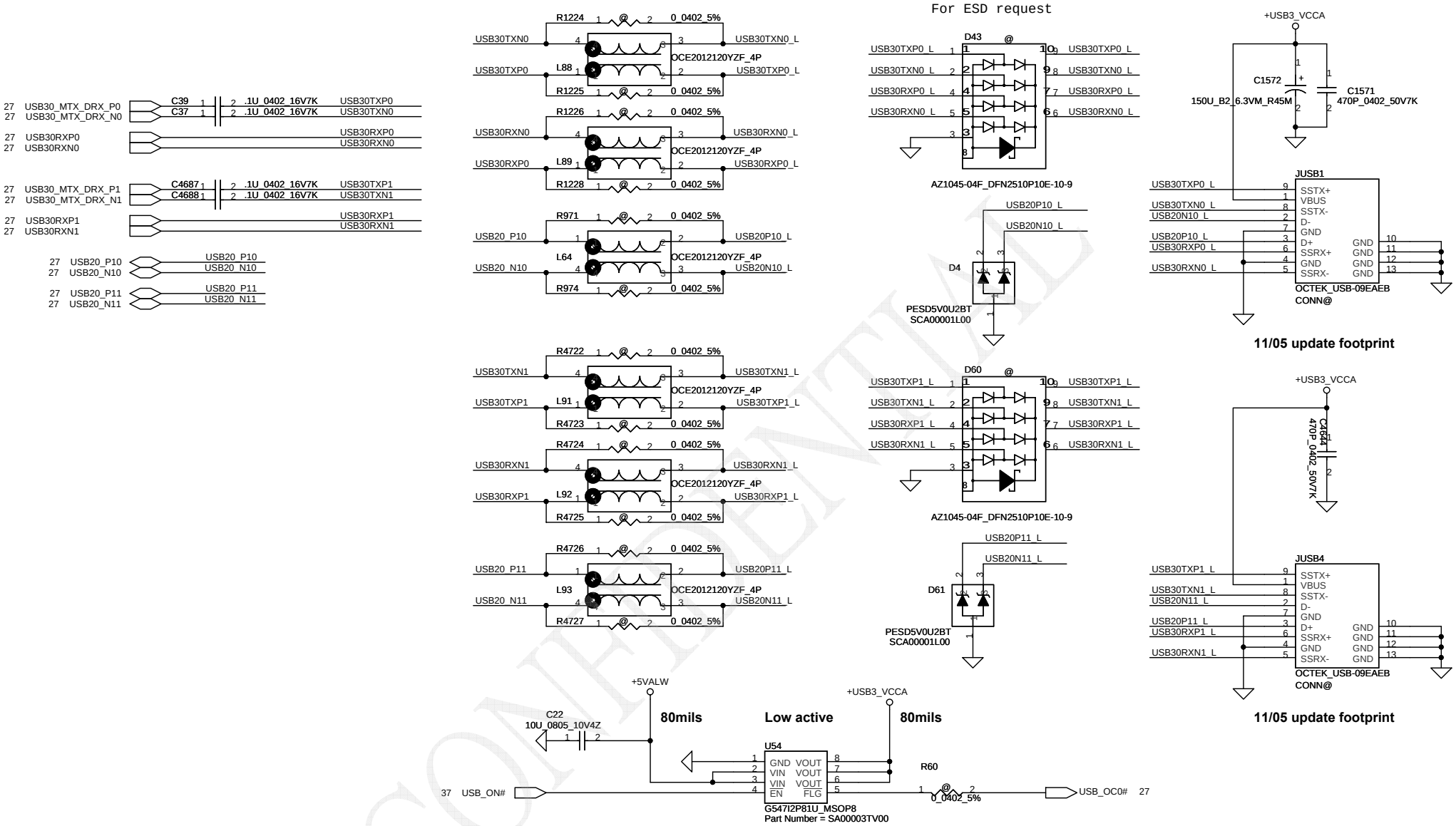

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

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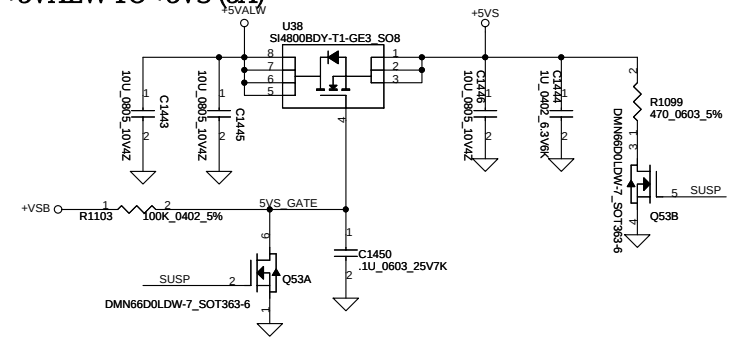
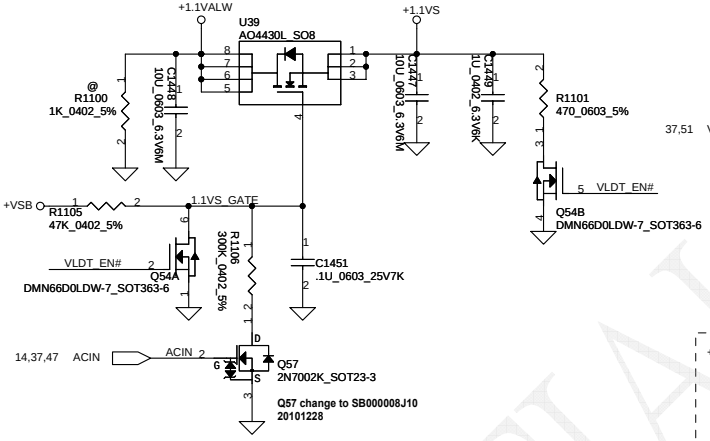
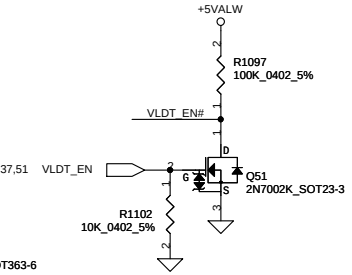
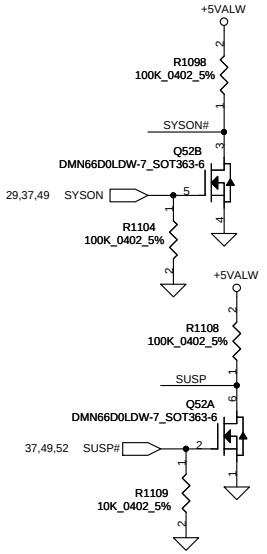
+5VALW TO +5VS (5A)

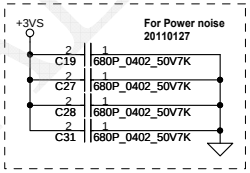


+1.1VALW TO +1.1VS (1.1A)

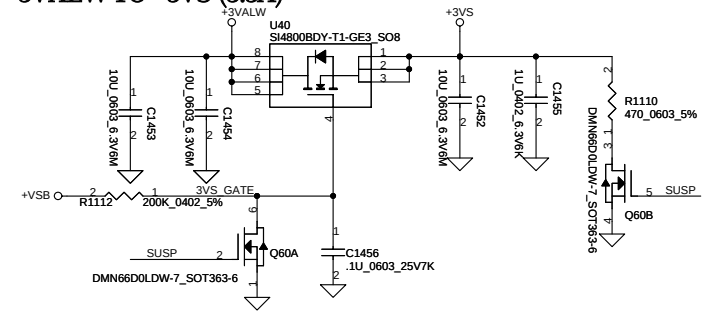


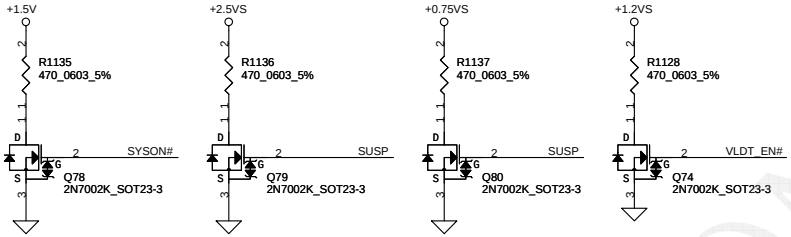






+3VALW TO +3VS (3.3A)





Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

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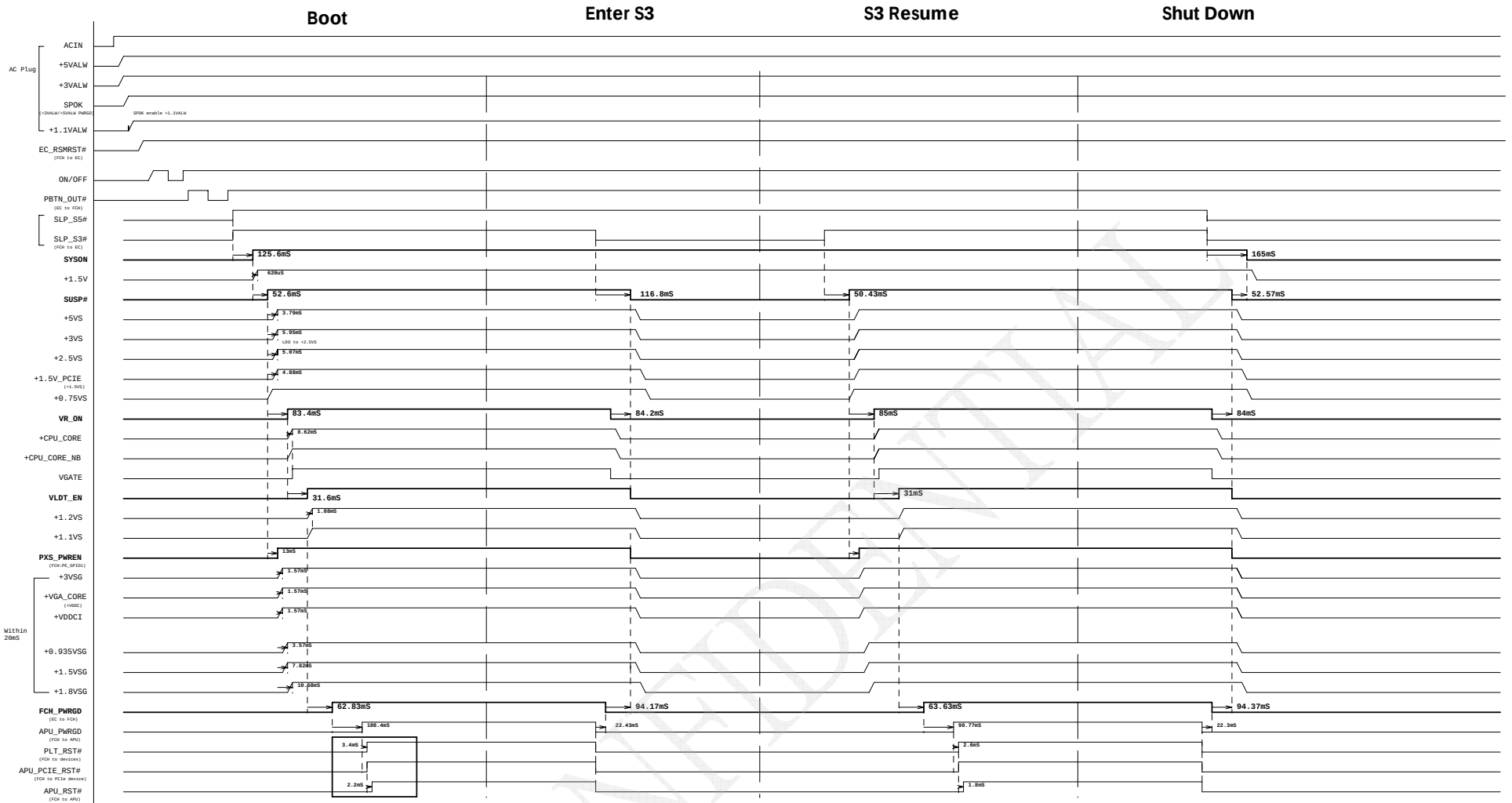

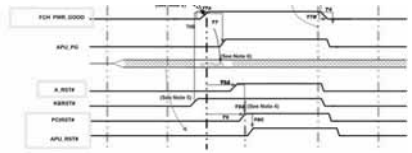

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.		
Title: SCHEMATICS, MB A8712		
Size: B	Document Number: 4019I5	Rev: A
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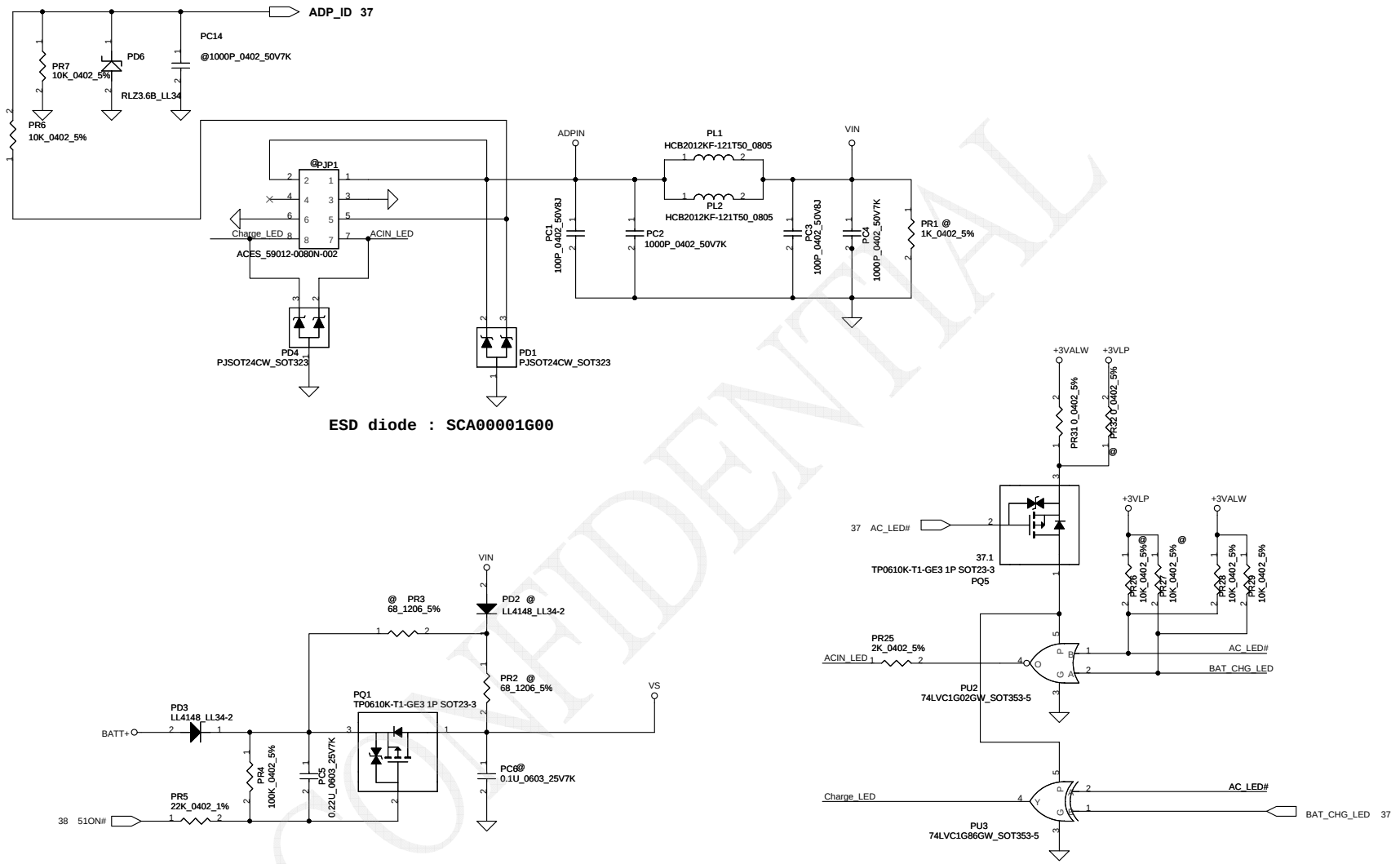

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title: SCHEMATICS, MB A8712			
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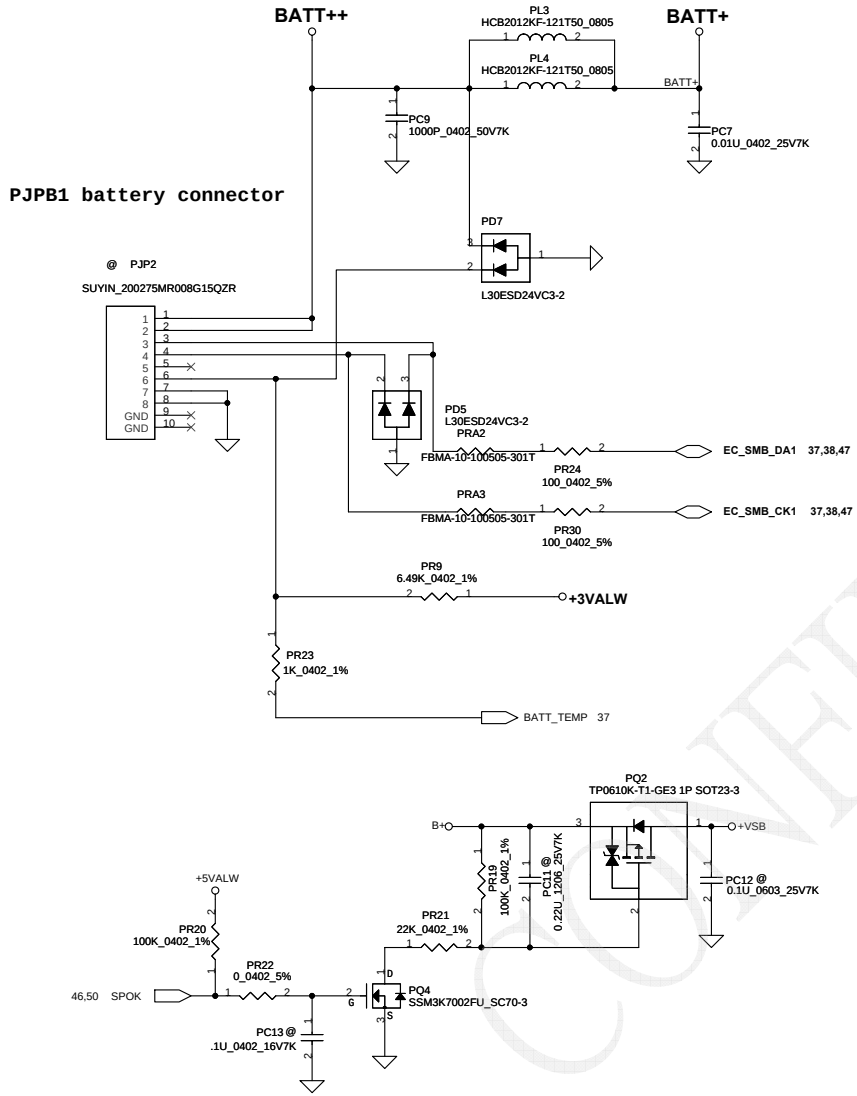
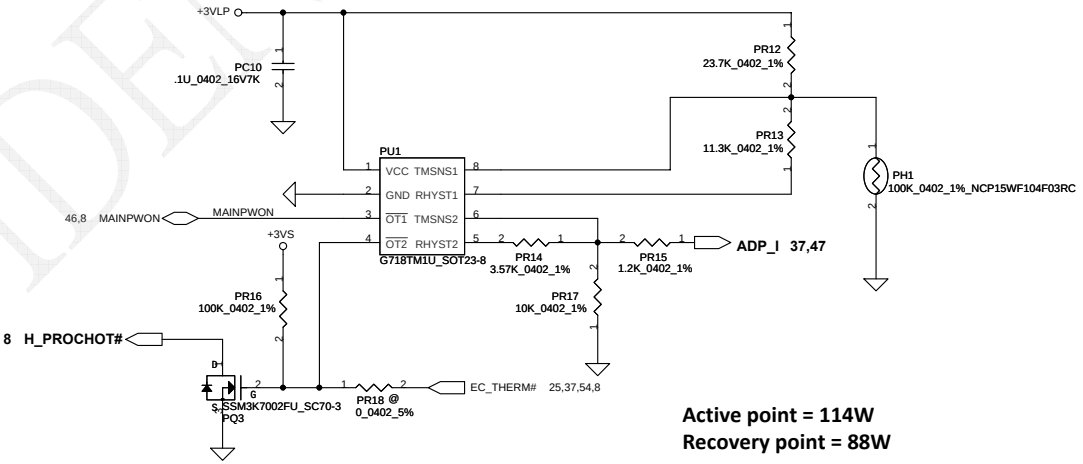
PJPB1 battery connector



For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 56 +-3 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



Active point = 114W
Recovery point = 88W

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
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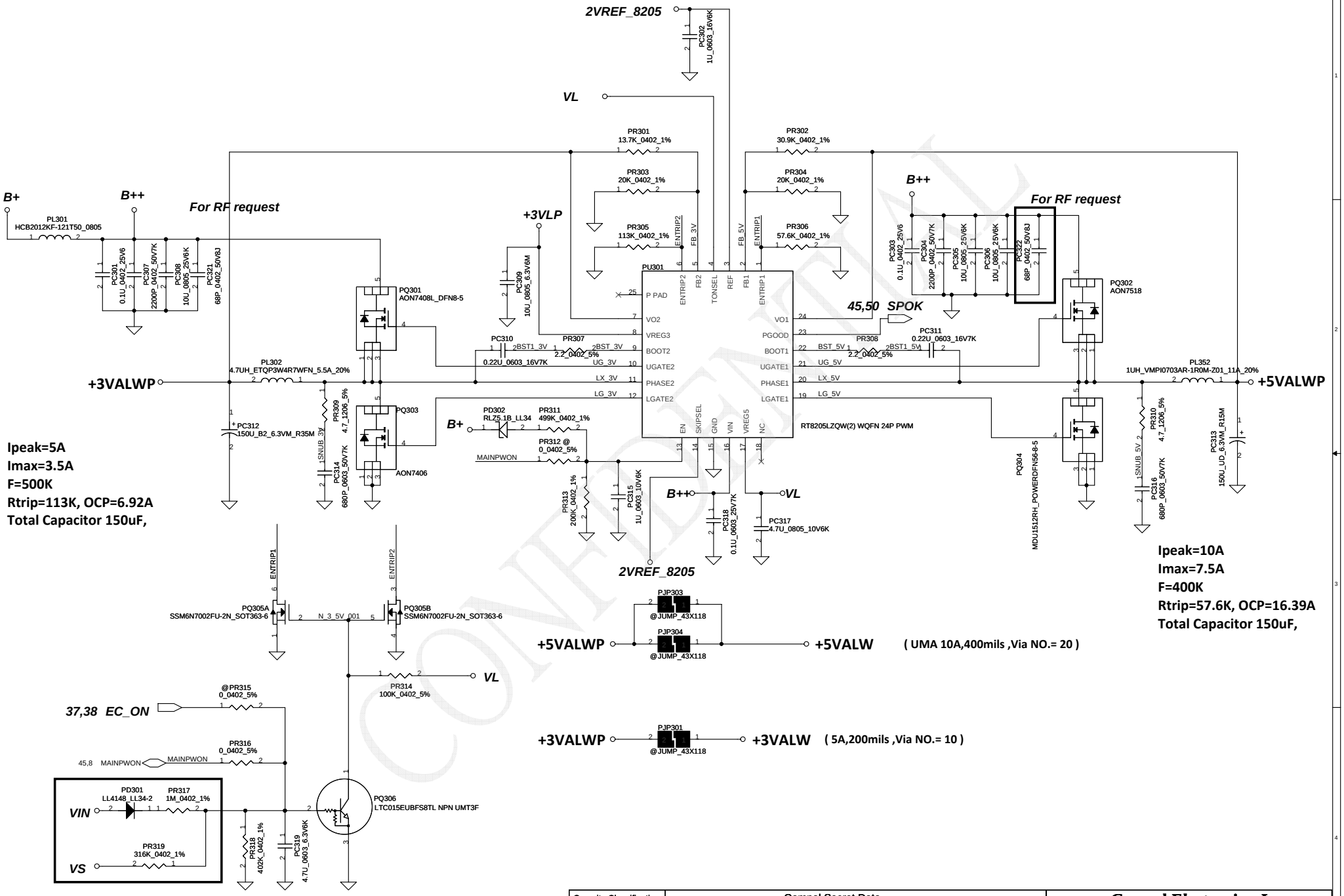

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title: SCHEMATICS, MB A8712			
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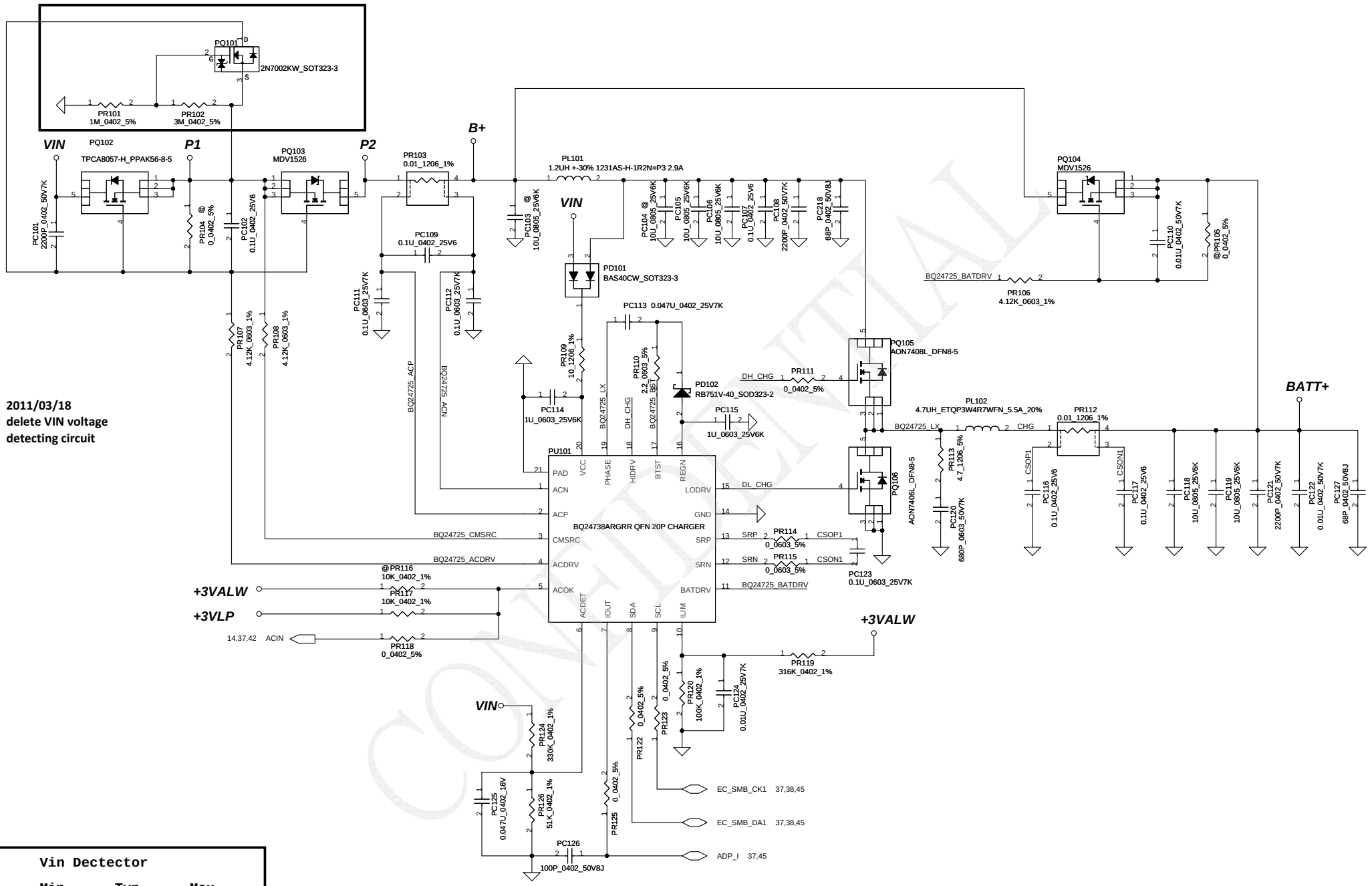
for reverse input protection



2011/03/18
delete VIN voltage
detecting circuit

Vin Dectector

	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

ILIM and external DPM
4.36A

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.	
Title	SCHEMATICS, MB A8712
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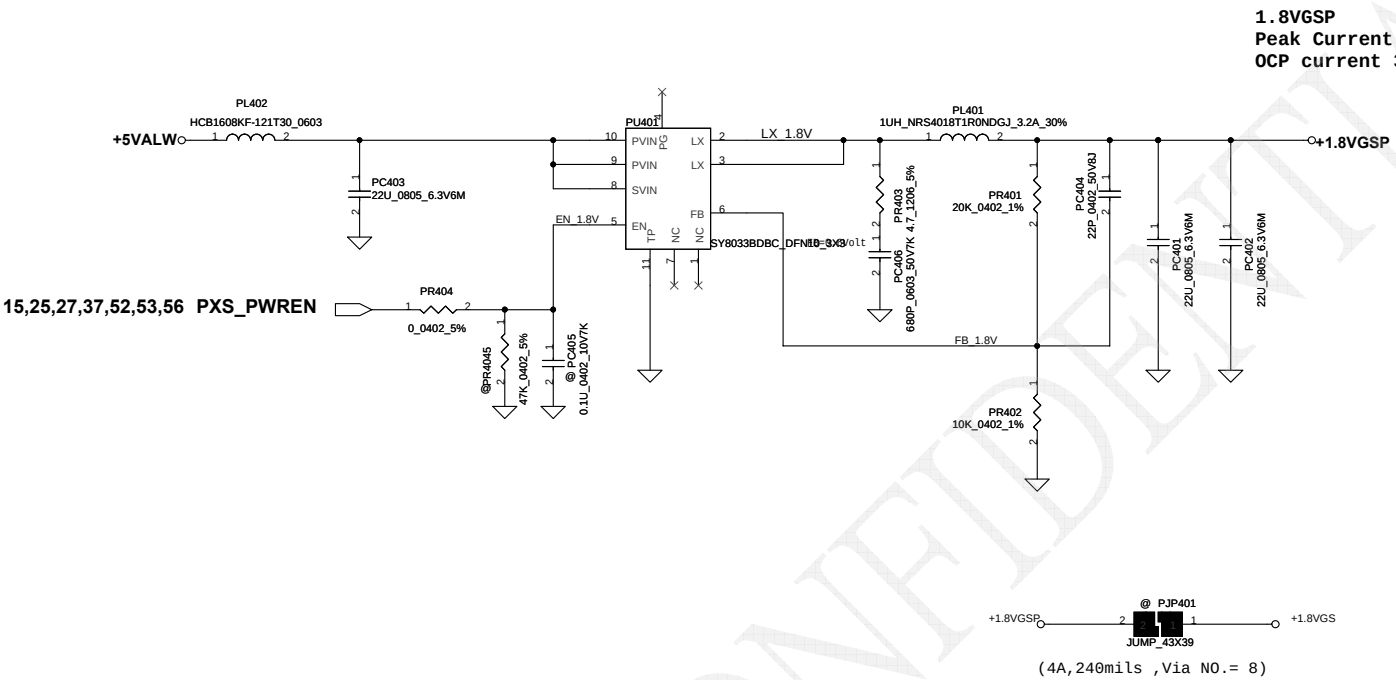

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	Title: SCHEMATICS, MB A8712

Size	Document Number		Rev
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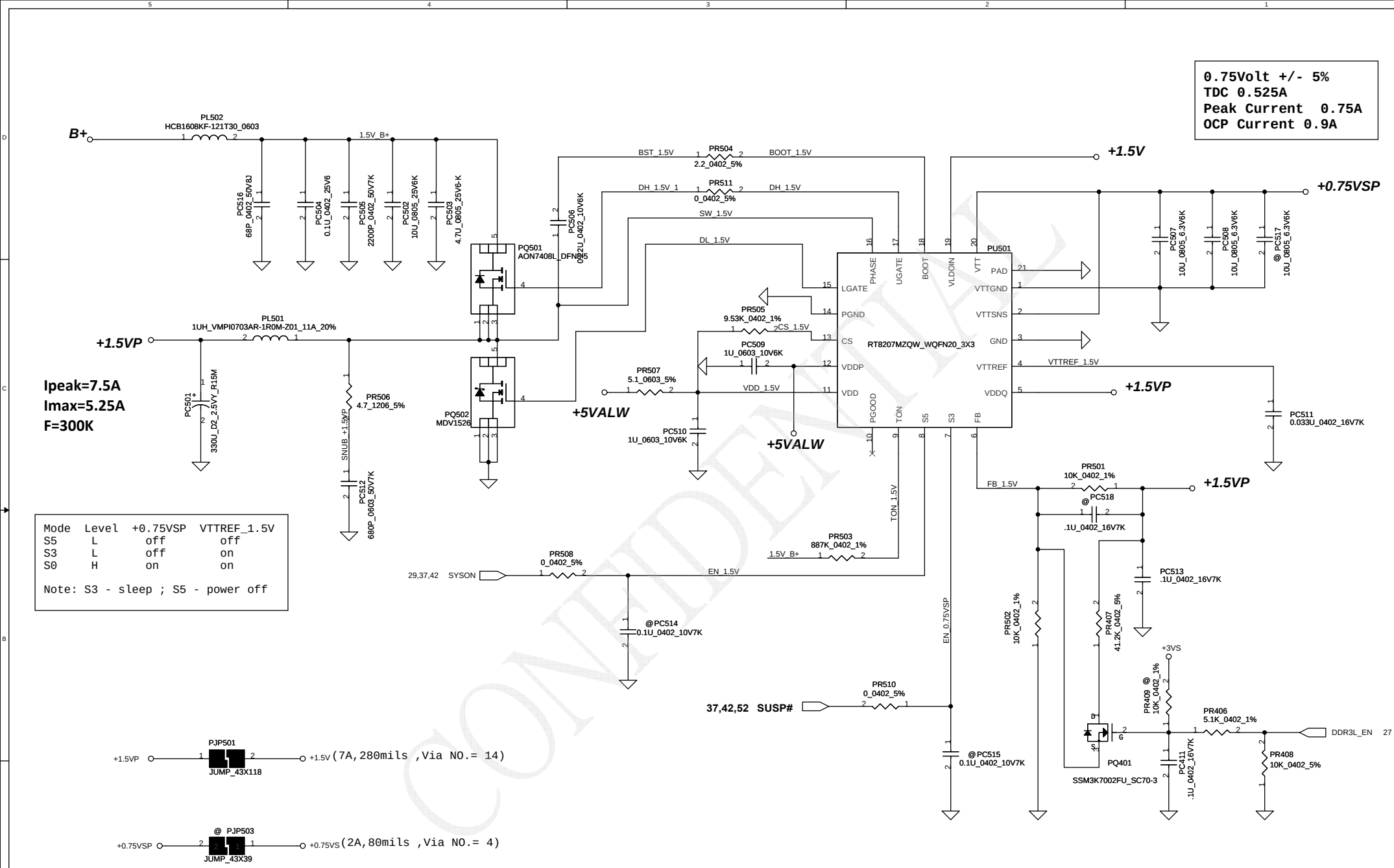

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8712

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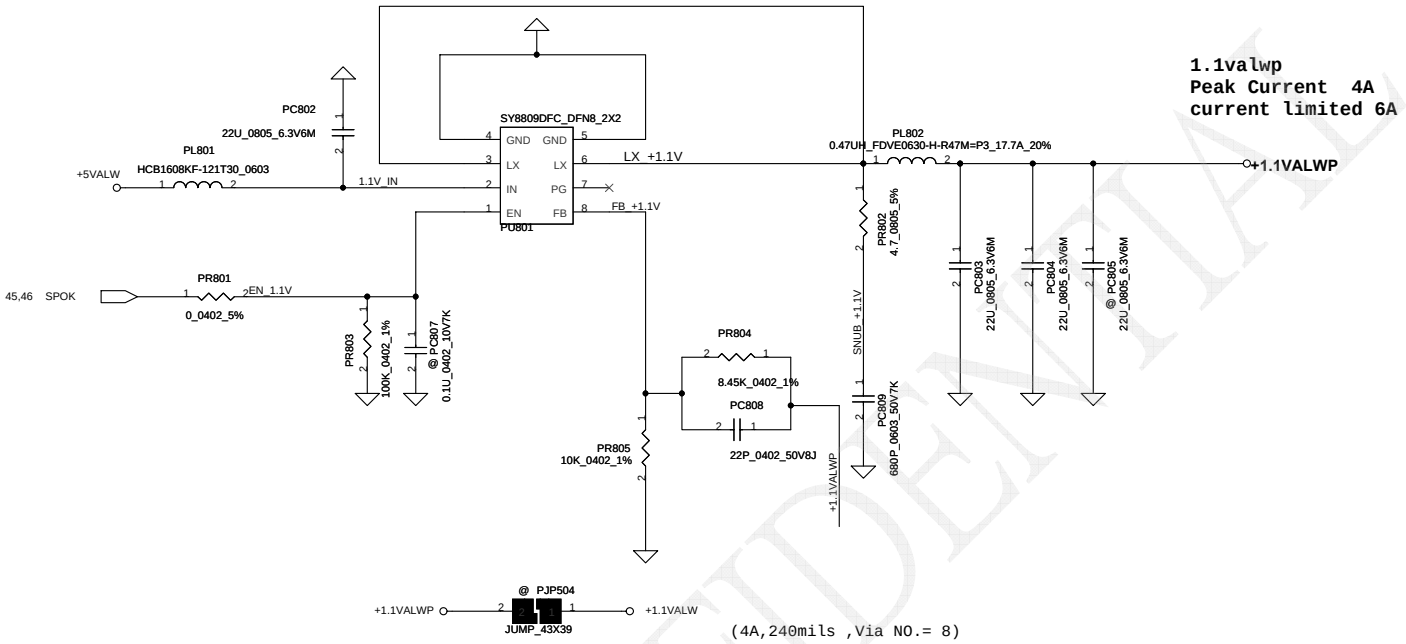

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	Title: SCHEMATICS, MB A8712

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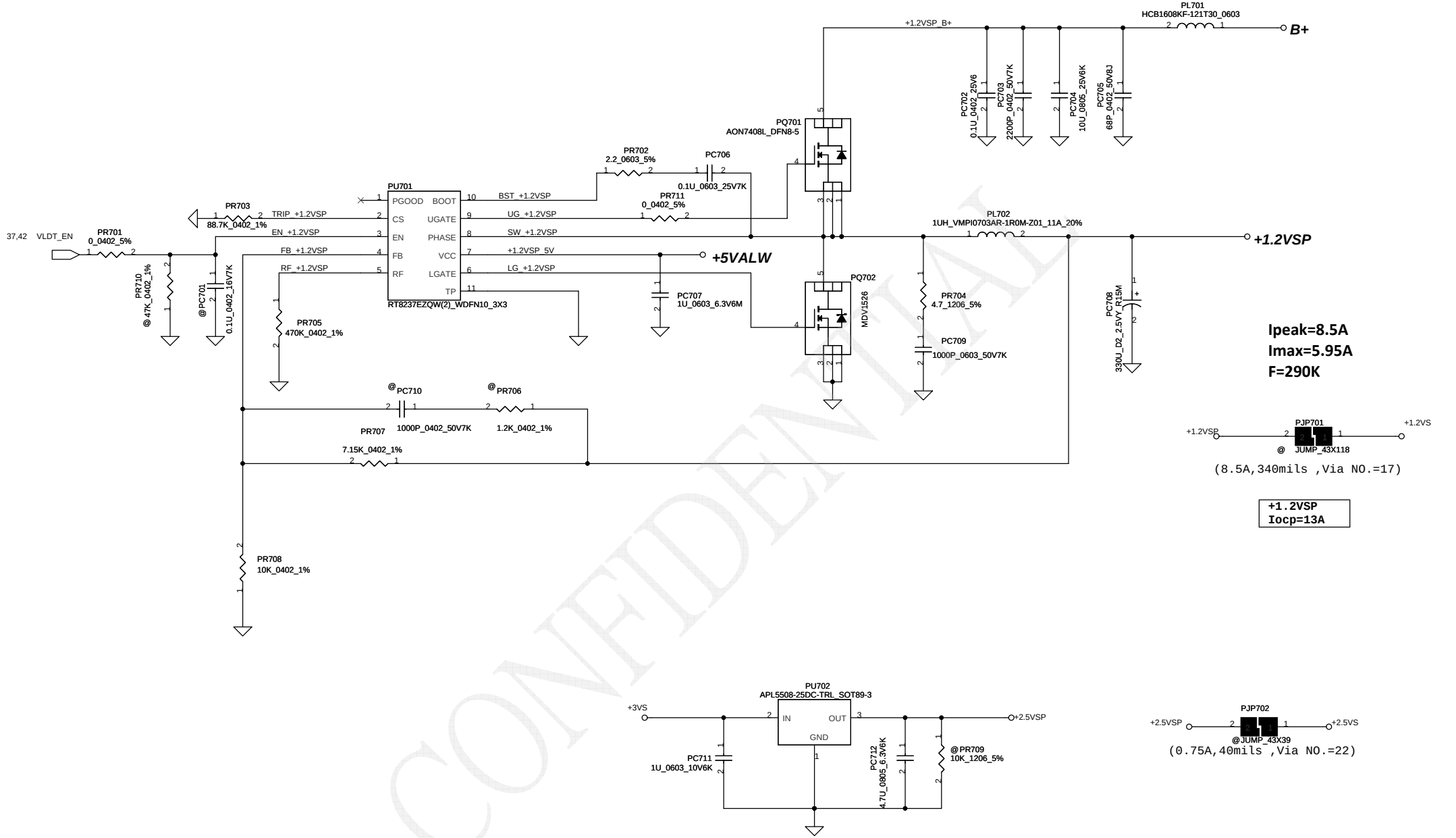

Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8712		
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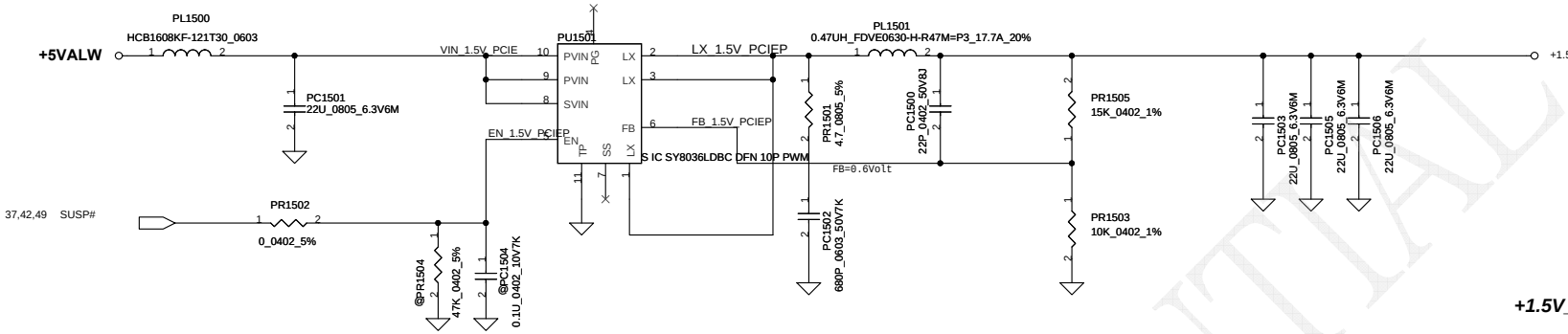
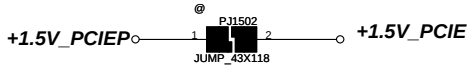
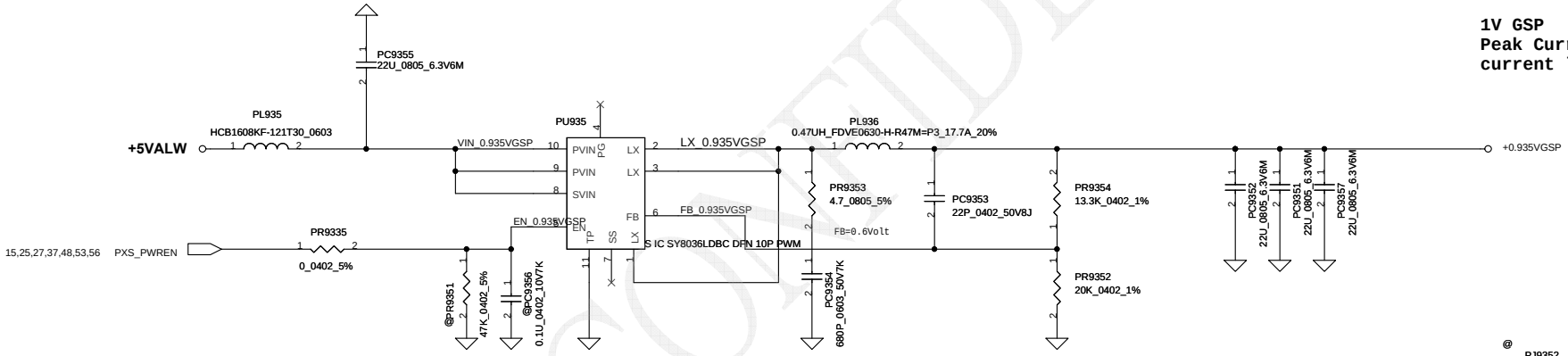
1.5VPCIEP
Peak Current 6A
OCP current 6A

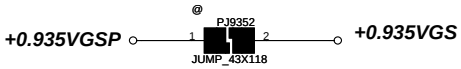




(6A,240mils ,Via NO.= 12)

1V GSP
Peak Current 4.2A
current limited 6A





(4.2A,460mils ,Via NO.= 8.4)

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.			
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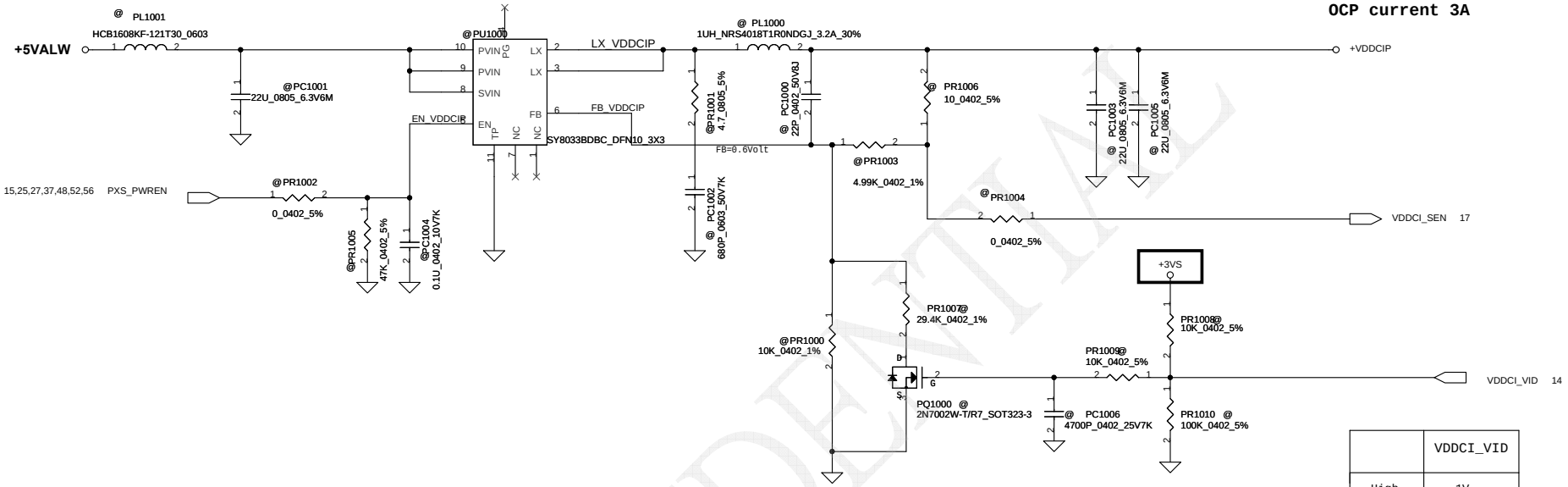
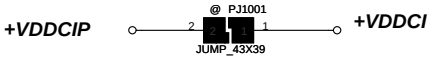
+VDDCI
TDC 2.2A

OCP current 3A



	VDDCI_VID
High	1V
Low	0.9V



(2.2A,100mils ,Via NO.= 5)

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8712**

Size: C | Document Number: **4019I5** | Rev: A

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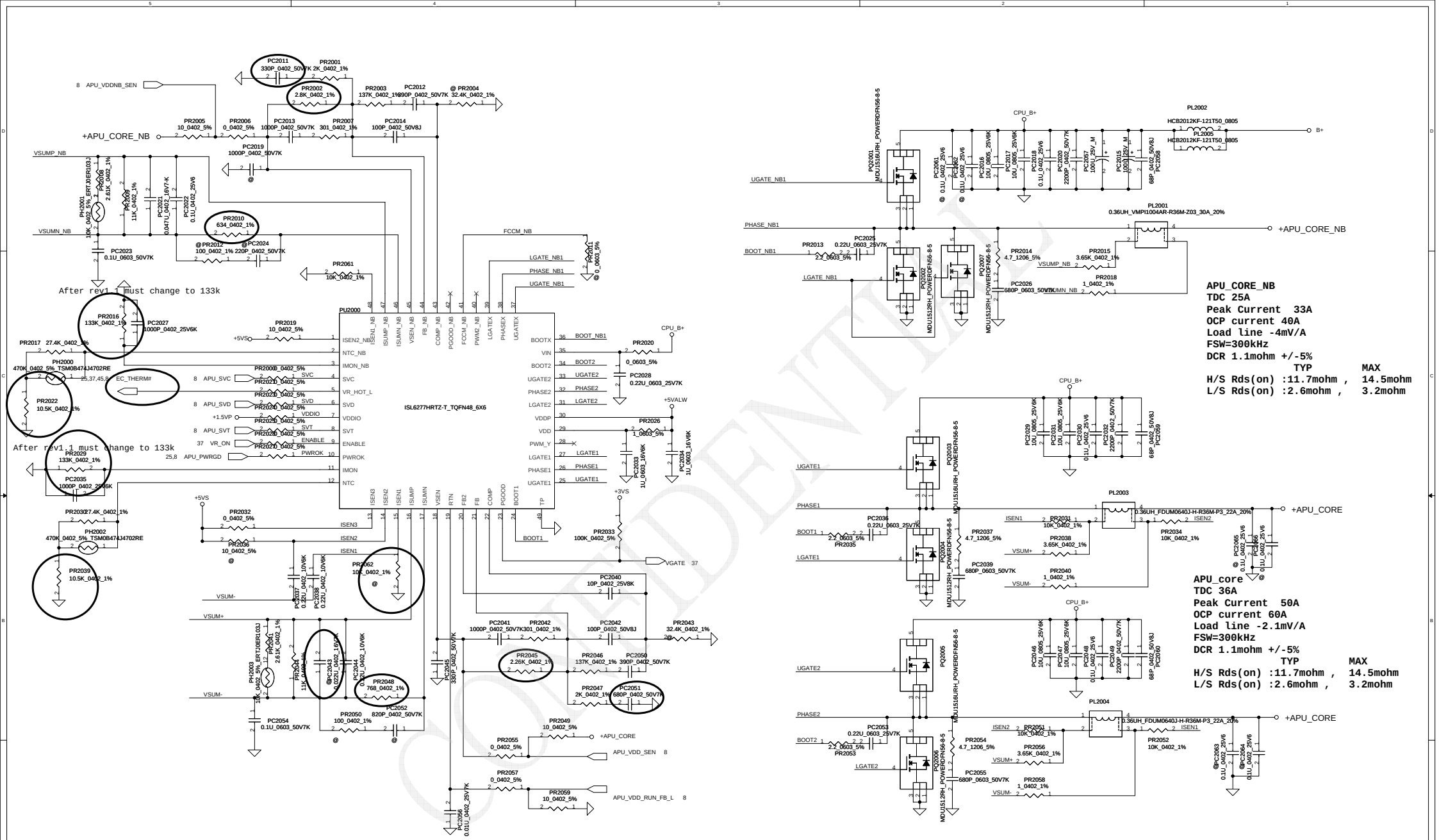

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8712		
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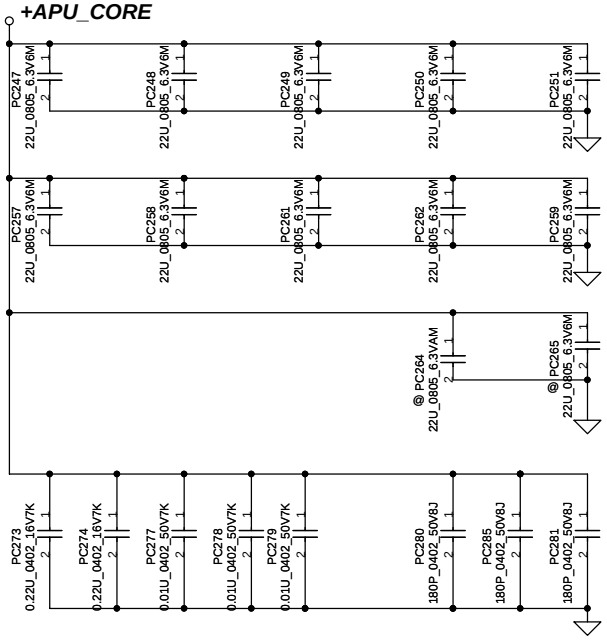
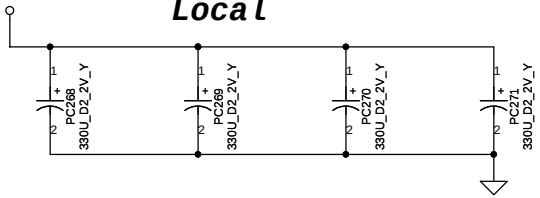
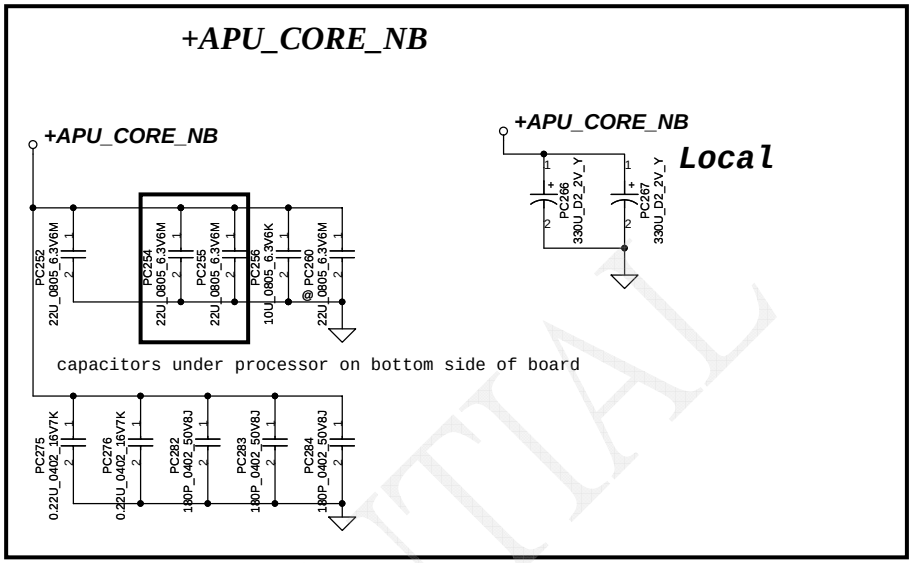
+APU_CORE

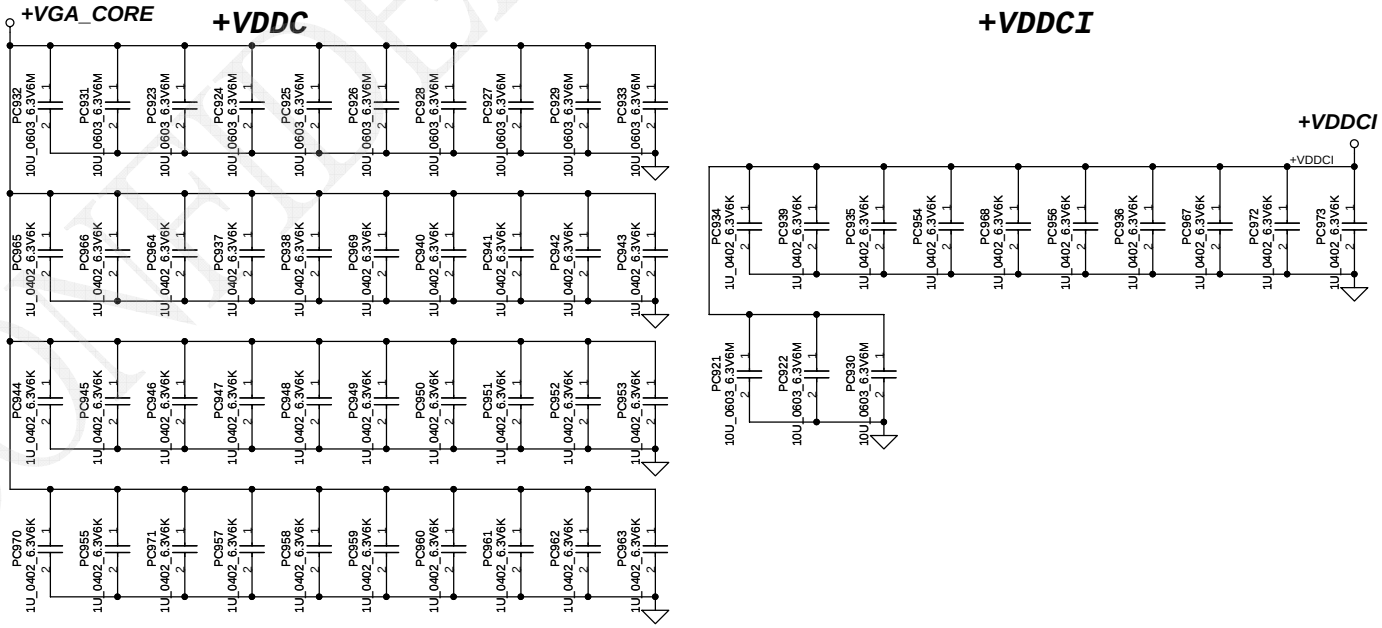




+APU_CORE_NB



+VGA_CORE



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.		
Title: SCHEMATICS, MB A8712		
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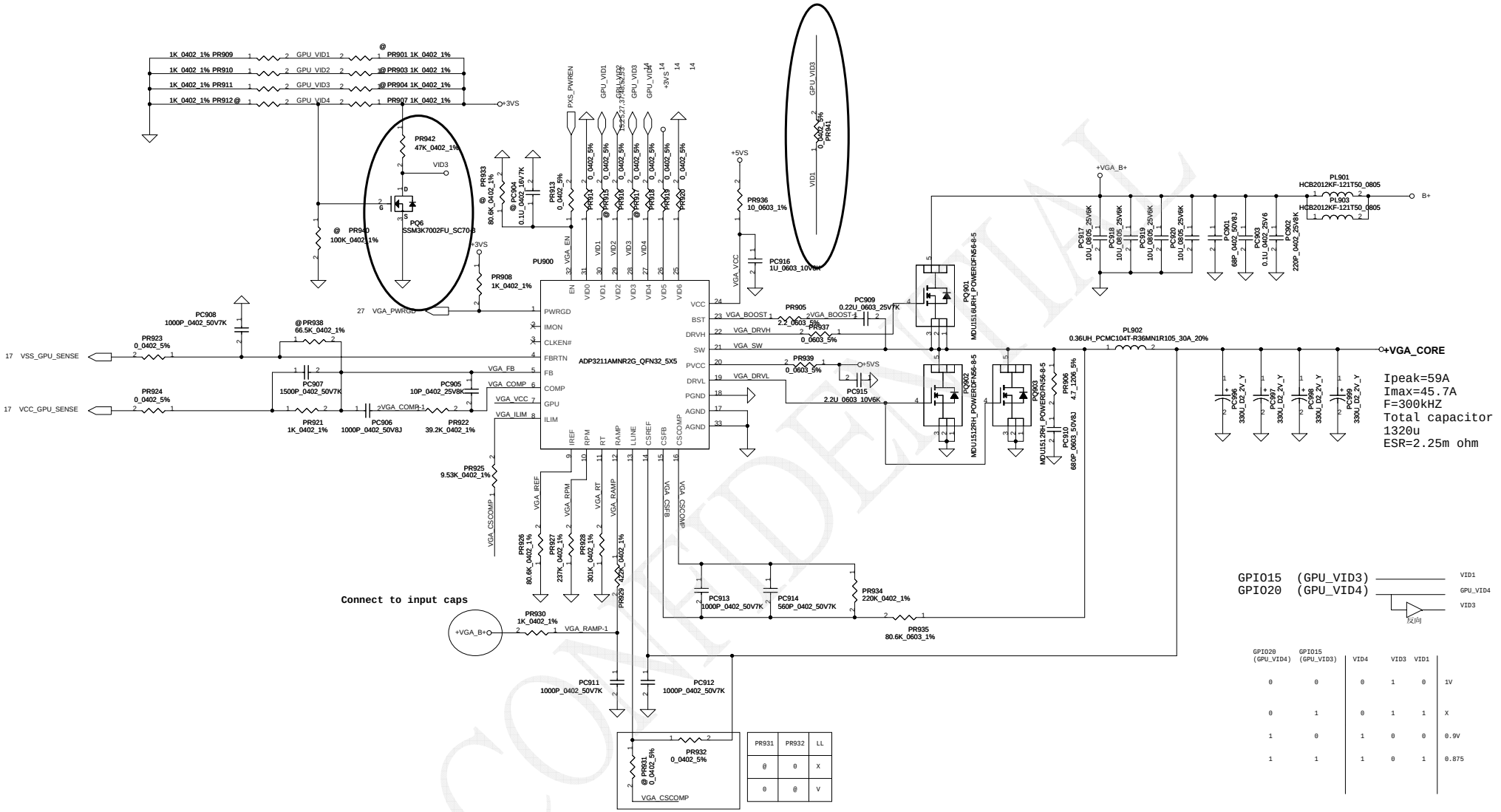

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/10/02	Deciphered Date	2010/10/02
Title	SCHEMATICS, MB A8712		
Size	Document Number LA-8712P		Rev A
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
DB-2	(12/2)	P52-PWR-+1.5VPCIE/0.935V	Change PU935 SY8809 to SY8036	For co-lay cost down
DB-2	(12/2)	P56-PWR_VGA_CORE	Add PQ6,PR941,PR942,PR940	For co-lay Thames and Chelsea
DB-2	(12/2)	P44-PWR-DCIN / Vin Detector	Change to PJP1 pine define	DC-IN jack buy and sale define does not change
DB-2	(12/8)	P45-PWR-BATTERY CONN	Pin 7 power source change +3VLP to +3VALW	EC command
DB-2	(12/8)	P52-PWR-+1.5VPCIE/0.935V	PC11506 loaction change to PC1156	CIC SMT command
DB-2	(12/12)	P52-PWR-+1.5VPCIE/1V	Change PR9352 11.3K to 13.3K (0.935V to 1V)	HW comand
DB-2	(12/12)	P53-PWR-+VDDCIP	Reserver the VDDCI component	For thames GPU
DB-2	(12/12)	P56-PWR_VGA_CORE	Add PR940,PR942,PQ6 ,reserve PR915 and PR917	For thames GPU
DB-2	(12/13)	P50-PWR-1.1VALWP	Add PR803 =10K	SY8809 enbale pin issue
SI	(12/30)	P54-PWR-CPU_CORE/CPU_CORE_NB	PC2057 change 33u 6.3*4.5	ME height limited
SI	(12/30)	P54-PWR-CPU_CORE/CPU_CORE_NB	Add PC2061,PC2062,PC2063,PC2064,PC2065&PC2066,	EMI command

Security Classification	Compal Secret Data		
Issued Date	2005/06/01	Deciphered Date	2006/06/01

Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8712**

Size	Document Number	Rev
	401915	A

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