Ultra-Low On-Resistance 6A Dual Load Switch

Features

- Integrated Dual Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-low On-Resistance R_{ON} of 20mΩ per Channel
- Maximum Continuous Current 6A per Channel
- Low Threshhold Control Input
- Adjustable Rise Time
- Integrated Quick Output Discharge
- RoHS-Compliant, halogen-free

Applications

- Telecom Systems
- Industrial Systems
- Set-Top Boxes
- Consumer Electronics
- Notebooks and Netbooks

Description

The APE8990-HF-3 is a small dual load switch with ultra-low RON of 20mΩ and controlled turn-on, using two N-channel MOSFETs that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 6A each. Each load switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 150Ω on-chip load resistor for output quick discharge when the switch is turned off. In order to avoid inrush current, the rise time is adjustable using an external ceramic capacitor on the CTx pin.

The APE8990-HF-3 is available in an ultra-small, space-saving 3mmx2mm 14-pin DFN package with a thermal pad.

Ordering Information

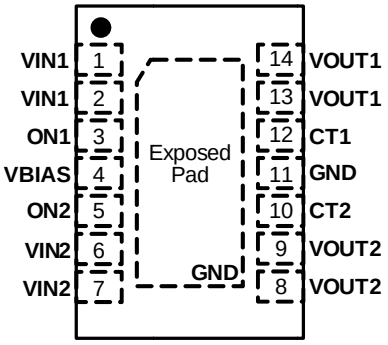
APE8990GN3B-HF-3TR

Package Type

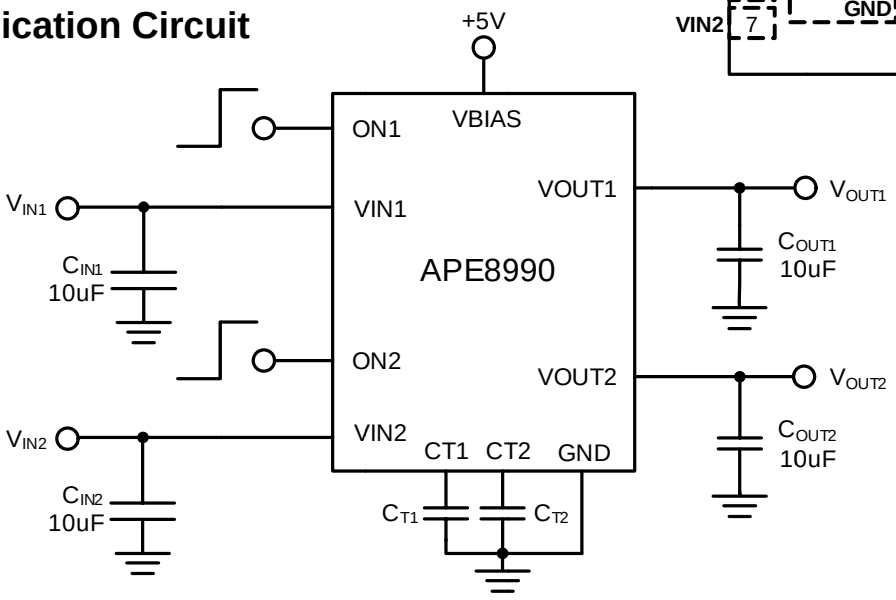
GN3B : DFN3x2-14L

Pin Configuration

Top View
DFN 3x2-14L



Typical Application Circuit



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Absolute Maximum Ratings (Note 1) at T_A= 25°C

VIN1, VIN2	-0.3V to 6V
VOUT1, VOUT2	VIN+0.3V
VON1, VON2	-0.3V to 6V
VBIAS	-0.3+6V
I_{MAX}	6A
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient (Rth_{JA})	
DFN-14L (3mmX2mm)	65°C/W
Thermal Resistance from Junction to (top)Case (Rth_{JC})	
DFN-14L (3mmX2mm)	57°C/W

Recommended Operating Conditions

VIN1,2	0.8V to 5.5V
VBIAS	3V to 5.5V (VBIAS > VIN)
VON1,2	0V to 5.5V
VOUT1,2	VIN1,2
CIN1,2	>4.7uF
Junction Temperature (T_J)	125°C
Operating Temperature Range	-40°C to +85°C

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Specifications.

Note2: The maximum power dissipation is a function of the maximum junction temperature, T_{Jmax} , total thermal resistance, $R_{th(ja)}$ and ambient temperature T_A . The maximum allowable power dissipation at any ambient temperature is (T_{jmax} -T_A) / $R_{th(ja)}$.

Note3: Low duty pulse techniques are used during test to maintain a junction temperature as close to ambient as possible.

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Electrical Specifications

(VIN1, 2=0.8 to 5.5V, VBIAS=5V, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNIT
Quiescent Current	I_{BIAS}	VIN1=VIN2=VON1=VON2=5V IOUT1=IOUT2=0A		120	180	μA
Shutdown Current	I_{SD}	VON1=VON2=GND, VOUT1=VOUT2=0V			1	μA
ON Resistance (each switch) (Note1)	R_{ON}	VONx=VBIAS=5V, IOUTx=1A		20	26	mΩ
		VONx=VBIAS=3.3V, IOUTx=1A		21	27	mΩ
Output Pull Down Resistance	R_{ON}	VBIAS=5V, VONx=0V		150	250	Ω
ONx Input Leakage Current	I_{ON}	VONx=5V or GND			1	μA
ONx Logic High	V_{IH}	Switch on	1.2			V
ONx Logic Low	V_{IL}	Switch off			0.5	V

Note1: Guaranteed by design, not production tested.

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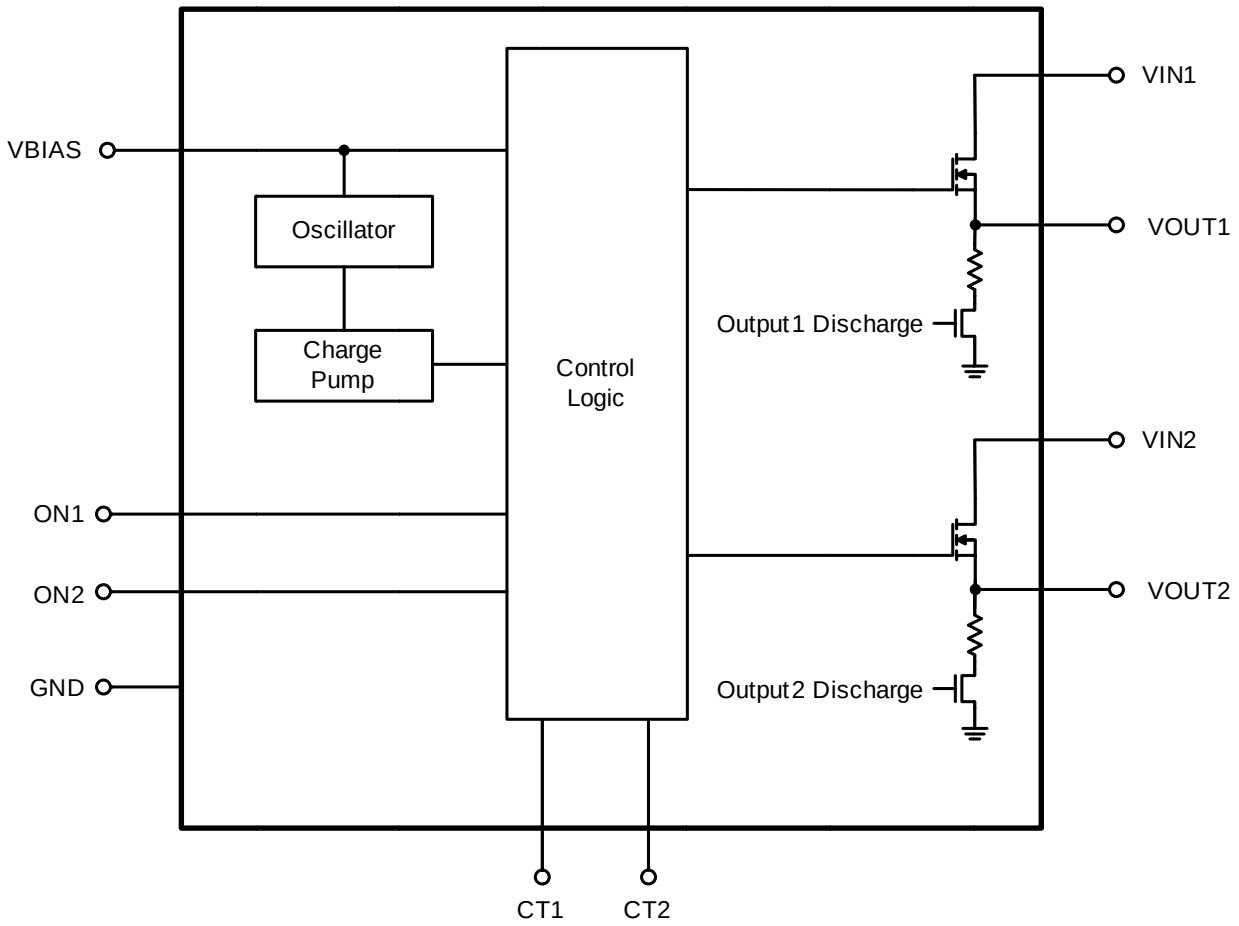
Pin Descriptions

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1, 2	VIN1	Channel 1 input, bypass this input with a ceramic capacitor to ground.
3	ON1	Channel 1 enable control input, active high. Do not leave floating.
4	VBIAS	5V bias voltage.
5	ON2	Channel 2 enable control input, active high. Do not leave floating.
6,7	VIN2	Channel 2 input, bypass this input with a ceramic capacitor to ground.
8,9	VOUT2	Channel 2 output.
10	CT2	A capacitor to ground sets the rise time of VOUT2
11	GND	Ground.
12	CT1	A capacitor to ground sets the rise time of VOUT1
13,14	VOUT1	Channel 1 output.

Block Diagram



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Typical Performance Characteristics

VBIAS=5V, Io=0A, C_{IN}=1µF, C_{OUT}=0.1µF, ch1:ON1, ch2:VOUT1, ch3:ON2, ch4:VOUT2

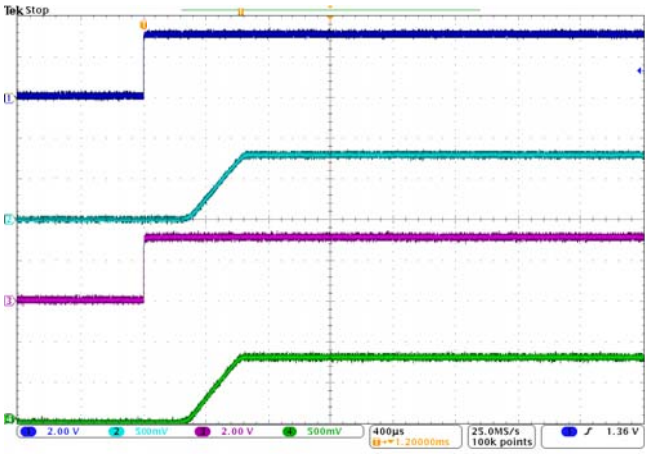

Fig.1 Turn-on Response, VIN=0.8V

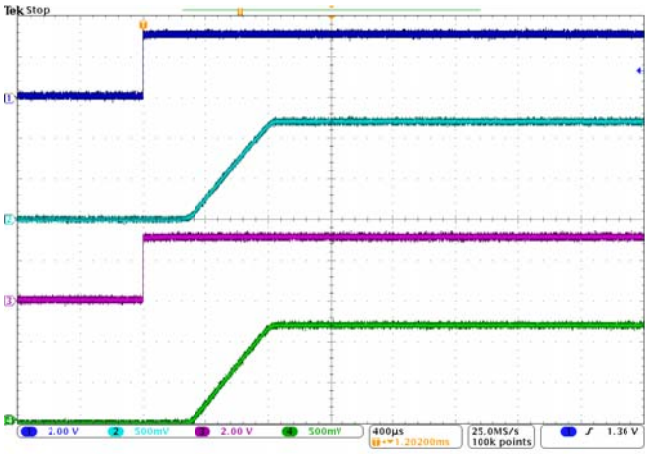

Fig.2 Turn-on Response, VIN=1.2V

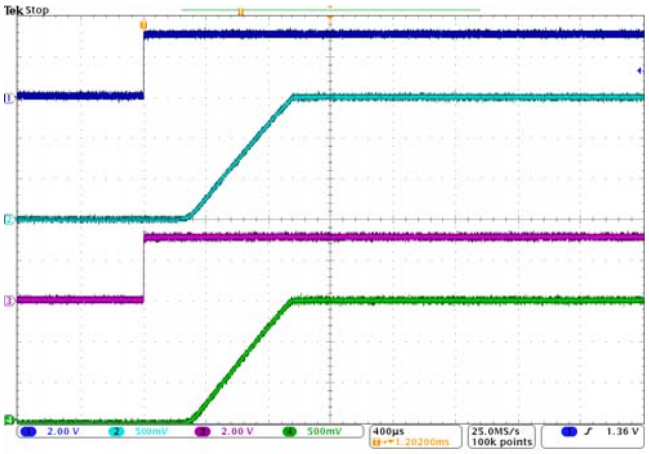

Fig.3 Turn-on Response, VIN=1.5V

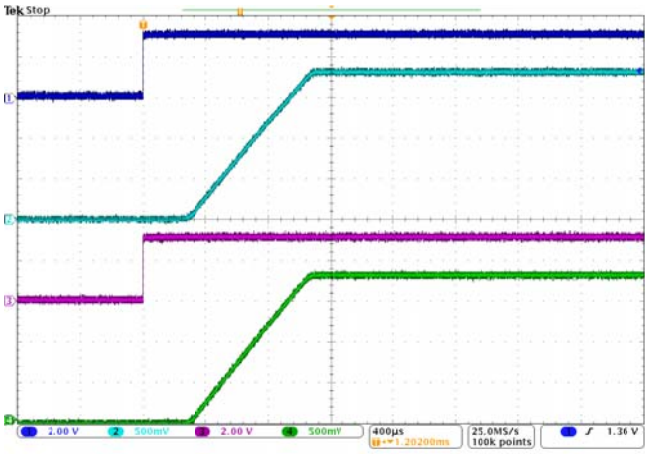

Fig.4 Turn-on Response, VIN=1.8V

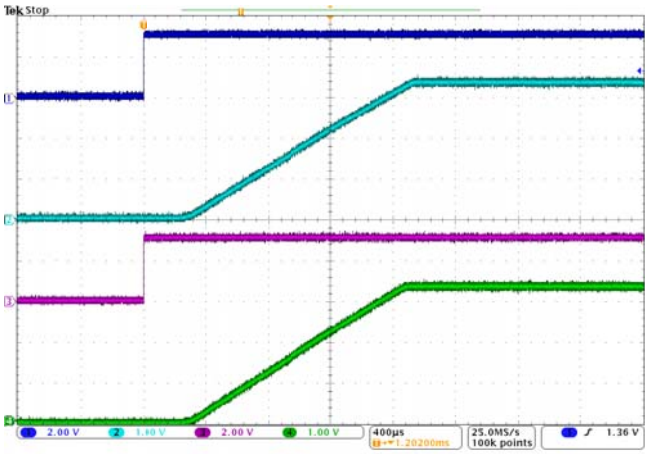

Fig.5 Turn-on Response, VIN=3.3V

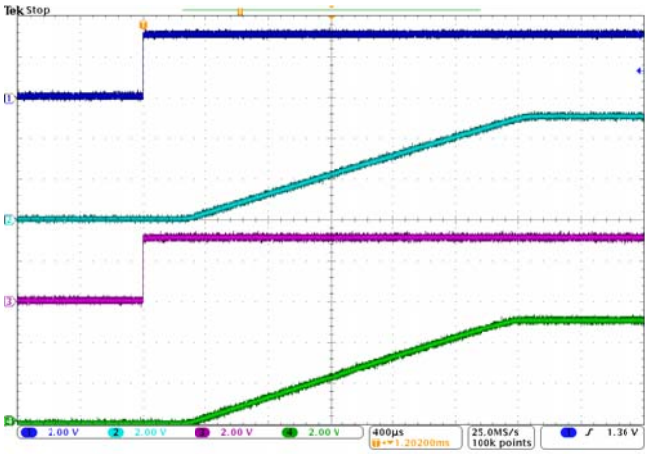

Fig.6 Turn-on Response, VIN=5.0V

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Typical Performance Characteristics (continued)

VBIAS=5V, Io=0A, C_{IN}=1µF, C_{OUT}=0.1µF, ch1:ON1, ch2:VOUT1, ch3:ON2, ch4:VOUT2

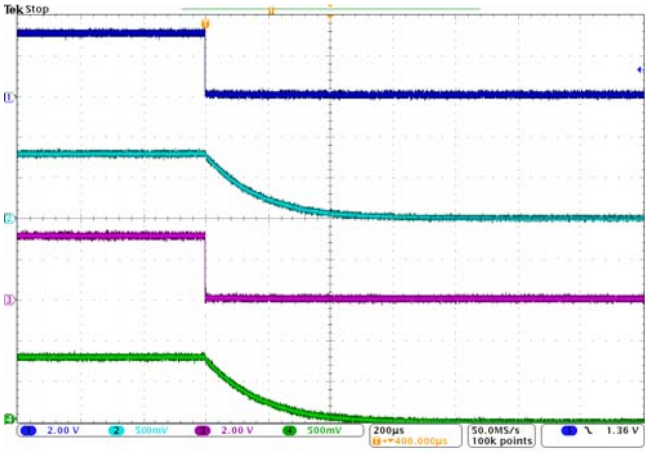

Fig.7 Turn-off Response, VIN=0.8V

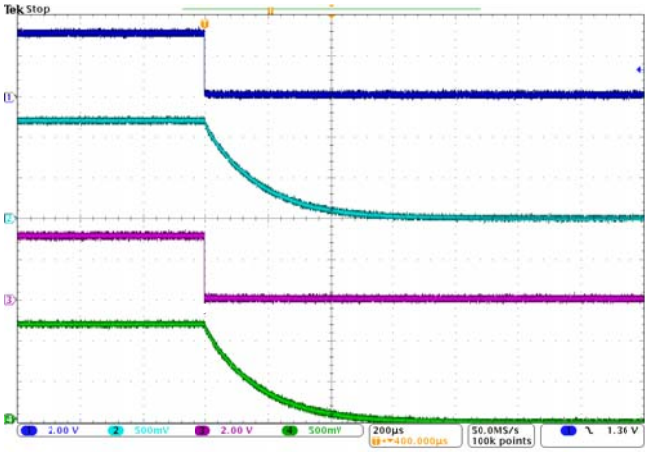

Fig.8 Turn-off Response, VIN=1.2V

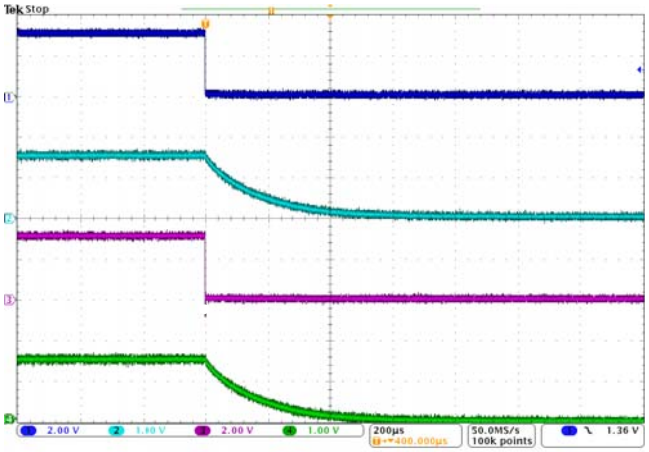

Fig.9 Turn-off Response, VIN=1.5V

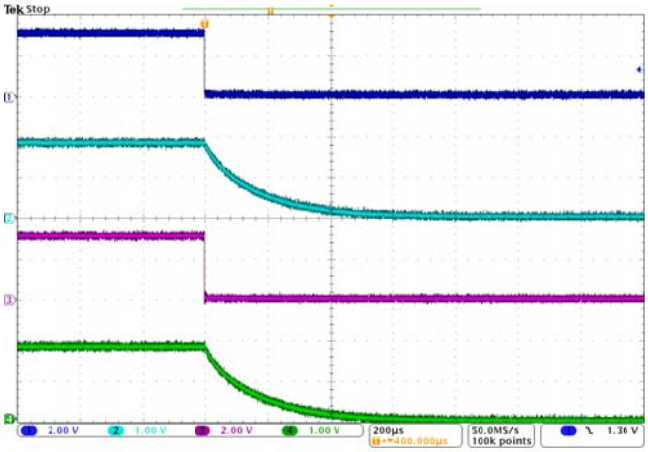

Fig.10 Turn-off Response, VIN=1.8V

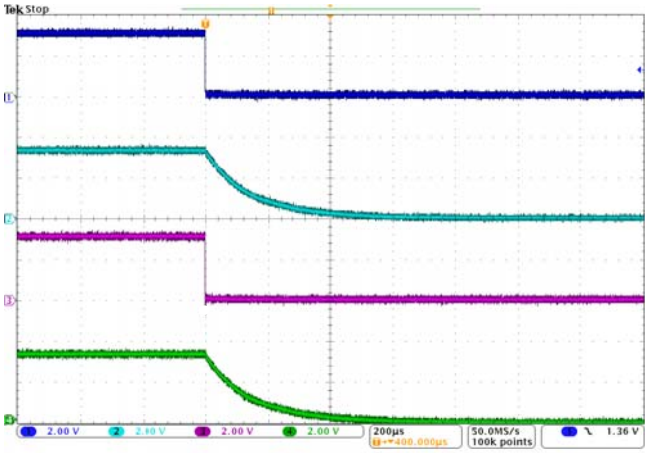

Fig.11 Turn-off Response, VIN=3.3V

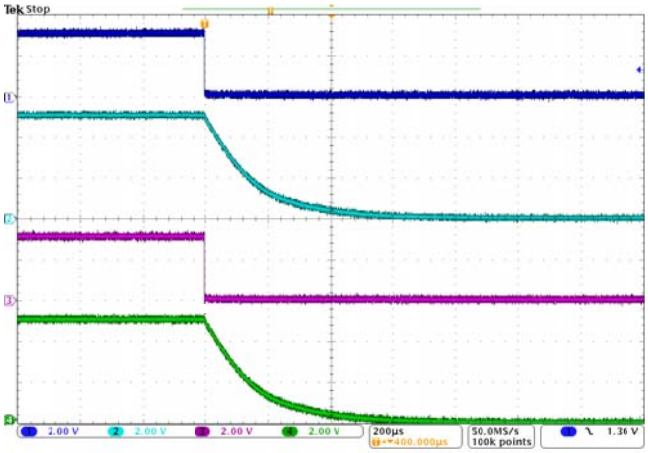

Fig.12 Turn-off Response, VIN=5.0V

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Typical Performance Characteristics (continued)

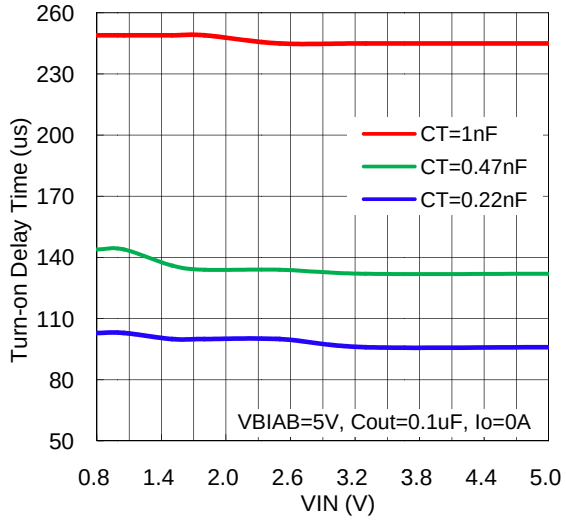

Fig.13 t_{D-ON} vs. VIN

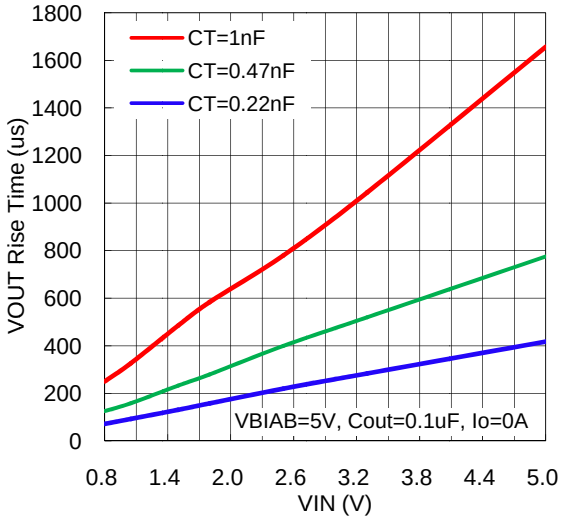

Fig.14 t_R vs. VIN

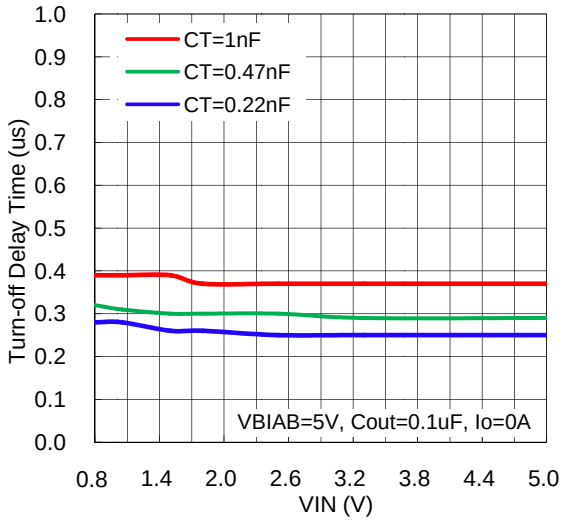

Fig.15 t_{D-OFF} vs. VIN

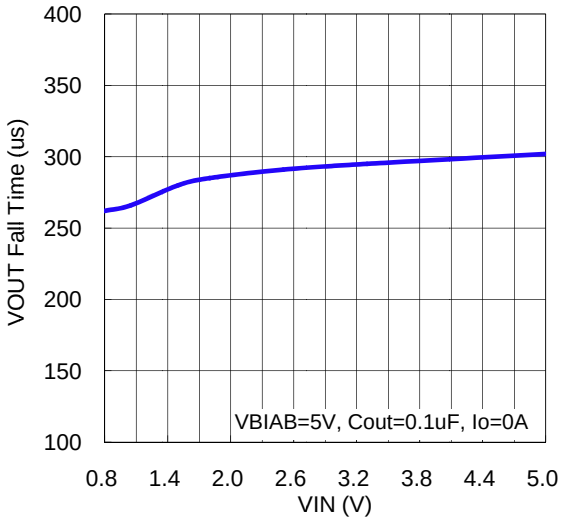

Fig.16 t_F vs. VIN

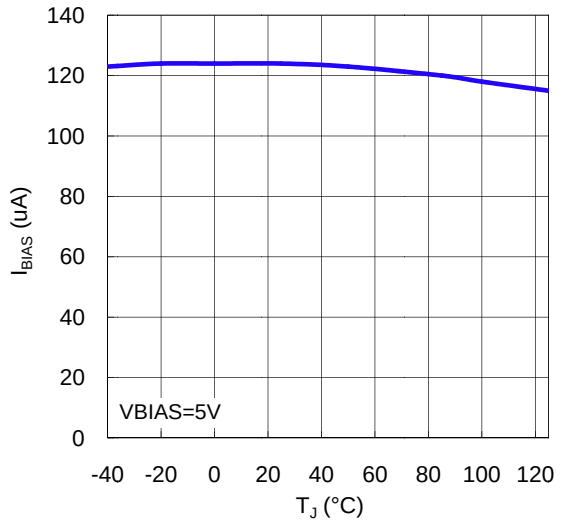

Fig.17 Quiescent Current vs. Temperature

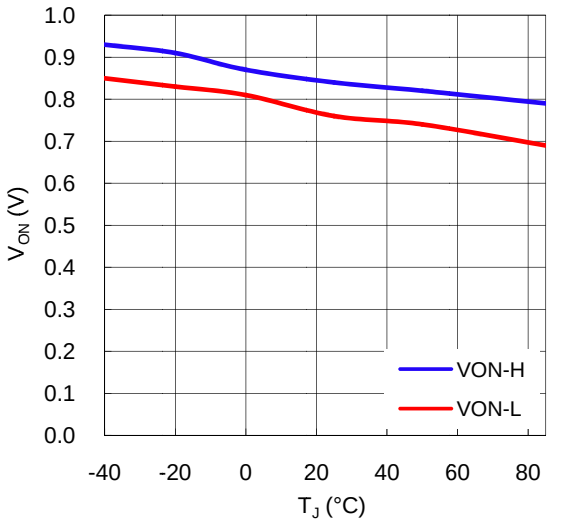

Fig.18 ON Threshold vs. Temperature

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Application Information

On/Off Control

The load switch is controlled by the ON pin. The ONx pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The ONx pin can be used with standard 1.2V, 1.8V, 2.5V or 3.3V GPIO logic threshoolds. Do not leeave the ONx pin floating.

The Figure19 show the VOUTx turn-on/off waveform.

t_{D-ON}: VOUT turn on delay

t_R: VOUT rise time

t_{D-OFF}: VOUT turn off delay

t_F: VOUT fall time

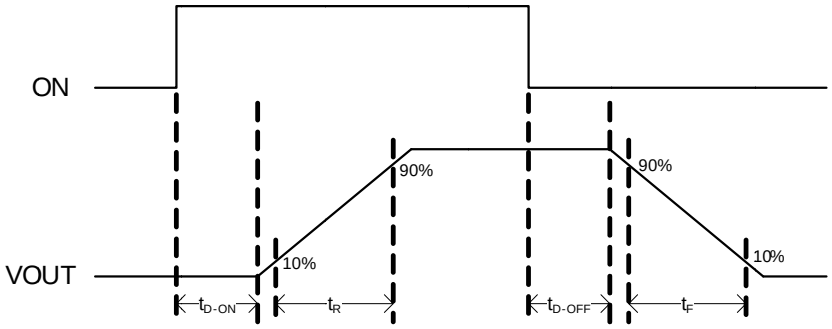

Fig19 ON/OFF Waveform

Output Rise Time Control

The rise time of each VOUTx is adjustable by an external capacitor on the CTx pin. The rise times shown in Table 1 below are typical measured values.

CT (nF)	Rise Time, t_R (µs),10%~90%, C_{OUT}=0.1µF,C_{IN}=1uF							
	VIN=0.8V	VIN=1.05V	VIN=1.2V	VIN=1.5V	VIN=1.8V	VIN=2.5V	VIN=3.3V	VIN=5V
0	27	31	34	38	40	48	59	75
0.22	72	93	107	131	158	220	284	418
0.47	126	159	178	233	280	400	520	776
1	250	327	378	485	584	780	1045	1657
2.2	509	725	827	1027	1235	1777	2391	3593
4.7	1012	1387	1699	1898	2269	3451	4670	7418
10	2008	2865	3425	4328	5203	7491	10142	15409

<Table 1>

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Application Information (continued)

Input Capacitor

An input capacitor is recommended to be placed between VINx and GND to limit the voltage drop on the input supply during high current applications.

Output Capacitor

Setting a C_{IN} greater than the C_{OUT} is highly recommended. Since the MOSFET switch has an internal body diode, this prevents the flow of current through the body diode from VOUTx to VINx when the system supply is removed.

Layout Considerations

Figure 20 shows the reference layout for APE8990-HF-3. The list below will help with layout.

1. The current loops of the two load switches should be separated and symmetrical to each other.
2. Keep the high current paths (VIN, VOUT and GND; blue circle) wide and short to obtain the best effect.
3. The input and output capacitors should be as close to the device as possible to minimize any parasitic trace inductances.
4. Place thermal vias under the exposed pad of the device (green circle). This helps with thermal diffusion away from the device.

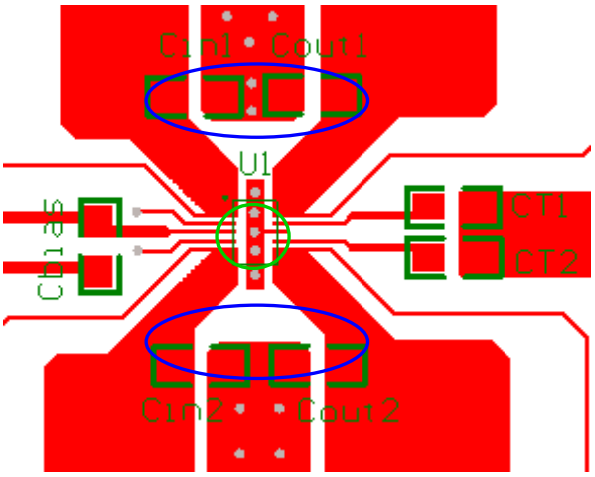

Fig20 APE8990-HF-3 Reference Layout

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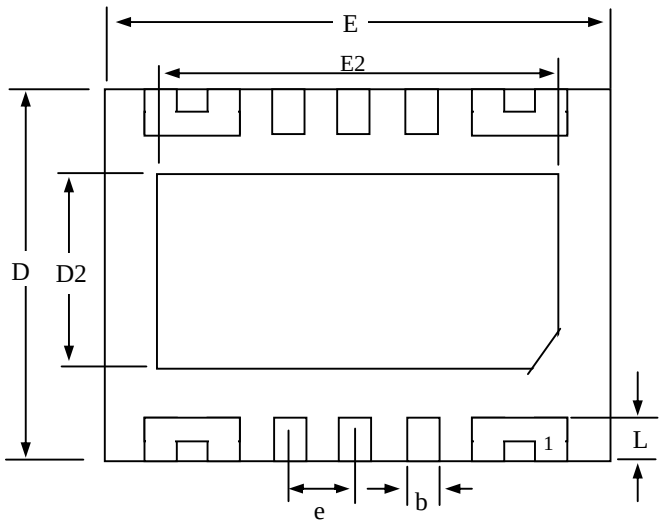
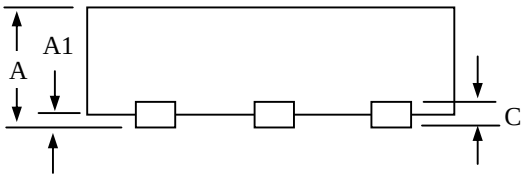
Package Dimensions: DFN3x2-14L



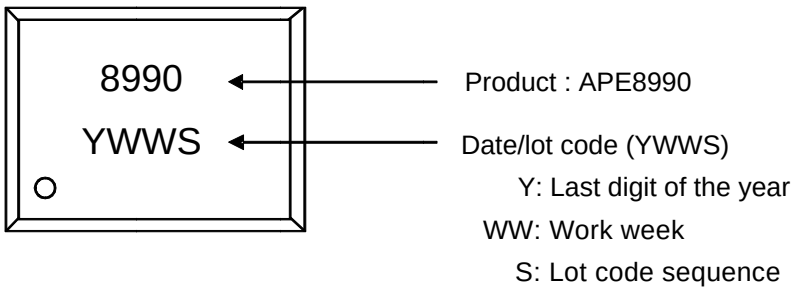
Bottom View



SYMBOLS	Millimeters		
	MIN	NOM	MAX
$A_{(DFN)}$	0.80	0.85	1.00
A1	0.00	-	0.05
b	0.13	0.18	0.23
C	0.195	0.203	0.211
D	1.95	2.00	2.05
D2	0.85	0.90	0.95
E	2.95	3.00	3.05
E2	2.45	2.50	2.55
e	0.40(Ref.)		
L	0.30(Ref.)		

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information



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