ADVANCED MULTI-CHEMISTRY AND MULTI-CELL SYNCHRONOUS SWITCH-MODE CHARGER AND SYSTEM POWER SELECTOR

FEATURES

- **High Efficiency NMOS-NMOS Synchronous Buck Converter With User-Selectable 300 kHz or 500 kHz frequency**
- **bq24721C Offers Softer Turn-On, Stronger Turn-Off**
- **SBS-Like (1) SMBus Interface for Control and Status Communications With Host**
- **Programmable Battery Voltage, Charge Current, and AC Adapter Current via SBS-Like SMBus Interface**
- **0.4% Charge Voltage Regulation Accuracy**
- **3% Charge Current Regulation Accuracy**
- **3% Adapter Current Regulation Accuracy Dynamic Power Management (DPM)**
- **2% Accuracy Integrated Charge and AC Adapter 20× Current Amplifier Output**
- **3-Cell and 4-Cell Li-Ion Voltage Regulation 9 V, 12 V–14.4 V, 16 V–19.2 V**
- **Battery Pack Voltage Operating Range 0 V–19.2 V**
- **AC Adapter Operating Range 8 V–28 V**
- **99.5% Max Duty Cycle**
- **Internal Soft Start**
- **Integrated 5% 5-V LDO When AC Adapter Applied**
- **6-V Drive Supply Voltage for Increased Efficiency**
- **Reverse Battery to Adapter Discharge Protection**
- **Battery/Adapter to System Power Selector Function**
- **Charge and Adapter Overcurrent Protection**
- **Battery Thermistor Sense, TS, Comparators**
- **Available in 32-Pin 5x5-mm QFN Package**

(1) SBS-Like interface is not 100% SBS compliant. SBS-Like interface is SMBus1.1 complaint but does not support Packet Error Correction (PEC). The control and status registers were changed to simplify and enhance notebook charger control. An 8-bit address (0x12) is used. See Table 1 for a comparison between SBS-like vs SBS Specification.

APPLICATIONS

- **Portable Notebook Computers**
- **Portable DVD Players**
- **Webpads, PC Tablets**

DESCRIPTION

The bq24721 is a high efficiency synchronous battery pack charger with high level of integration for portable applications. This device implements a high performance analog front-end that interfaces to the system power management micro-controller through a simplified SBS-like SMBus interface.

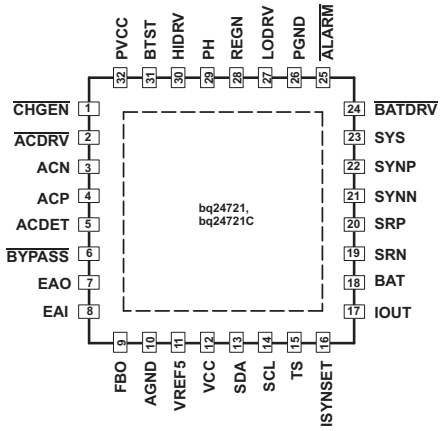
The dynamic power management (DPM) function modifies the charge current depending on system load conditions, avoiding ac adapter overload.

High accuracy current sense amplifiers enable accurate measurement of either the charge current or the ac adapter current, allowing termination of nonsmart packs and monitoring of overall system power.

The adapter isolation diode can be bypassed or entirely replaced with an external MOSFET using a control signal provided by the bq24721, thus reducing overall power dissipation.

Integrated features such as charger soft start, charge overcurrent protection, and IC temperature monitoring provide a second level of protection, in addition to pack and system protection functions.

5x5 QFN PACKAGE (TOP VIEW)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NO.	PACKAGE	THERMISTOR SENSE	BATTERY SHORTED (VERY LOW BATTERY VOLTAGE) OPERATION	ORDERING NUMBER (TAPE AND REEL)	QUANTITY
bq24721	32 PIN 5x5mm QFN	TS	Charge Current Changes to C/8	bq24721RHBR	3000
				bq24721RHBT	250
bq24721C	32 PIN 5x5mm QFN	TS	Charge Current Changes to C/8	bq24721CRHBR	3000
				bq24721CRHBT	250

PACKAGE THERMAL DATA

PACKAGE(1)	θ_{JA}	TA ≤ 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
RHB(2)	36°C/W	2.36 W	0.028 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2×3 via matrix.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	$\overline{\text{CHGEN}}$	Charge enable logic level low input. Logic HI on the $\overline{\text{CHGEN}}$ pin disables the charger. Logic LO on the $\overline{\text{CHGEN}}$ pin enables the charger. When the SMBus control register = bit0, $\overline{\text{CHGEN}}$ is also LO.
2	$\overline{\text{ACDRV}}$	AC adapter to system switch driver output. Connect directly to the gate of the ACFET PMOS power FET. Connect the FET source to the PVCC node and negative side of the input current-sense resistor. Connect the FET drain to the system load side. Recommend placing a 10-kΩ resistor from the gate to the source of the Bypass FET. If needed, an optional capacitor from gate to source of the ACFET is used to help slow down the ON and OFF times. The internal gate drive is asymmetrical allowing a quick turn-off and slower turn-off in addition to the internal break-before-make logic with respect to the $\overline{\text{BATDRV}}$.
3	ACN	Adapter current sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from this pin to AGND for common-mode filtering. An optional 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering.
4	ACP	Adapter current sense resistor, positive input. Place this on the adapter side of the input current sense resistor. Recommend placing a 0.1-µF ceramic capacitor from ACP to AGND to provide common-mode filtering.
5	ACDET	AC adapter detected sense voltage input. Connect a voltage divider resistor from adapter input (before Bypass FET) to ACDET, and another resistor from ACDET to AGND, in order to program adapter detect threshold of 1.2 V. ACDET threshold should be greater than maximum battery regulation voltage, and lower than the minimum adapter voltage.
6	$\overline{\text{BYPASS}}$	Gate drive for the adapter input BYPASS switch to prevent reverse discharge from the battery to the input. Connect this pin directly to the gate of the input bypass PMOS power FET. The source of the FET is connected to the adapter input voltage node. Recommend placing a 10-kΩ resistor from the gate to the source of the BYPASS FET. The drain of the FET is connected to the positive node of the input current-sense resistor. An optional capacitor can be placed from the gate to the source to slow-down the switching times. Adjusting the turn-on and turn-off times is typically not needed for this FET.
7	EAO	Error amplifier output for compensation. Connect the feedback compensation components from EAO to EAI. Typically a capacitor in parallel with a series resistor and capacitor. See the compensation calculation procedures. This node is internally compared to the PWM saw-tooth oscillator.

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NO.	NAME	
8	EAI	Error amplifier input for compensation, also connect the feedback compensation components from EAI to EAO. Connect the input compensation components from FBO to EAI. See the compensation calculation procedures.
9	FBO	Feedback output for compensation. Connect the input compensation components from FBO to EAI. Typically, a resistor in parallel with a series resistor and capacitor. See the compensation calculation procedures.
10	AGND	Analog ground. Ground connection for low current sensitive analog and digital signals. Only connect to the PGND node by connecting to the PowerPAD™ underneath the IC.
11	VREF5	5-V regulated voltage output, used for internal bias and the reference for programming the TS thermistor sense network. Used to indicate adapter present status. It is enabled by ac detected. Connect a 1-μF ceramic capacitor from VREF5 pin to AGND as close to IC as possible.
12	VCC	IC analog positive supply. Connect to adapter input, or diode, or by putting a diode from adapter input and a diode from battery pack to VCC. Put a 1-μF ceramic capacitor from VCC to AGND, as close to the IC as possible.
13	SDA	SMBus Data input. Connect to SMBus data line from the host controller. A 10-kΩ pullup resistor to the host controller supply rail is needed.
14	SCL	SMBus Clock input. Connect to SMBus clock line from the host controller. A 10-kΩ pullup resistor to the host controller supply rail is needed.
15	TS	Thermistor sense input. Use a voltage divider from VREF5 to TS and AGND. Place a resistor from VREF to TS, and a resistor from TS to AGND to program the hot and cold battery pack thermistor temperatures. Charge is disabled when outside the hot/cold window. The TS pin is also used to detect if a battery is connected.
16	ISYNSET	Program current threshold for synchronous to nonsynchronous regulation transition. Place a resistor from ISYNSET to AGND to program the charge undercurrent threshold to force nonsynchronous converter operation at low output current and prevent negative inductor current. Threshold should be set from ½ inductor current ripple to full value of inductor current ripple.
17	IOUT	Battery charger or adapter current amplifier output. Current sense amplifier that outputs a voltage 20x the current sense resistor differential voltage. The output can be selected by SMBus charge control register (0x12) bit3 to be the input adapter current (ACP-ACN), or the battery charge current (SRP-SRN). Place a 0.1-μF capacitor from IOUT to AGND for filtering the output ripple. Optionally, add an RC filter after the output filter for further filtering.
18	BAT	Battery voltage remote sense. Directly connect a kelvin sense trace from the battery pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1-μF capacitor from BAT to AGND close to the IC to filter high frequency noise.
19	SRN	Charge current sense resistor, negative input. Connect to the charge current sense resistor negative terminal. Optionally, add a 0.1-μF ceramic capacitor from SRN to AGND near the IC for common-mode filter.
20	SRP	Charge current sense resistor, positive input. Connect to the charge current sense resistor positive terminal. Recommend placing a 0.1-μF ceramic capacitor from SRP to AGND near the IC for common-mode filter. Optionally, place a 0.1-μF ceramic capacitor from SRP to SRN near the IC for differential-mode filter.
21	SYNN	Charge overcurrent and charge undercurrent negative sense input. Connect to the charge current sense resistor negative terminal. If sensing the same sense resistor as SRN, the user can connect directly to the SRN pin and no further filter capacitors are needed. To sense a different sense resistor, add a 0.1-μF ceramic capacitor from SYNN to AGND near the IC for common-mode filter.
22	SYNP	Charge overcurrent and charge undercurrent negative sense input. Connect to the charge current sense resistor positive terminal. If sensing the same sense resistor as SRP, the user can connect directly to the SRP pin, and no further filter capacitors are needed. To sense a different sense resistor, add a 0.1-μF ceramic capacitor from SYNP to AGND near the IC for common-mode filter, and place a 0.1-μF ceramic capacitor from SYNP to SYNN near the IC for differential-mode filter.
23	SYS	System load, voltage sense. Connect directly to the system load node and the drain of the BAT PMOS power FET.

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NO.	NAME	
24	$\overline{\text{BATDRV}}$	Battery to system switch driver output. Gate drive for the battery to system load BAT PMOS power FET to isolate the system from the battery to prevent current flow from the system to the battery, while allowing a low impedance path from battery to system while discharging the battery pack to the system load. Connect this pin directly to the gate of the input BAT PMOS power FET. Connect the source of the FET to the system load voltage node. Connect the drain of the FET to the battery pack positive node. Recommend placing a 10-kΩ resistor from the gate to the source of the BAT FET. An optional capacitor is placed from the gate to the source to slow-down the switching times. The internal gate drive is asymmetrical allowing a quick turn-off and slower turn-off in addition to the internal break-before-make logic with respect to the $\overline{\text{ACDRV}}$.
25	$\overline{\text{ALARM}}$	Alarm indicating charger status change, open-drain output. The $\overline{\text{ALARM}}$ is pulled low (LO) whenever the SMBus status register (0x13) has a change. The $\overline{\text{ALARM}}$ output is cleared (HI) when the SMBus status (0x13) register is read, or there is a reset. This is used to alert the host and initiate an interrupt with the host instead of having to continuously poll the charger. A 10-kΩ pull-up resistor to the host controller supply rail is needed.
26	PGND	Power ground. Ground connection for the high-current power converter nodes. Only connect to the AGND node by connecting to the PowerPAD™ underneath the IC.
27	LODRV	PWM low side driver output. Connect directly to the gate of the low-side NMOS power FET with a short trace.
28	REGN	Low-side driver gate voltage regulator and source for high-side driver bootstrap voltage. Add a 1-µF ceramic capacitor from REGN pin to PGND pin, close to the IC. Place a small signal Schottky diode from REGN to BTST for bootstrap voltage.
29	PH	High-side driver negative supply. Connect directly to the source of the high-side NMOS FET with a short trace. This node is the common connection between the high-side FET, low-side FET, and output inductor. Connect a 0.1-µF boot-strap ceramic capacitor from BTST to PH.
30	HIDRV	PWM high side driver output. Connect directly to the gate of the high-side NMOS power FET with a short trace.
31	BTST	High-side driver positive supply, connect pos-side of boot-strap capacitor. Connect a 0.1-µF bootstrap capacitor from the BTST pin to the PH node. Also, connect a bootstrap diode with the anode connected to the REGN pin and the cathode connected to the BTST pin. An optional 4.7-Ω - 15-Ω series resistor is placed between the BTST pin and the bootstrap-diode/capacitor junction to slow-down the turn-on time of the high-side FET for reducing ringing due to high dv/dt of the phase node.
32	PVCC	IC power positive supply. Connect directly to the drain of the high-side NMOS power FET. Recommend placing at least a 10-µF ceramic capacitor directly from the drain of the high-side NMOS power FET to PGND. Up to 40 µF may be needed to prevent resonance filtering inductance. Also, a 0.1-µF decoupling ceramic capacitor is recommended.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

PARAMETER	PIN	VALUE / UNIT
Supply voltage range	ACN, ACP, PVCC, $\overline{\text{ACDRV}}$, SYNN, SYNP, SRP, SRN, $\overline{\text{BATDRV}}$, BAT, $\overline{\text{BYPASS}}$, SYS, VCC	–0.3 V to 30 V
	PH	–1 V to 30 V
	LODRV, REGN, FBO, EAI, EAO, ISYNSET, $\overline{\text{CHGEN}}$, TS , VREF5, ACDET, IOUT, $\overline{\text{ALARM}}$, SCL, SDA	–0.3 V to 7 V
	BTST, HIDRV (with respect to AGND and PGND)	–1 V to 36 V
Maximum differential voltage	AGND-PGND	–0.3 V to 0.3 V
Maximum difference voltage	ACP–ACN , SRP–SRN, and SYNP–SYNN	0.6 V
Operating ambient temperature range (T_A)		–40°C to 85°C
Maximum junction temperature (T_{J_MAX})		150°C
Storage temperature range (T_{stg})		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to AGND, unless otherwise noted. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	PIN	MIN	NOM	MAX	UNIT
Supply voltage range	ACN, ACP, PVCC, $\overline{\text{ACDRV}}$, SRP, SRN, $\overline{\text{BATDRV}}$, BAT, $\overline{\text{BYPASS}}$, SYS, VCC, SYNN, SYNP	0		24	V
	PH	–0.5		30	V
	LODRV, REGN, VREF5	0		6.5	V
	FBO, EAI, EAO, ISYNSET, $\overline{\text{CHGEN}}$, TS , ACDET, SCL, SDA, $\overline{\text{ALARM}}$	0		5.5	V
	IOUT, ACDET	0		5.5	V
	BTST, HIDRV	0		30	V
Maximum differential voltage	AGND-PGND			0	V
Maximum difference voltage	ACP–ACN, SYNN–SYNP, SRP–SRN			0.5	V
Junction temperature Range (T_J)		0		125	°C
Storage temperature Range (T_{stg})		-55		150	°C

ELECTRICAL CHARACTERISTICS

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BATTERY VOLTAGE REGULATION							
$V_{(BAT_ICR)}$	VBAT Input voltage range	$V_{(BAT)}$		0		PVCC	V
	Battery Regulation Voltage Accuracy	Full valid voltage DAC range, SMBus DAC register 0×15	T_J = 0°C – 85°C	–0.4		0.4	%
			T_J = 0°C – 125°C	–0.5		0.5	
$V_{(VBATREG)}$	BAT voltage regulation range			9		19.2	V
PWM AC ADAPTER INPUT CURRENT REGULATION, DPM (Dynamic Power Management), $I_{(REG_DPM)}$= $V_{(IREG_DPM)}$/$R_{(SENSE_DPM)}$							
$V_{(IREG_DPM)}$	ACP-ACN differential voltage range for input current regulation	$V_{(IREG_DPM)}$ = $V_{(ACP)}$- $V_{(ACN)}$ SMBus DAC register 0×3F, bits b0–b13		1.28		162.56	mV
$I_{(REG_step_DPM)}$	Current regulation LSB programming current step	$V_{(ACP-ACN)}$ / 10mΩ Using a 10mΩ sense resistor, $R_{(SNS)}$			128		mA
	Current regulation accuracy	V_{CC} ≥ V_{CC} (min), V_{CC} ≥ $V_{I(BAT)}$ + $V_{(DO-MAX)}$, (1) Over differential threshold range, $V_{(IREG)}$, Does not include error induced by the tolerance of the sense resistor, $R_{(SNS)}$	$V_{(ACP)}$ – $V_{(ACN)}$ > 40.96 mV (4096 mA with 10 mΩ)	–3%		3%	
			$V_{(ACP)}$ – $V_{(ACN)}$ > 20.48 mV (2048 mA with 10 mΩ)	–5%		5%	
			$V_{(ACP)}$ – $V_{(ACN)}$ > 5.12 mV (512 mA with 10 mΩ)	–25%		25%	
PWM BATTERY CHARGE CURRENT REGULATION, $I_{(REG_CHG)}$= $V_{(IREG_CHG)}$/ $R_{(SENSE_CHG)}$							
$V_{(IREG_CHG)}$	SRP-SRN differential voltage range for input current regulation	$V_{(IREG_CHG)}$ = $V_{(SRP)}$- $V_{(SRN)}$ SMBus DAC register 0×14, bits b0–b13		1.28		162.56	mV
$I_{(REG_step_CHG)}$	Current regulation LSB programming current step	$V_{(SRP-SRN)}$ / 10 mΩ Using a 10mΩ sense resistor, $R_{(SNS)}$			128		mA
	Current regulation accuracy	V_{CC} ≥ V_{CC} (min), V_{CC} ≥ $V_{I(BAT)}$ + $V_{(DO-MAX)}$, (1) Over differential threshold range, $V_{(IREG)}$, Does not include error induced by the tolerance of the sense resistor, $R_{(SNS)}$	$V_{(SRP-SRN)}$ > 40.96 mV (4096 mA with 10 mΩ)	–3		3	%
			$V_{(SRP-SRN)}$ >20.48 mV (2048 mA with 10 mΩ)	–5		5	
			$V_{(SRP-SRN)}$ > 5.12 mV (512 mA with 10 mΩ)	–25		25	
CURRENT SENSE AMPLIFIERS – IBAT AMPLIFIER and IADAPT AMPLIFIER → MUX TO IOUT							
$V_{(IOUT_IBAT)}$	SRP, SRN common-mode input voltage range			2.5		20	V
	IOUT output voltage range with IBAT selected	$V_{(IOUT)}$ = $V_{(SRP,\ SRN)}$× $A_{(IBAT)}$ $V_{(BAT)}$ > 2.5 V or $V_{(BAT)}$ > $V_{(IOUT)}$ + $V_{(DO-MAX)}$(1)		0		3.5	V
$G_{(IBAT)}$	Voltage gain	$A_{(IOUT)}$ = $V_{(IOUT)}$/ $V_{(SRP,\ SRN)}$			20		V/V
	Charge current amplifier accuracy	$V_{(BAT)}$ > 2.5 V or $V_{(BAT)}$ > $V_{(IOUT)}$ + $V_{(DO-MAX)}$(1)	$V_{(SRP,\ SRN)}$ = 40 mV and higher	–2		2	%
			$V_{(SRP,\ SRN)}$ = 20 mV and higher	–3		3	
			$V_{(SRP,\ SRN)}$ = 5 mV and higher	–25		25	
$V_{(IOUT_IADAPT)}$	ACP, ACN Common-mode input voltage range			0		24	V
	IOUT output voltage range with IADAPT selected	$V_{(IOUT)}$ = $V_{(ACP,\ ACN)}$× $A_{(IADP)}$ $V_{(SRP)}$ > 2.5 V or $V_{(SRP)}$ > $V_{(IOUT)}$ + 1 V		0		3.5	V
$G_{(IADP)}$	Voltage gain	$A_{(IADP)}$ = $V_{(IOUT)}$/ $V_{(ACP,\ ACN)}$			20		V/V
	Adapter current amplifier accuracy, bq24721	$V_{(BAT)}$ > 2.5 V or $V_{(BAT)}$ > $V_{(IOUT)}$ + $V_{(DO-MAX)}$(1)	$V_{(ACP,\ ACN)}$ = 40 mV and higher	–2		2	%
			$V_{(ACP,\ ACN)}$ = 30 mV and higher	–3		3	
			$V_{(ACP,\ ACN)}$ = 5 mV and higher	–25		25	
	Adapter current amplifier accuracy, bq24721C	$V_{(BAT)}$ > 2.5 V or $V_{(BAT)}$ > $V_{(IOUT)}$ + $V_{(DO-MAX)}$(1)	$V_{(ACP,\ ACN)}$ = 40 mV and higher	–2		2	%
			$V_{(ACP,\ ACN)}$ = 30 mV and higher	–5		5	
			$V_{(ACP,\ ACN)}$ = 5 mV and higher	–25		25	
$I_{(OUT_LIM)}$	IOUT output current limit	IOUT shorted to AGND		4.5			mA
OPERATING CONDITIONS							
$V_{(INOP)}$	$V_{(VCC)}$, $V_{(PVCC)}$, input voltage operating range	Selector and charger operational.		8		24	V

(1) $V_{(DO-max)}$ is defined as the maximum drop-out voltage. $V_{(DO-MAX)}$ = 1 V unless other wise specified. In an actual application, $V_{(DO\ -\ MAX)}$ = ($R_{(SNS)}$× I_O) + $V_{(DSON_HIGH_SIDE_FET)}$ + $V_{(DSON_BYPASS_FET)}$.

ELECTRICAL CHARACTERISTICS (continued)

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT – NO ADAPTER CONNECTED						
$I_{(VCC,PVCC)}$	VCC and PVCC quiescent current	$I_{(VCC,PVCC)}$ = ($I_{(VCC)}$ + $I_{(PVCC)}$) at $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			254	µA
$I_{(ACP,ACN)}$	ACP and ACN quiescent current	$I_{(ACP,ACN)}$ = ($I_{(ACP)}$ + $I_{(ACN)}$) at $V_{(ACP)}$ = $V_{(ACN)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			1	µA
$I_{(BAT)}$	BAT quiescent current	$I_{(BAT)}$ at $V_{(BAT)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			17	µA
$I_{(SRP,SRN)}$	SRP and SRN quiescent current	$I_{(SRP,SRN)}$ = ($I_{(SRP)}$ + $I_{(SRN)}$) at $V_{(SRP)}$ = $V_{(SRN)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			1	µA
$I_{(SYNN,SYNP)}$	SYNN and SYNP quiescent current	$I_{(SYNN,SYNP)}$ = ($I_{(SYNN)}$ + $I_{(SYNP)}$) at $V_{(SYNP)}$ = $V_{(SYNN)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			1	µA
$I_{(SYS)}$	SYS quiescent current	$I_{(SYS)}$ at $V_{(SYS)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			25	µA
$I_{(PH)}$	PH quiescent current	$I_{(PH)}$ at $V_{(PH)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			1	µA
$I_{(BTST)}$	BTST quiescent current	$I_{(BTST)}$ at $V_{(BTST)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			1	µA
QUIESCENT CURRENT – ADAPTER CONNECTED AND READY TO CHARGE						
$I_{(VCC,PVCC)}$	VCC and PVCC quiescent current	$I_{(VCC,PVCC)}$ = ($I_{(VCC)}$ + $I_{(PVCC)}$ at $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			4.45	mA
$I_{(ACP,ACN)}$	ACP and ACN quiescent current	$I_{(ACP,ACN)}$ = ($I_{(ACP)}$ + $I_{(ACN)}$) at $V_{(ACP)}$ = $V_{(ACN)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			815	µA
$I_{(BAT)}$	BAT quiescent current	$I_{(BAT)}$ at $V_{(BAT)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			500	µA
$I_{(SRP,SRN)}$	SRP and SRN quiescent current	$I_{(SRP,SRN)}$ = ($I_{(SRP)}$ + $I_{(SRN)}$) at $V_{(SRP)}$ = $V_{(SRN)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			305	µA
$I_{(SYNN,SYNP,SYS)}$	SYNN, SYNP, and SYS quiescent current	$I_{(SYNN,SYNP,SYS)}$ = ($I_{(SYNN)}$ + $I_{(SYNP)}$ + $I_{(SYS)}$) at $V_{(SYNP)}$ = $V_{(SYNN)}$ = $V_{(SYS)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			321	µA
$I_{(PH)}$	PH quiescent current	$I_{(PH)}$ at $V_{(PH)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			1	µA
$I_{(BTST)}$	BTST quiescent current	$I_{(BTST)}$ at $V_{(BTST)}$ = $V_{(VCC)}$ = $V_{(PVCC)}$ = 16.8 V			1	µA
$I_{(VCC_SW)}$	VCC Current while converter is switching including gate drive current	$I_{(VCC_SW)}$ = $I_{(VCC)}$ FPWM = 300 kHz, charger on ($\overline{CHGEN}$ = LO) = ENABLED $Q_{(G)}$ at HIDRV = $Q_{(G)}$ at LODRV = 30 nC, [No Load on VREF5] Gate drive switching current = $Q_{(G)}$× FPWM = (30nC + 30nC) × 300kHz = 18mA		25		mA
5-V REFERENCE LDO VOLTAGE AND AC DETECTION STATUS (VREF5, TURNS ON WHEN AC DETECTED)						
$V_{(VREF5)}$	5V Regulator output voltage	Adapter detected (V_{ACDET} >$V_{(ACD)}$), V_{CC}> 7 V 0 → 10 mA, source current	4.75	5	5.25	V
$V_{(VREF5_SAT)}$	Saturation voltage when VREF5 is off	Adapter not detected, (V_{ACDET}< $V_{(ACD)}$) 0 →– 10 mA, ac adapter inserted, C_O = 1 µF, discharge Load			0.3	V
$I_{(VREF5_LIM)}$	Short-circuit current	$V_{(VREF5)}$ = AGND		20		mA
UNDERVOLTAGE LOCKOUT CIRCUIT						
UVLO	Undervoltage lockout threshold	VREF5 rising, POR mode set at VREF5 < $V_{(UVLO)}$		3.7		V
	$V_{(UVLO)}$ hysteresis	VREF5 falling		100		mV
SBS-Like SMBus LOGIC LEVELS						
V_{IL}	Input low threshold level	2.7 V < $V_{(pull-up)}$ < 5.5 V, SDA and SCL			0.8	V
V_{IH}	Input high threshold level	2.7 V < $V_{(pull-up)}$ < 5.5 V, SDA and SCL	2.1			V
$I_{(bias)}$	Input bias current	2.7 V < $V_{(pull-up)}$ < 5.5 V, SDA and SCL			1	µA
$\overline{ALARM}$ OPEN DRAIN OUTPUT						
$V_{(ALARM_sat)}$	$\overline{ALARM}$ output low saturation level	$I_{(ALARM)}$ = 5mA			0.5	V
$I_{lkg(ALARM)}$	$\overline{ALARM}$ leakage current	$V_{(\overline{ALARM})}$ = 5V			1	µA
THERMAL SHUTDOWN, IC OVERTEMPERATURE PROTECTION						
$T_{(SHUT)}$	Thermal shutdown Threshold	T_J rising, Charge disabled at T_J > $T_{(SHUT)}$		145		°C
$T_{(SHUTH)}$	Hysteresis	T_J falling, Charge enabled at T_J < $T_{(SHUT)}$– $T_{(SHUTH)}$		15		°C
	Deglitch time, thermal shutdown	T_J rising/falling		8		ms

ELECTRICAL CHARACTERISTICS (continued)

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMISTOR COMPARATORS, TS						
$V_{(LTF)}$	Cold temperature threshold, TS pin voltage	$V_{(TS)}$ rising	72.8	73.5	74.2	%VREF5
$V_{(LTFH)}$	Hysteresis for LTF threshold	$V_{(TS)}$ falling	0.5	1	1.5	%VREF5
$V_{(TCO)}$	Cutoff temperature threshold, TS pin voltage	$V_{(TS)}$ rising	28.7	29.3	29.9	%VREF5
$V_{(HTF)}$	Hot temperature threshold, TS pin voltage	$V_{(TS)}$ rising/falling	33.7	34.4	35.1	%VREF5
$V_{(TSDET)}$	Pack thermistor insertion detected	$V_{T(S)}$ rising/falling	82.45	85	87.55	%VREF5
	Deglitch time for temperature out of range detection	$V_{(TS)}$ rising above $V_{(LTF)}$, or $V_{(TS)}$ falling below $V_{(TCO)}$, or $V_{(TS)}$ falling below $V_{(HTF)}$		16		µs
	Deglitch time for temperature in valid range detection	$V_{(TS)}$ falling below ($V_{(LTF)}$ - $V_{(LTFH)}$), or $V_{(TS)}$ rising above $V_{(TCO)}$, or $V_{(TS)}$ rising above $V_{(HTF)}$		8		ms
	Deglitch time for thermistor removal detection	$V_{(TS)}$ rising above $V_{(TSDET)}$ $V_{(TS)}$ > $V_{(TSDET)}$ (pack removed)		16		µs
	Deglitch time for thermistor insertion detection	$V_{(TS)}$ falling below $V_{(TSDET)}$ $V_{(TS)}$ < $V_{(TSDET)}$ (pack inserted)		1		s
CHARGE OVERCURRENT COMPARATOR						
$V_{(OLP)}$	Overcurrent protection threshold	$V_{(SYNP-SYNN)}$ rising		200		%$I_{(REG_CHG)}$
$V_{(OLPH)}$	Hysteresis	$V_{(SYNP-SYNN)}$ falling		20		%$I_{(REG_CHG)}$
	Deglitch time	$V_{(SYNP-SYNN)}$ rising and falling		1		µs
SYNCHRONOUS to NONSYNCHRONOUS CURRENT COMPARATOR (ISYNSET)						
$V_{(SYNSET)}$	ISYNSET pin set voltage			1		V
$K_{(SYNSET)}$	ISYNSET current set factor	$V_{(SYNP-SYNN)}$ falling, I_{SYN_NSYN}= ($V_{(SYNSET)}$ × $K_{(SYNSET)}$)/($R_{(SYNSET)}$ × $R_{(SENSE_CHG)}$)		500		V/A
$V_{(SYN_HYS)}$	$V_{(SYNP-SYNN)}$ hysteresis voltage, rising	$V_{(SYNP-SYNN)}$ rising		1.5		mV
	Deglitch time, Synch to Non-Synch	$V_{(SYNP-SYNN)}$ rising and falling		1		µs
ADAPTER OVERCURRENT COMPARATOR (ACOC)						
$V_{(ACOC)}$	ACOC Input over-current protection sense resistor voltage threshold	$V_{(ACP-ACN)}$ ≥ $V_{(ACOC)}$, where SMBus charge mode register (0×12), b6 = 1 = ACOC_protection_enabled, b8 = 0, b7 = 0	110	130	155	% of $I_{(REG_DPM)}$
		$V_{(ACP-ACN)}$ ≥ $V_{(ACOC)}$, where SMBus charge mode register (0×12), b6 = 1 = ACOC_protection_enabled, b8 = 0, b7 = 1	130	150	175	% of $I_{(REG_DPM)}$
		$V_{(ACP-ACN)}$ ≥ $V_{(ACOC)}$, where SMBus charge mode register (0×12), b6 = 1 = ACOC_protection_enabled, b8 = 1, b7 = 0	150	170	195	% of $I_{(REG_DPM)}$
		$V_{(ACP-ACN)}$ ≥ $V_{(ACOC)}$, where SMBus charge mode register (0×12), b6 1 = ACOC_protection_enabled, b8 = 1, b7 = 1	170	190	215	% of $I_{(REG_DPM)}$
$V_{(ACOCH)}$	ACOC Hysteresis	$V_{(SRP-SRN)}$ falling		7		%$I_{(REG_CHG)}$
	ACOC deglitch time before ACDRV turns-off	$V_{(ACP-ACN)}$ rising		16		µs
	ACOC delay time after $V_{(ACP-ACN)}$≤$V_{(ACOC)}$ before ACDRV turn-on	$V_{(ACP-ACN)}$ falling, $V_{(ACP-ACN)}$≤$V_{(ACOC)}$		8		ms
SYSTEM STATUS COMPARATORS INPUT SPECIFICATIONS						
V_{ICR}	Common mode input range at pin: ACDET		0		5	V
	Common mode input range at TS pin		0.5		VREF5	V
	Common mode input voltage range at pins: BAT, SYS		0		VCC	V
$I_{(bias)}$	Input bias currents at pins: ACDET, TS, BATDEP, SYS				0.2	µA
BATTERY DEPLETED COMPARATOR (BATDEP)						
$V_{(BATDEP)}$	BAT depleted voltage range	$V_{(BATDEP)}$ = 2.2 V + $V_{(step)}$× batdep_dac_code, where batdep_dac_code = 0 - 7, and Vstep = 0.1V, SMBus Charge Mode register 0×12, bits b9, b10, b11 For programmed $V_{(BATREG)}$ = 9 V, then cell = 2 For programmed $V_{(BATREG)}$ = 12 V - 14.4 V, then cell = 3 For programmed $V_{(BATREG)}$ = 16 V - 19.2 V, then cell = 4	2.2		2.9	V/cell
	BAT depleted accuracy		-2%		2%	
	Battery depleted detection deglitch time	$V_{(BAT)}$ falling		1		s
	Battery not depleted detection deglitch time	$V_{(BAT)}$ rising		1		s

ELECTRICAL CHARACTERISTICS (continued)

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ADAPTER DETECT COMPARATOR (ACDET)						
$V_{(ACD)}$	AC adapter detect threshold	$V_{(ACDET)}$ rising, When adapter detected, VREF5 is enabled, and REGN regulates to 6 V	1.176	1.2	1.224	V
$V_{(ACDH)}$	AC adapter detect hysteresis	$V_{(ACDET)}$ falling		15		mV
	AC adapter detected deglitch time	$V_{(ACDET)}$ rising		8		ms
	AC adapter not detected deglitch time	$V_{(ACDET)}$ falling		1		µs
AC ADAPTER (ACP) - BATTERY (BAT) COMPARATOR						
$V_{(ACP-BAT)}$	ACP voltage above BAT voltage threshold	$V_{(ACP)}$ falling with respect to $V_{(BAT)}$		250	300	mV
$V_{(ACP-BAT)}$	Hysteresis	$V_{(ACP-BAT)}$ rising with respect to $V_{(BAT)}$		50		mV
	$V_{(ACP-BAT)}$ falling below threshold deglitch time	$V_{(ACP)}$ falling with respect to $V_{(BAT)}$		16		µs
	$V_{(ACP-BAT)}$ rising above threshold deglitch time	$V_{(ACP-BAT)}$ rising with respect to $V_{(BAT)}$		8		ms
SYSTEM (SYS) - BATTERY (BAT) COMPARATOR						
$V_{(SYS-BAT)}$	System voltage above pack voltage at $V_{(VS,BAT)}$ > $V_{(SYS)}$	$V_{(SYS)}$ falling with respect to $V_{(BAT)}$		250	300	mV
$V_{(SYS-BAT)}$	Hysteresis	$V_{(SYS-BAT)}$ rising with respect to $V_{(BAT)}$		50		mV
	$V_{(SYS-BAT)}$ falling below threshold deglitch time	$V_{(SYS)}$ falling with respect to $V_{(BAT)}$		1		µs
	$V_{(SYS-BAT)}$ rising above threshold deglitch time	$V_{(SYS-BAT)}$ rising with respect to $V_{(BAT)}$		8		ms
BATTERY SHORTED COMPARATOR						
$V_{(BATSHORT)}$	Battery shorted threshold(2)	$V_{(BAT)}$ falling, Programmed $V_{(BAT)}$ = 9V	3.230	3.4	3.570	V
		$V_{(BAT)}$ falling, Programmed $V_{(BAT)}$ = 12-14.4V	4.845	5.1	5.355	V
		$V_{(BAT)}$ falling, Programmed $V_{(BAT)}$ = 16-19.2V	6.460	6.8	7.140	V
$V_{(SHRT_HYS)}$	Hysteresis	$V_{(BAT)}$ rising		200		mV/cell
	Battery shorted deglitch time	$V_{(BAT)}$ rising/falling		1		s
BYPASS P-Channel MOSFET DRIVER ($\overline{BYPASS}$)						
$R_{(DS_BYP)\ Hi}$	$\overline{BYPASS}$ off-state resistance	Driver output = HI, $\overline{BYPASS}$ = $V_{(PVCC)}$, $V_{(PVCC)}$ = 18 V		1	2	kΩ
$R_{(DS_BYP)\ Lo}$	$\overline{BYPASS}$ on-state resistance	Driver output = LO, $\overline{BYPASS}$ = $V_{(PVCC)}$ - $V_{(REGBYPASS)}$, $V_{(PVCC)}$ = 18 V		1	2	kΩ
$V_{(REGBYPASS)}$	Drive regulator turn-on voltage for $\overline{BYPASS}$ with respect to $V_{(PVCC)}$	$V_{(VCC,\ \overline{BYPASS})}$, $V_{(VCC)}$ > 13 V, $I_{(\overline{BYPASS})}$ = 5 mA	-5	-6	-7.5	V
AC ADAPTER P-Channel MOSFET DRIVER ($\overline{ACDRV}$)						
$R_{(DS_AC)\ Hi}$	$\overline{ACDRV}$ off-state resistance	Driver output = HI, $\overline{ACDRV}$ = PVCC, $V_{(PVCC)}$ = 18 V		100	150	Ω
$R_{(DS_AC)\ Lo}$	$\overline{ACDRV}$ on-state resistance	Driver output = LO, $\overline{ACDRV}$ =$V_{(PVCC)}$-$V_{(REGAC)}$, $V_{(PVCC)}$ = 18 V		10	20	kΩ
$V_{(REGAC)}$	Drive regulator turn-on voltage for $\overline{ACDRV}$ with respect to $V_{(PVCC)}$	$V_{(VCC,\ \overline{ACDRV})}$, $V_{(VCC)}$ > 13 V, $I_{(\overline{ACDRV})}$ = 5 mA	-5	-6.5	-7.5	V
BATTERY P-Channel MOSFET DRIVER ($\overline{BATDRV}$)						
$R_{(DS_BAT)\ Hi}$	$\overline{BATDRV}$ off-state resistance	Driver output = HI, $V_{(PVCC)}$ = 18 V		100	150	Ω
$R_{(DS_BAT)\ Lo}$	$\overline{BATDRV}$ on-state resistance	Driver output = LO, $\overline{BATDRV}$=$V_{(PVCC)}$-$V_{(REGBAT)}$, $V_{(PVCC)}$ = 18 V		10	20	kΩ
$V_{(REGBAT)}$	Drive regulator negative turn-on voltage for $\overline{BATDRV}$ with respect to $V_{(SYS)}$	$V_{(VCC,\ \overline{BATDRV})}$, $V_{(VCC)}$ > 13 V, $I_{(\overline{BATDRV})}$ = 5 mA	-5	-6.5	-7.5	V
SYSTEM POWER SELECTOR TIMING						
	Dead time when switching between ACDRV and BATDRV	No load at ACDRV and BATDRV		1		µs
BYPASS SWITCH TIMING						
	Delay to turn-off BYPASS			1		µs

(2) For the **bq24721**: When BAT falls below the $V_{(BATSHORT)}$ threshold, the charger continues regulating at the programmed current down to zero volts on BAT; then after 1 second deglitch time, the charge current automatically changes to 1/8 the programmed charge current. The charge current automatically changes from 1/8 the programmed charge current to the full programmed charge current when BAT voltage rises above ($V_{(BATSHORT)}$ + 200 mV hysteresis), after 1 second deglitch time.

ELECTRICAL CHARACTERISTICS (continued)

8 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, 0°C ≤ T_J ≤ 125°C, all voltages with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM HIGH-SIDE N-Channel MOSFET DRIVER (HIDRV), bq24721						
$R_{(DS_HIDRV)\ Hi}$	High-side on-state resistance	HSD switch on, HIDRV = HI, $V_{(BOOST,PH)}$ = 5.5 V		2.2	3	Ω
$R_{(DS_HIDRV)\ Lo}$	High-side off-state resistance	HSD switch off, HIDRV = LO, $V_{(BOOST,PH)}$ = 5.5 V		1.5	2.5	Ω
PWM HIGH-SIDE N-Channel MOSFET DRIVER (HIDRV), bq24721C						
$R_{(DS_HIDRV)\ Hi}$	High-side on-state resistance	HSD switch on, HIDRV = HI, $V_{(BOOST,PH)}$ = 5.5 V		4.5	8.6	Ω
$R_{(DS_HIDRV)\ Lo}$	High-side off-state resistance	HSD switch off, HIDRV = LO, $V_{(BOOST,PH)}$ = 5.5 V		1.5	2.6	Ω
PWM LOW-SIDE N-Channel MOSFET DRIVER (LODRV), bq24721						
$R_{(DS_LODRV)\ Hi}$	Low-side on-state resistance	LSD switch on, LODRV = HI, $V_{(PVCC)}$ = 7 V		2.2	3	Ω
$R_{(DS_LODRV)\ Lo}$	Low-side off-state resistance	LSD switch off, LODRV = LO, $V_{(PVCC)}$ = 7 V		1.5	2.5	Ω
PWM LOW-SIDE N-Channel MOSFET DRIVER (LODRV), bq24721C						
$R_{(DS_LODRV)\ Hi}$	Low-side on-state resistance	LSD switch on, LODRV = HI, $V_{(PVCC)}$ = 7 V		4.5	8.6	Ω
$R_{(DS_LODRV)\ Lo}$	Low-side off-state resistance	LSD switch off, LODRV = LO, $V_{(PVCC)}$ = 7 V		1.5	2.6	Ω
PWM LOW-SIDE DRIVER REGULATOR (REGN)						
$V_{O(HREGN)}$	REGN output voltage	V(REGN) at I(REGN) = 10 mA, sourcing, Adapter detected ($V_{(ACDET)}$ > $V_{(ACD)}$), $V_{(PVCC)}$ > 7 V	5.5	6	6.5	V
		V(REGN) at I(REGN) = 10 mA, sourcing, Adapter not detected, ($V_{(ACDET)}$ < $V_{(ACD)}$), $V_{(PVCC)}$ > 7 V		4.2		V
$I_{O(REGN_SW)}$	REGN output current while charger switching	2 times 25 nC load, fs = 300 kHz		15		mA
		2 times 25 nC load, fs = 500 kHz		25		mA
$I_{(REGN_LIM)}$	REGN Current limit Adapter detected	VREGN = 5 V Adapter detected ($V_{(ACDET)}$ > $V_{(ACD)}$), $V_{(PVCC)}$> 7 V		100		mA
		VREGN = 0 V, shorted Adapter detected ($V_{(ACDET)}$ > $V_{(ACD)}$), $V_{(PVCC)}$> 7 V		13.3		mA
	REGN Current limit Adapter not detected	VREGN = 4.2 V Adapter not detected, ($V_{(ACDET)}$ < $V_{(ACD)}$), $V_{(PVCC)}$> 7 V		15		mA
PWM DRIVERS TIMING						
	Dead time when switching between LSD and HSD, no load at LSD and HSD			30		ns
PWM OSCILLATOR						
$V_{(RAMPLO)}$	PWM oscillator ramp voltage , low value	0% duty cycle occurs below this threshold		0.35		V
$V_{(RAMPHI)}$	PWM oscillator ramp voltage , high value	near 100% duty cycle occurs above this threshold			3	V
$V_{PP(RAMP)}$	PWM ramp peak-to-peak amplitude			0.1×VCC		V
$V_{(RAMPCL)}$	PWM oscillator ramp clamp voltage			3.5		V
F_S	PWM oscillator frequency (300 kHz)		265	300	345	kHz
	PWM oscillator frequency (500 kHz)		425	500	575	kHz
INTERNAL SOFT START (8 steps to Ireg)						
	SRSET pin voltage number of steps during soft start.	Eight steps of charge current regulation to get to programmed value (SRSET = 1 V).		8		step
	Step Duration.	Eight steps of charge current regulation to get to programmed value (SRSET = 1 V).	0.8	1	1.2	ms/step
CHARGER SECTION POWER-UP SEQUENCING						
	Time delay between power up of charger block references (first) and start charge (second)			1		ms
	Time delay from adapter detected until ACDRV enable and charger block enable			500		ms

TYPICAL CHARACTERISTICS

VREF5 LOAD REGULATION vs LOAD CURRENT

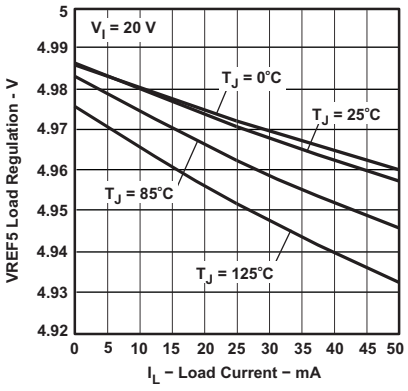


Figure 1.

VREF5 LINE REGULATION vs INPUT VOLTAGE

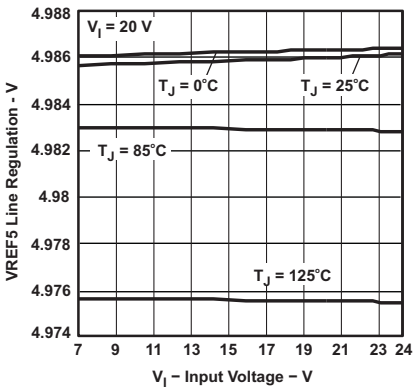


Figure 2.

VREF5 CURRENT LIMIT vs JUNCTION TEMPERATURE

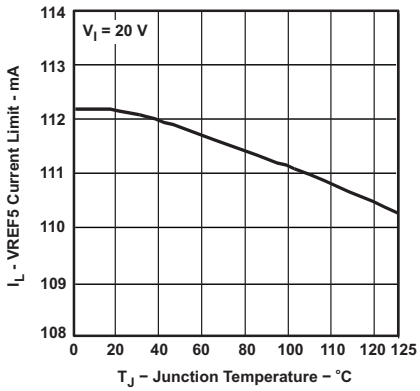


Figure 3.

REGN LOAD REGULATION vs LOAD CURRENT

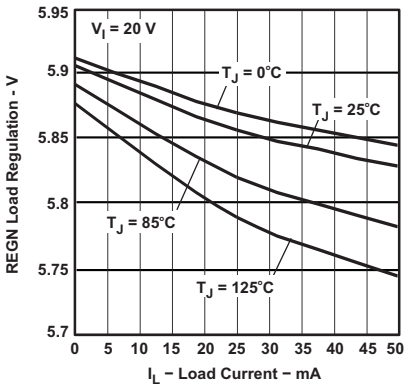


Figure 4.

REGN LINE REGULATION vs INPUT VOLTAGE

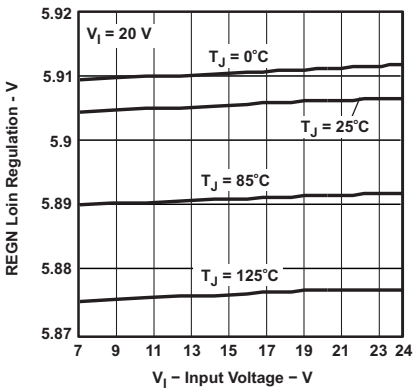


Figure 5.

REGN CURRENT LIMIT vs JUNCTION TEMPERATURE

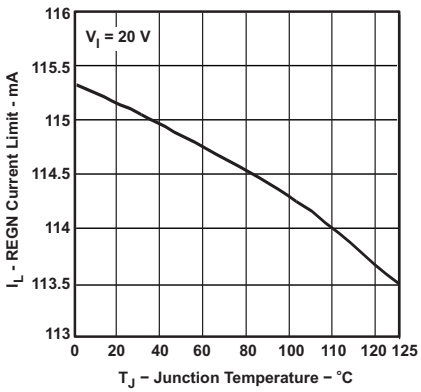


Figure 6.

REGN CURRENT LIMIT vs FORCED REGN VOLTAGE

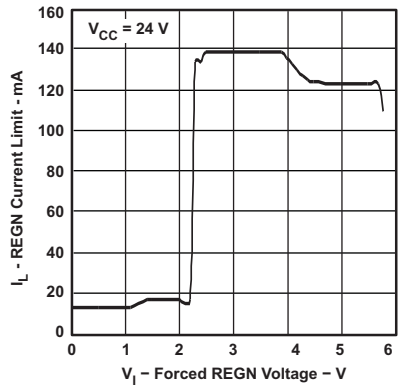


Figure 7.

QUIESCENT CURRENT, NO ADAPTER vs JUNCTION TEMPERATURE

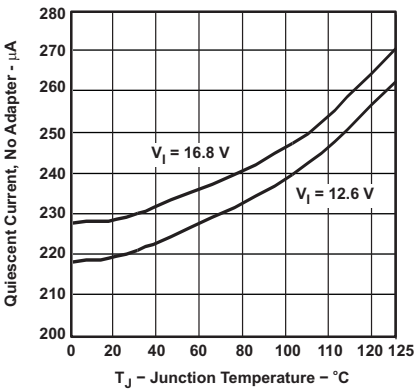


Figure 8.

QUIESCENT CURRENT, WITH ADAPTER vs JUNCTION TEMPERATURE

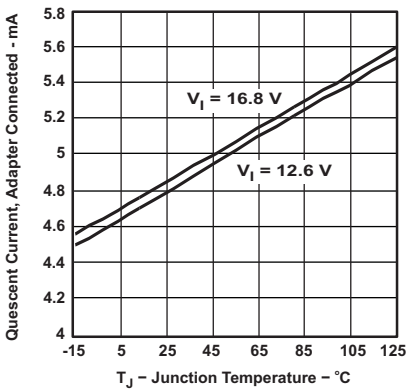


Figure 9.

TYPICAL CHARACTERISTICS (continued)

ACDET THRESHOLD vs JUNCTION TEMPERATURE

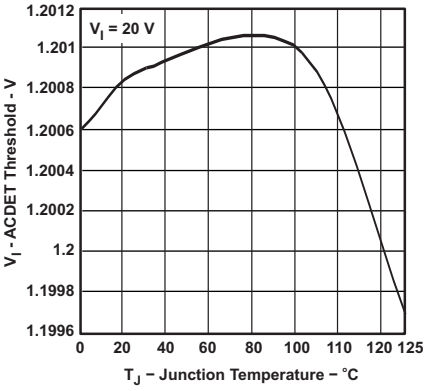


Figure 10.

ACDET HYSTERESIS vs JUNCTION TEMPERATURE

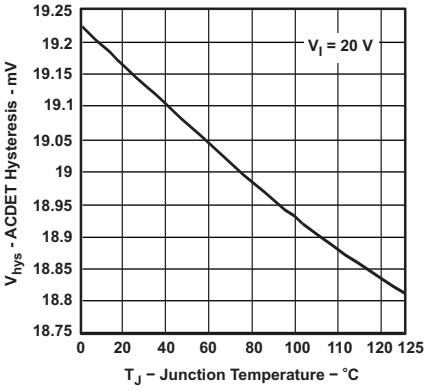


Figure 11.

HIDRV, $r_{DS(on)}$, PULL UP vs JUNCTION TEMPERATURE

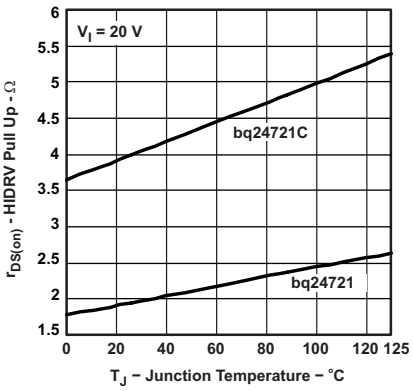


Figure 12.

HIDRV, $r_{DS(on)}$, PULL DOWN vs JUNCTION TEMPERATURE

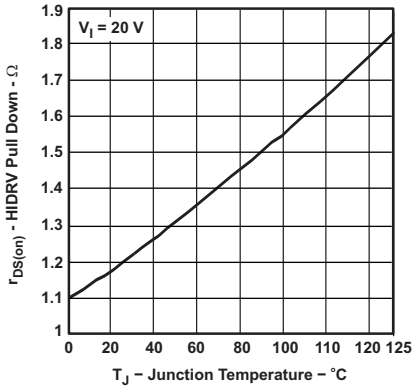


Figure 13.

LODRV, $r_{DS(on)}$, PULL UP vs JUNCTION TEMPERATURE

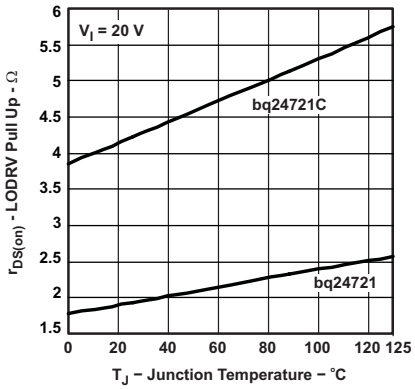


Figure 14.

LODRV, $r_{DS(on)}$, PULL DOWN vs JUNCTION TEMPERATURE

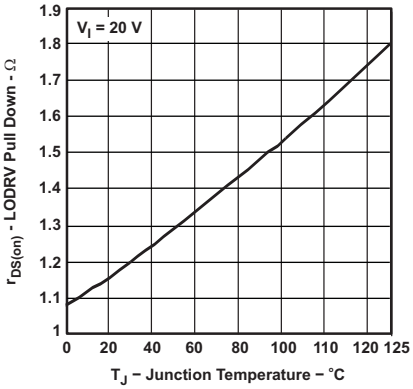


Figure 15.

BATTERY VOLTAGE REGULATION ACCURACY vs BATTERY VOLTAGE

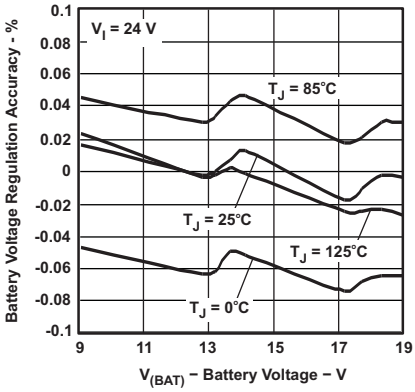


Figure 16.

BATTERY VOLTAGE REGULATION vs JUNCTION TEMPERATURE

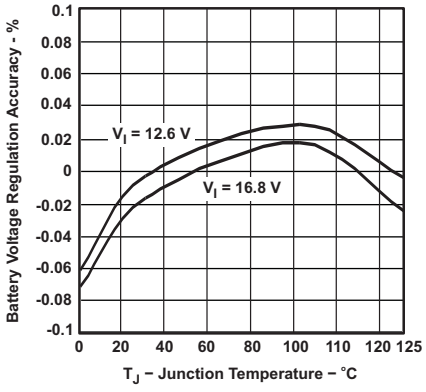


Figure 17.

CHARGE CURRENT REGULATION ACCURACY vs SRP-SRN VOLTAGE

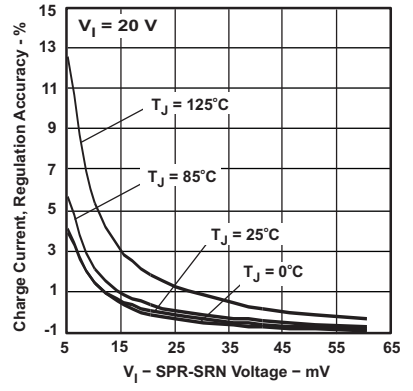


Figure 18.

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT REGULATION (DPM) ACCURACY vs ACP-ACN VOLTAGE

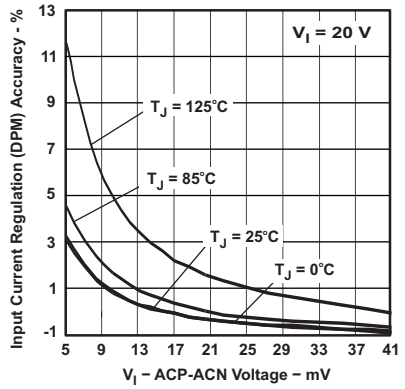


Figure 19.

INPUT CURRENT REGULATION (DPM) ACCURACY vs INPUT VOLTAGE

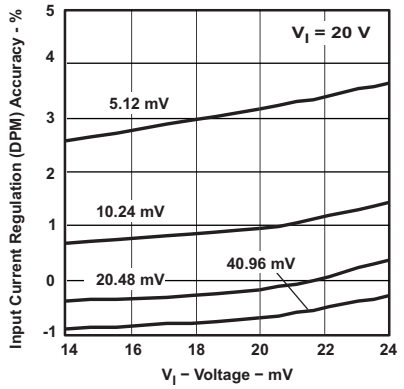


Figure 20.

I_O = DPM CURRENT SENSE AMPLIFIER ACCURACY vs ACP-ACN VOLTAGE

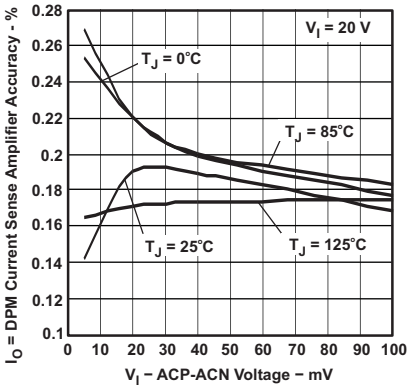


Figure 21.

I_O = DPM CURRENT SENSE AMPLIFIER OFFSET vs JUNCTION TEMPERATURE

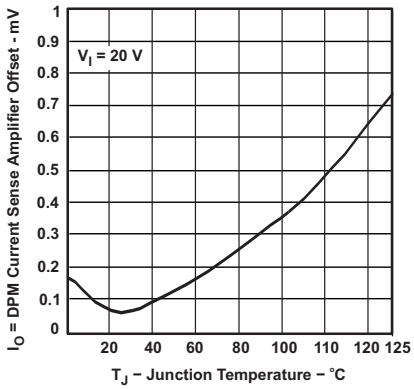


Figure 22.

I_O = ADAPTER OUTPUT CURRENT LIMIT vs JUNCTION TEMPERATURE

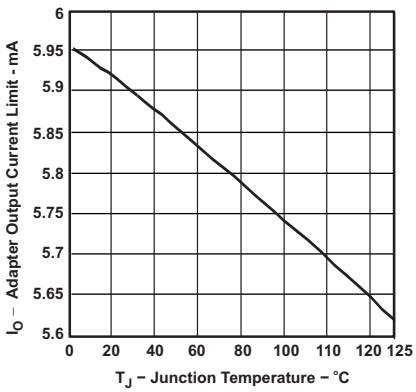


Figure 23.

I_O = CHARGE SENSE AMPLIFIER ACCURACY vs SRP-SRN VOLTAGE

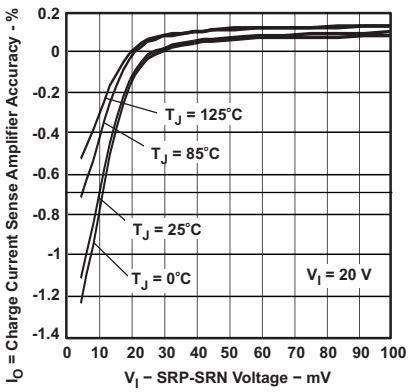


Figure 24.

I_O = CHARGE CURRENT LIMIT vs JUNCTION TEMPERATURE

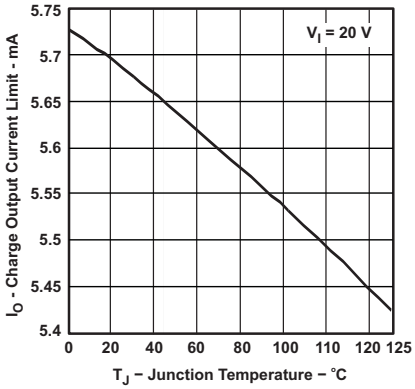


Figure 25.

300-kHz SWITCHING FREQUENCY vs INPUT VOLTAGE

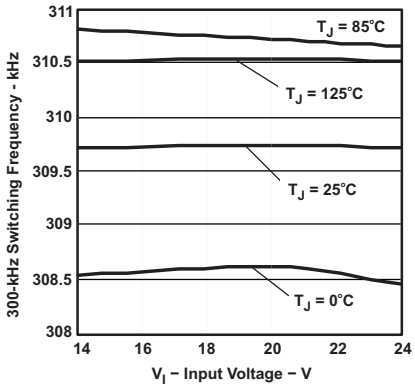


Figure 26.

300-kHz SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

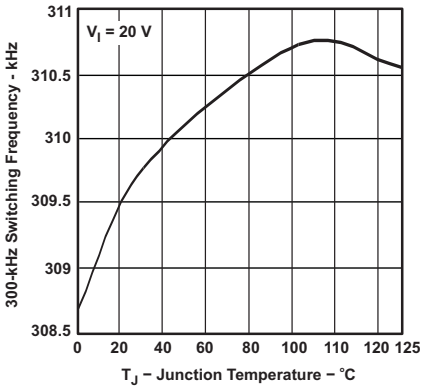


Figure 27.

TYPICAL CHARACTERISTICS (continued)

500-kHz SWITCHING FREQUENCY vs INPUT VOLTAGE

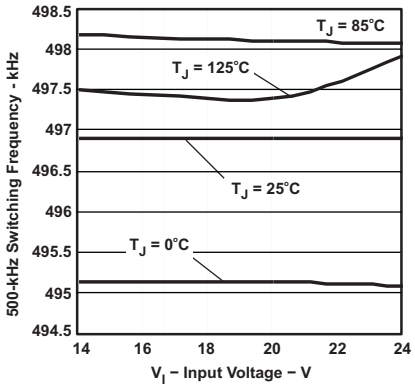


Figure 28.

500-kHz SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

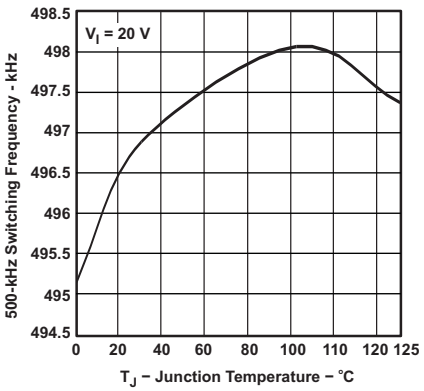


Figure 29.

THERMISTOR LTF THRESHOLD vs JUNCTION TEMPERATURE

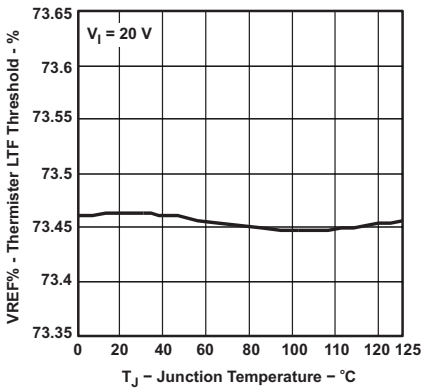


Figure 30.

THERMISTOR LTF THRESHOLD vs JUNCTION TEMPERATURE

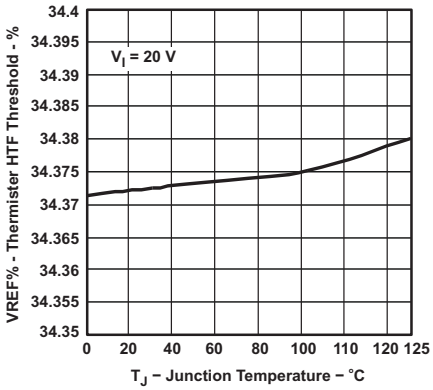


Figure 31.

THERMISTOR TCO THRESHOLD vs JUNCTION TEMPERATURE

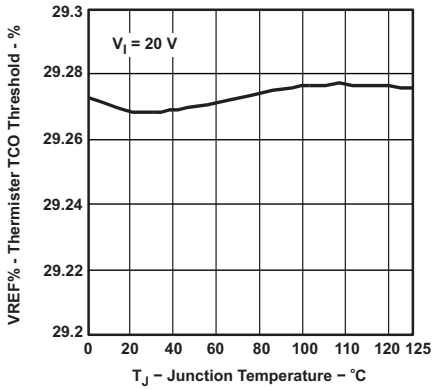


Figure 32.

THERMISTOR TSDET THRESHOLD vs JUNCTION TEMPERATURE

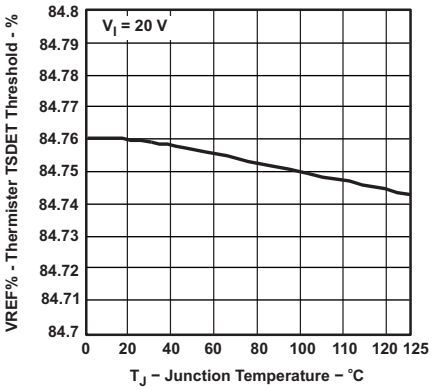


Figure 33.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
BATTERY CHARGE CURRENT

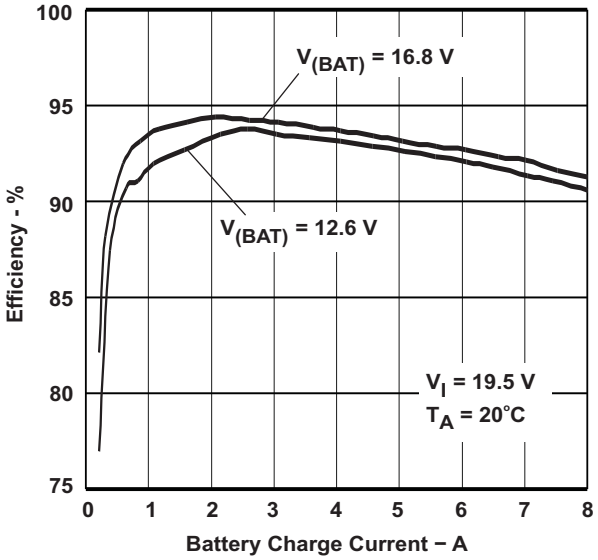


Figure 34.

REGULATION CURRENT
vs
SYSTEM CURRENT

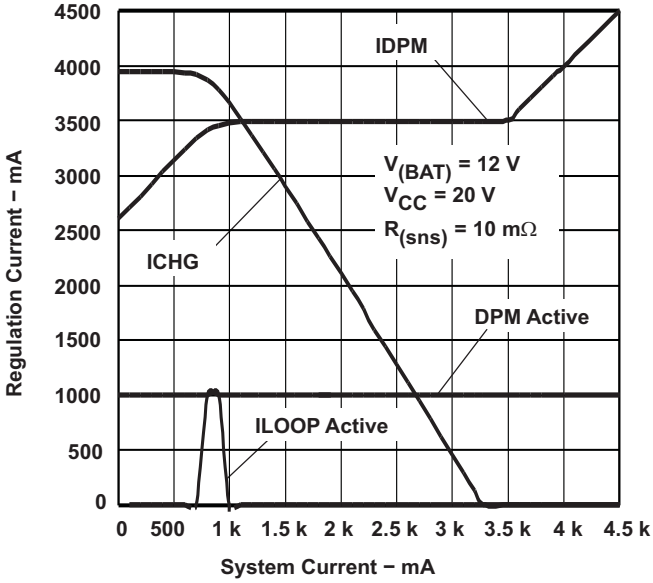


Figure 35.

TRANSIENT SYSTEM LOAD

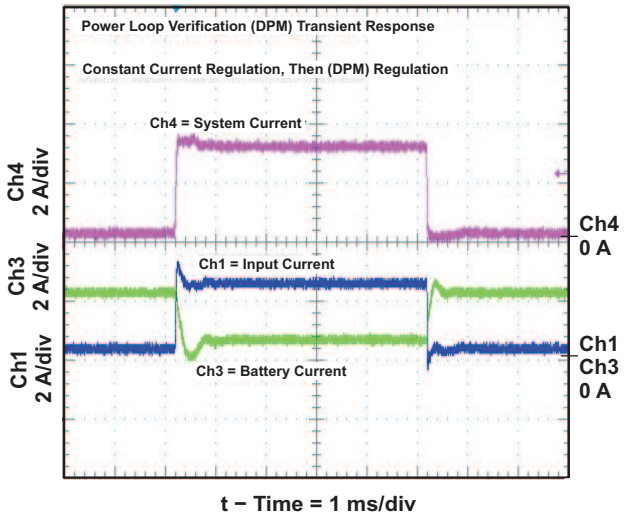


Figure 36.

SYSTEM SELECTOR GATE DRIVES AFTER ACDET

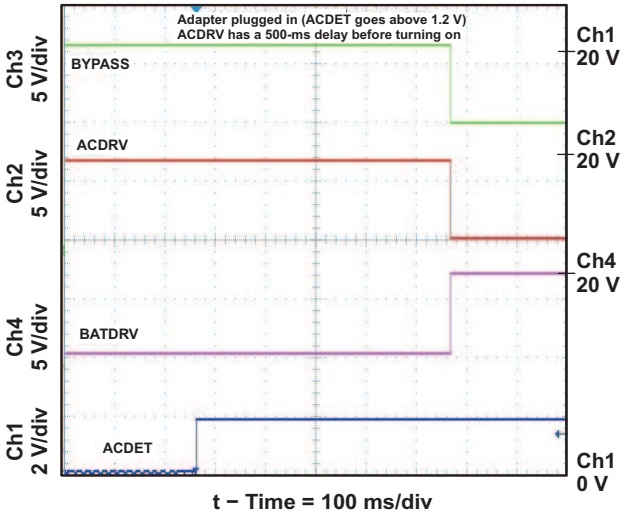


Figure 37.

TYPICAL CHARACTERISTICS (continued)

SYSTEM SELECTOR ADAPTER INSERTION

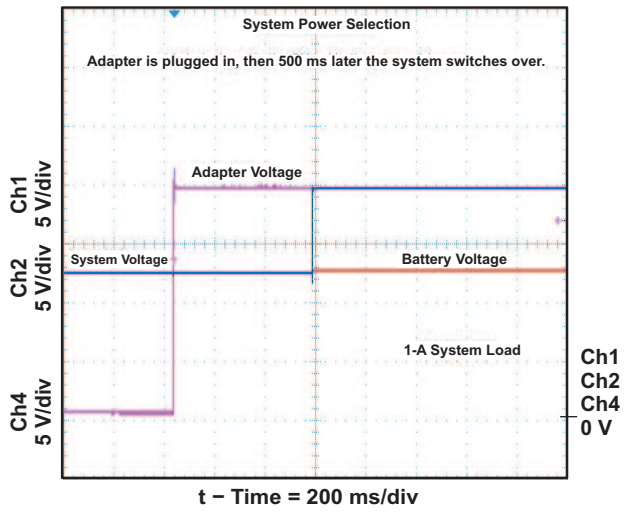


Figure 38.

SYSTEM SELECTOR ADAPTER REMOVAL

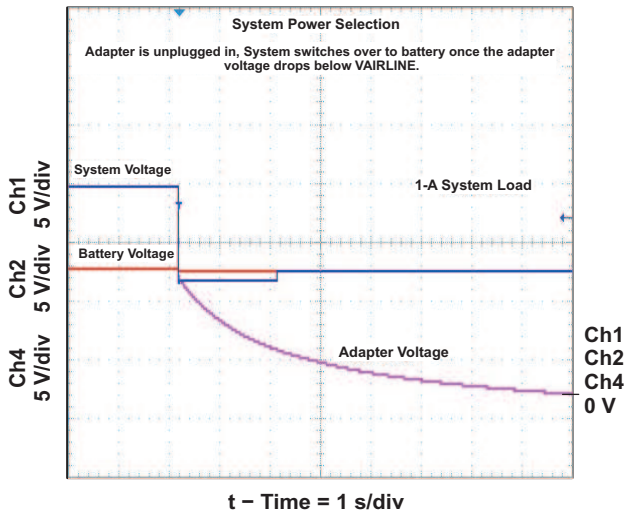


Figure 39.

REGN VREF5 POWER UP

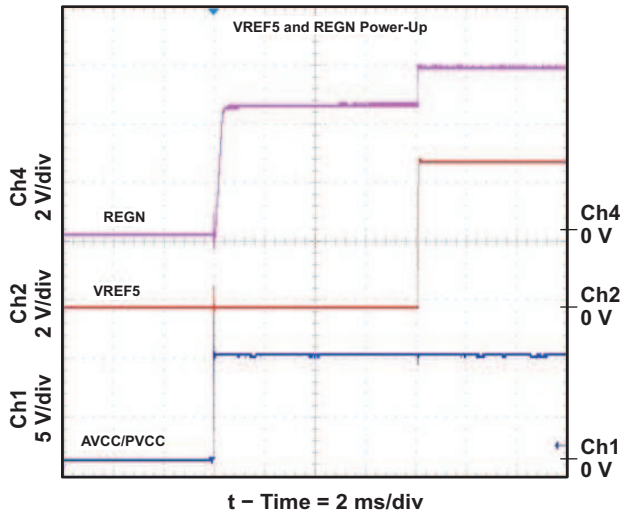


Figure 40.

SOFTSTART CHARGE CURRENT

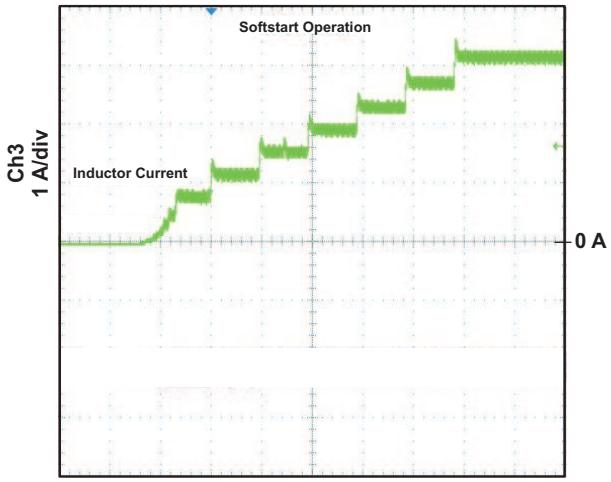


Figure 41.

TYPICAL CHARACTERISTICS (continued)

NONSYNCHRONOUS TO SYNCHRONOUS TRANSITION

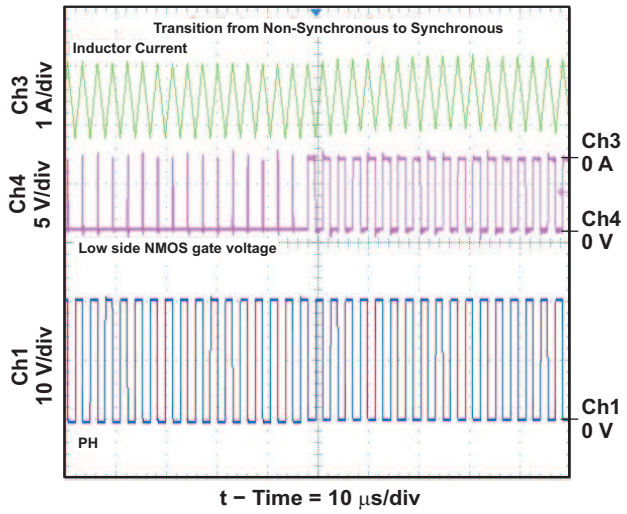


Figure 42.

SYNCHRONOUS TO NONSYNCHRONOUS TRANSITION

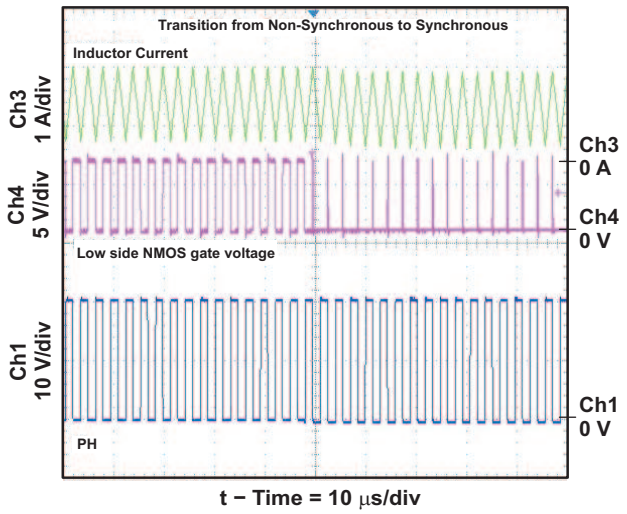


Figure 43.

NEAR 100% DUTY CYCLE BTST RECHARGE PULSE

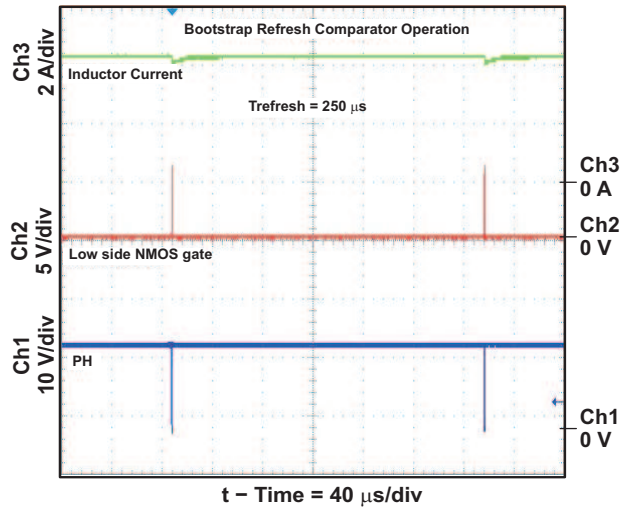


Figure 44.

BATTERY SHORT RESPONSE

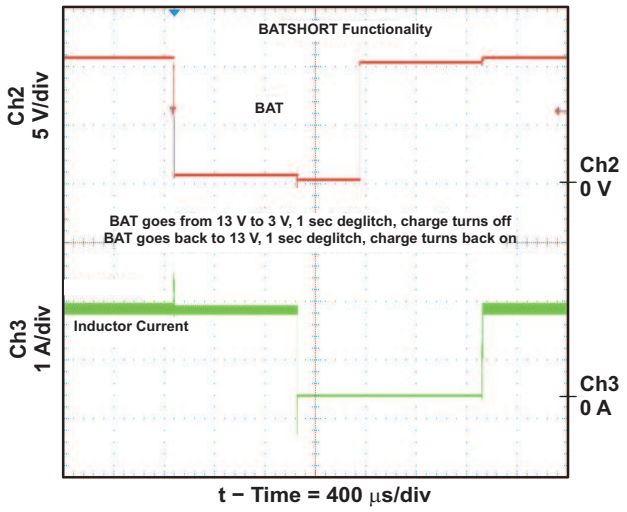


Figure 45.

TYPICAL CHARACTERISTICS (continued)

CHARGE OVERCURRENT

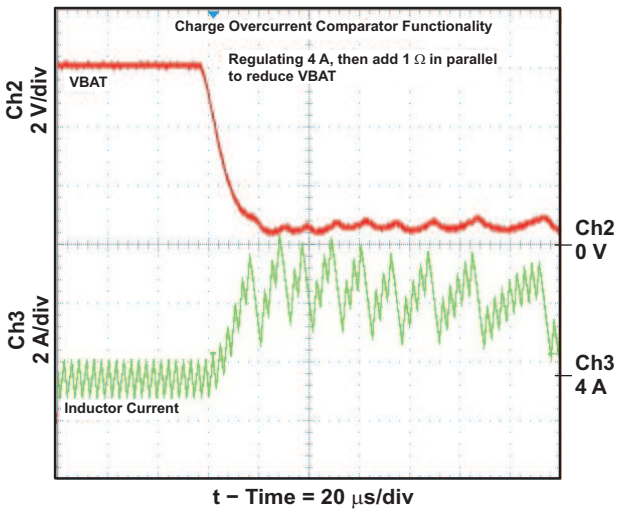


Figure 46.

ACOC ACDRV TURN OFF (32-μs DEGLITCH)

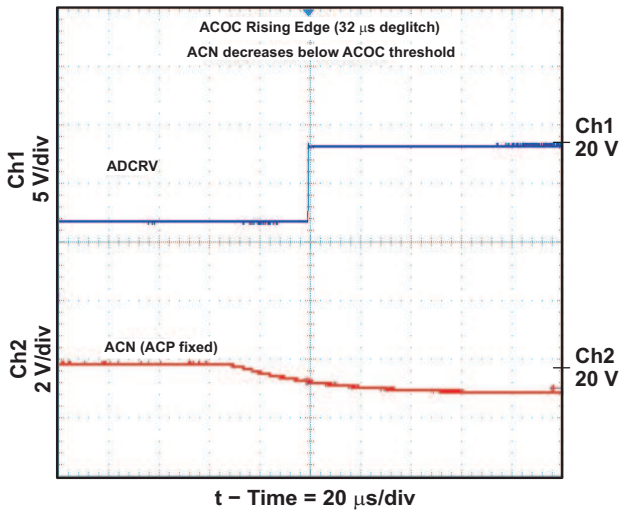


Figure 47.

ACOC ACDRV TURN ON (500-μs DEGLITCH)

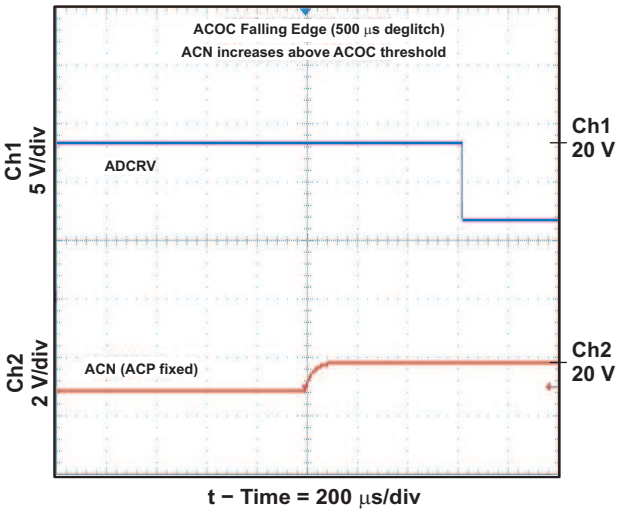


Figure 48.

SWITCHING CONTINUOUS CURRENT MODE (CCM)

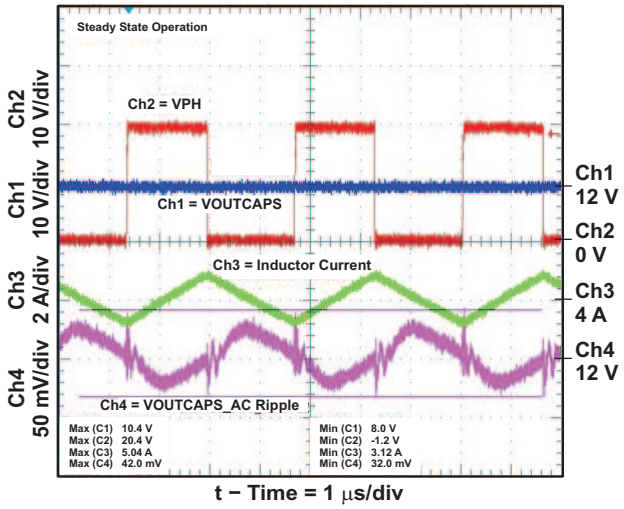


Figure 49.

TYPICAL CHARACTERISTICS (continued)

SWITCHING DISCONTINUOUS CURRENT MODE VS (DCM)

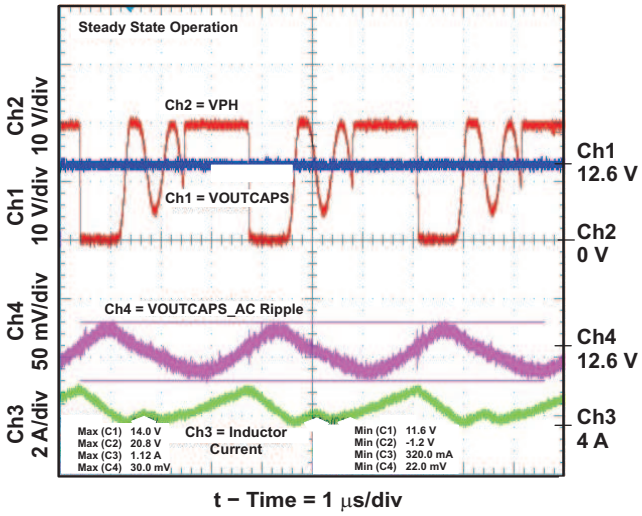


Figure 50.

SIMPLIFIED BLOCK DIAGRAM

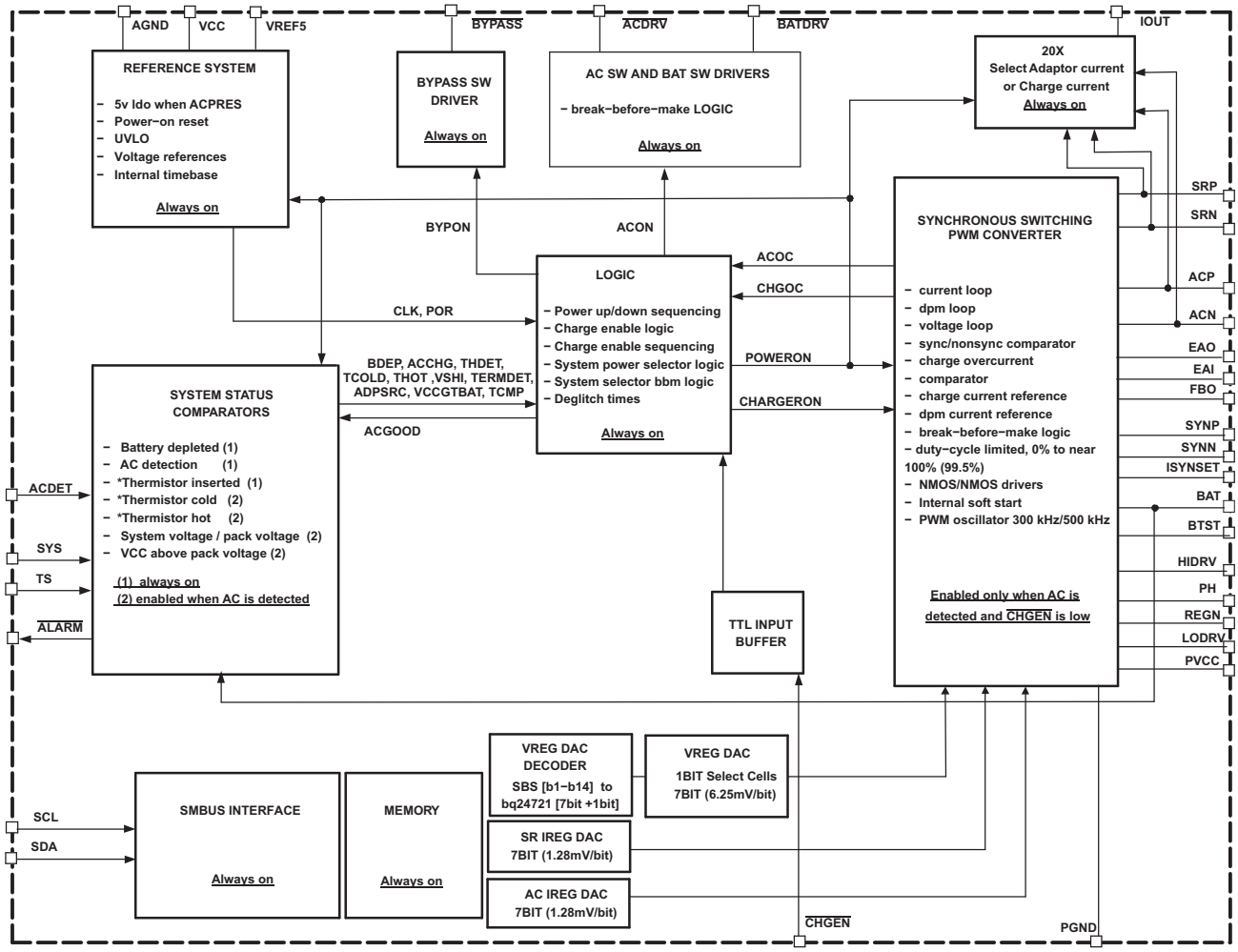


Figure 51. bq24721 SBS-Like SMBus Controlled Simplified Block Diagram

TYPICAL APPLICATION bq24721

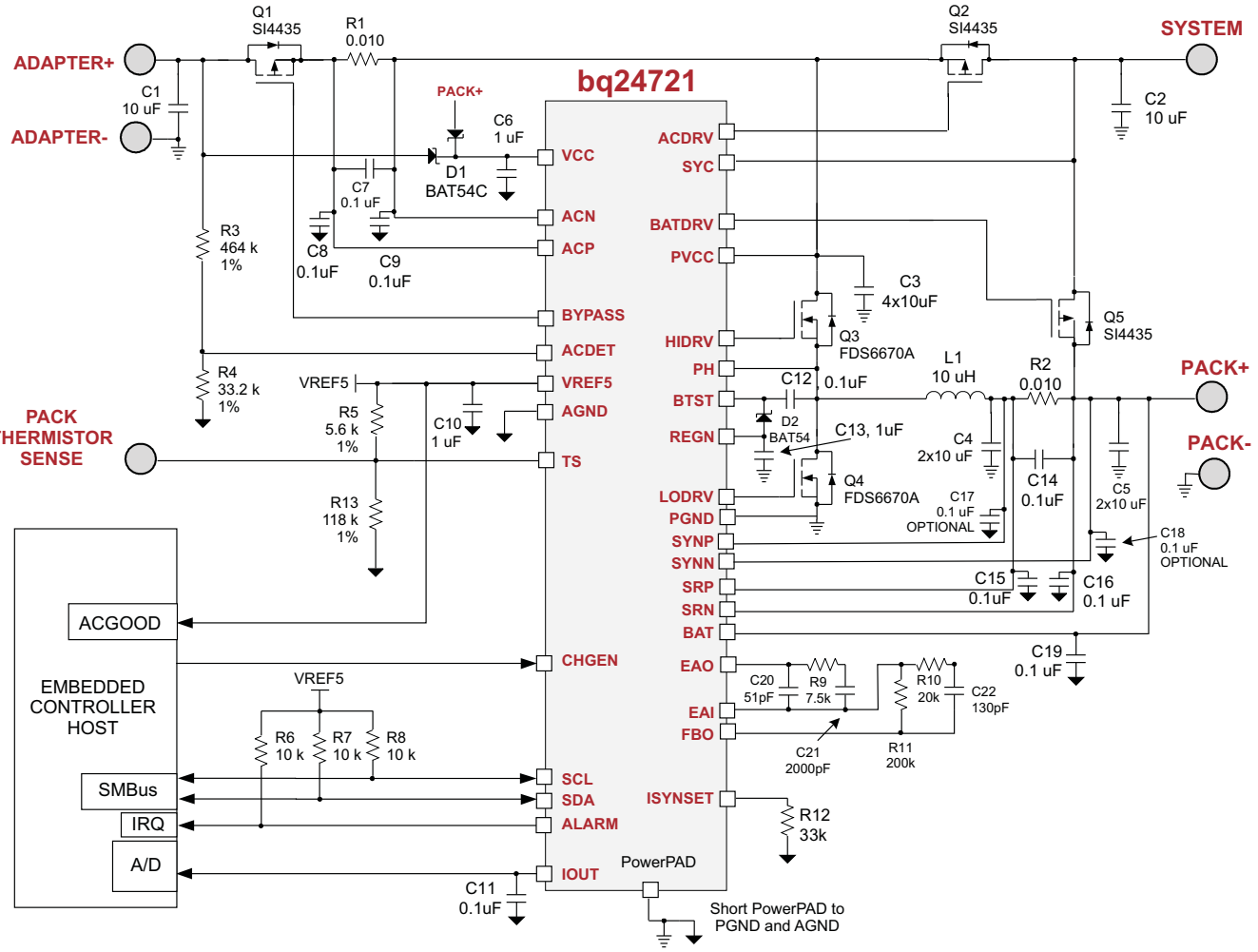


Figure 52. bq24721 SBS-Like SMBus Host Control With System Power Selector (bq24721 With TS Thermistor Sense Input Pin)

BOM Key Components (For Figure 52, bq24721 Typical Application Circuit)

Reference Designator	Qty	Description(1)
Q3	1	N-channel MOSFET, 30V, 12.5A, SO-8, FDS6680A
Q4	1	N-channel MOSFET, 30V, 13A, SO-8, FDS6670A
Q1, Q2, Q5	3	P-channel MOSFET, -30V,-6A, SO-8, Vishay-Siliconix, Si4435
D1	1	Diode, Dual Schottky, 30V, 200mA, SOT23, Fairchild, BAT54C
D2	1	Diode, Single Schottky, 30V, 200mA, SOT23, Fairchild, BAT54
L1	1	Inductor, 10µH, 7A, 31mΩ, Vishay-Dale, IHLP5050FD-01
R1, R2	2	Sense Resistor, 10 mΩ, 1%, 1W, 2010, Vishay-Dale, WSL2010R0100F
C1, C2, C3, C4, C5	10	Capacitor, Ceramic, 10µF, 35V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C6, C10, C13	3	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C7, C8, C9, C12, C14, C15, C16, C19, (C17 and C18 optional)	10	Capacitor, Ceramic, 0.1µF, 50V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C20	1	Capacitor, Ceramic, 51pF, 50V, 5%, NPO, 0603

(1) The manufacturer's part number are used for test purposes only.

BOM Key Components (For Figure 52, bq24721 Typical Application Circuit) (continued)

Reference Designator	Qty	Description(1)
C21	1	Capacitor, Ceramic, 2000pF, 50V, 5%, X7R, 0805
C22	1	Capacitor, Ceramic, 130pF, 50V, 5%, NPO, 0603
R3	1	Resistor, Chip, 464kΩ, 1/16W, 1%, 0402
R4	1	Resistor, Chip, 33.2kΩ, 1/16W, 1%, 0402
R12	1	Resistor, Chip, 33kΩ, 1/16W, 5%, 0402
R9	1	Resistor, Chip, 7.54kΩ, 1/16W, 1%, 0402
R10	1	Resistor, Chip, 20kΩ, 1/16W, 1%, 0402
R11	1	Resistor, Chip, 200kΩ, 1/16W, 1%, 0402
R6, R7, R8	3	Resistor, Chip, 10kΩ, 1/16W, 5%, 0402
R5	1	Resistor, Chip, 5.6kΩ, 1/16W, 1%, 0402
R13	1	Resistor, Chip, 118kΩ, 1/16W, 1%, 0402

Typical bq24721 Narrow VDC (NVDC) Application (2 sense resistors)

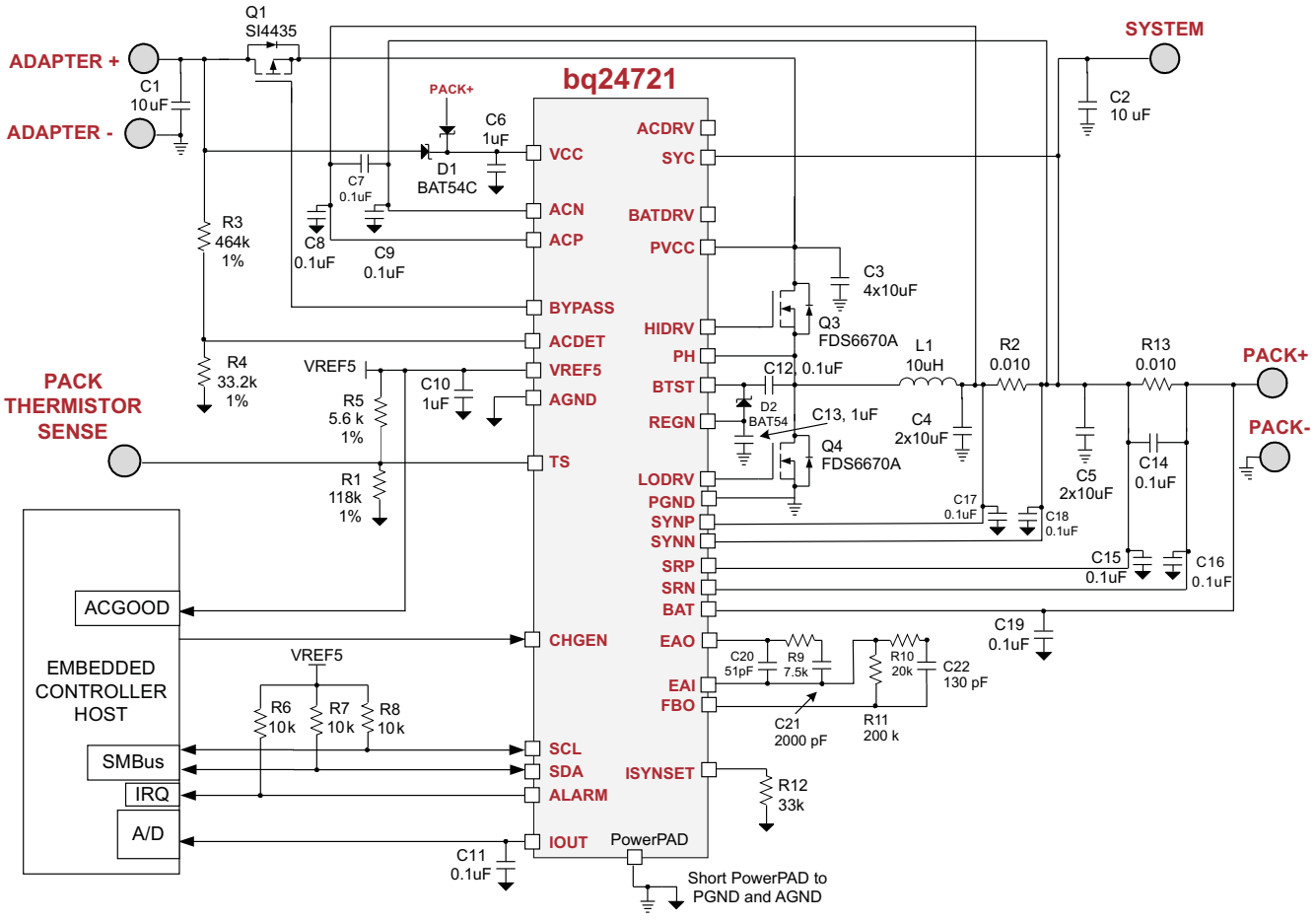


Figure 53. bq24721 SBS-Like SMBus Host Control, NVDC (no system power selector) With 2 Sense Resistors. ACP and ACN Regulating Converter Current Instead of Input Current

Typical bq24721 Narrow VDC (NVDC) Application (3 sense resistors)

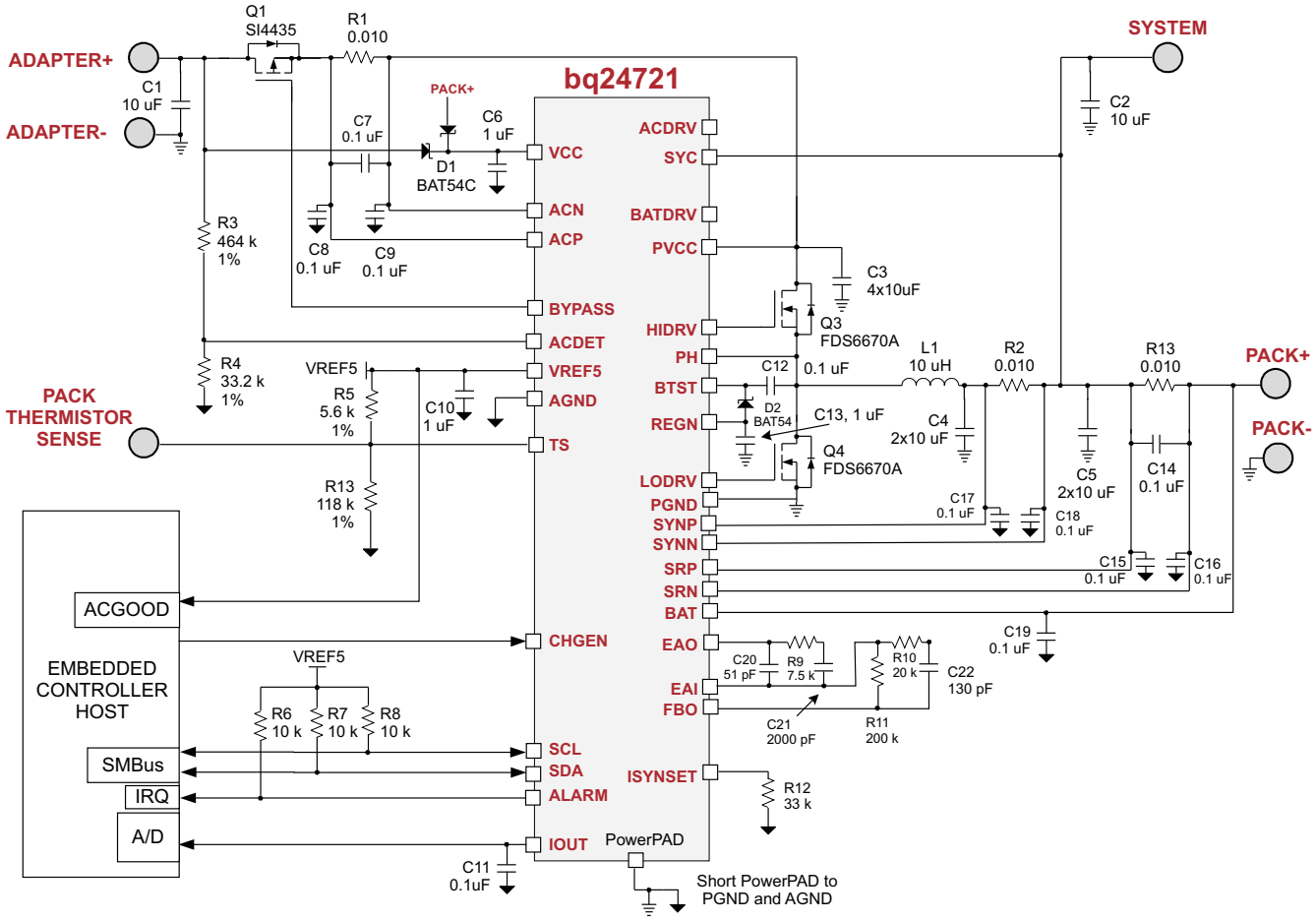


Figure 54. bq24721 SBS-Like SMBus Host Control, NVDC (no system power selector) With 3 Sense Resistors

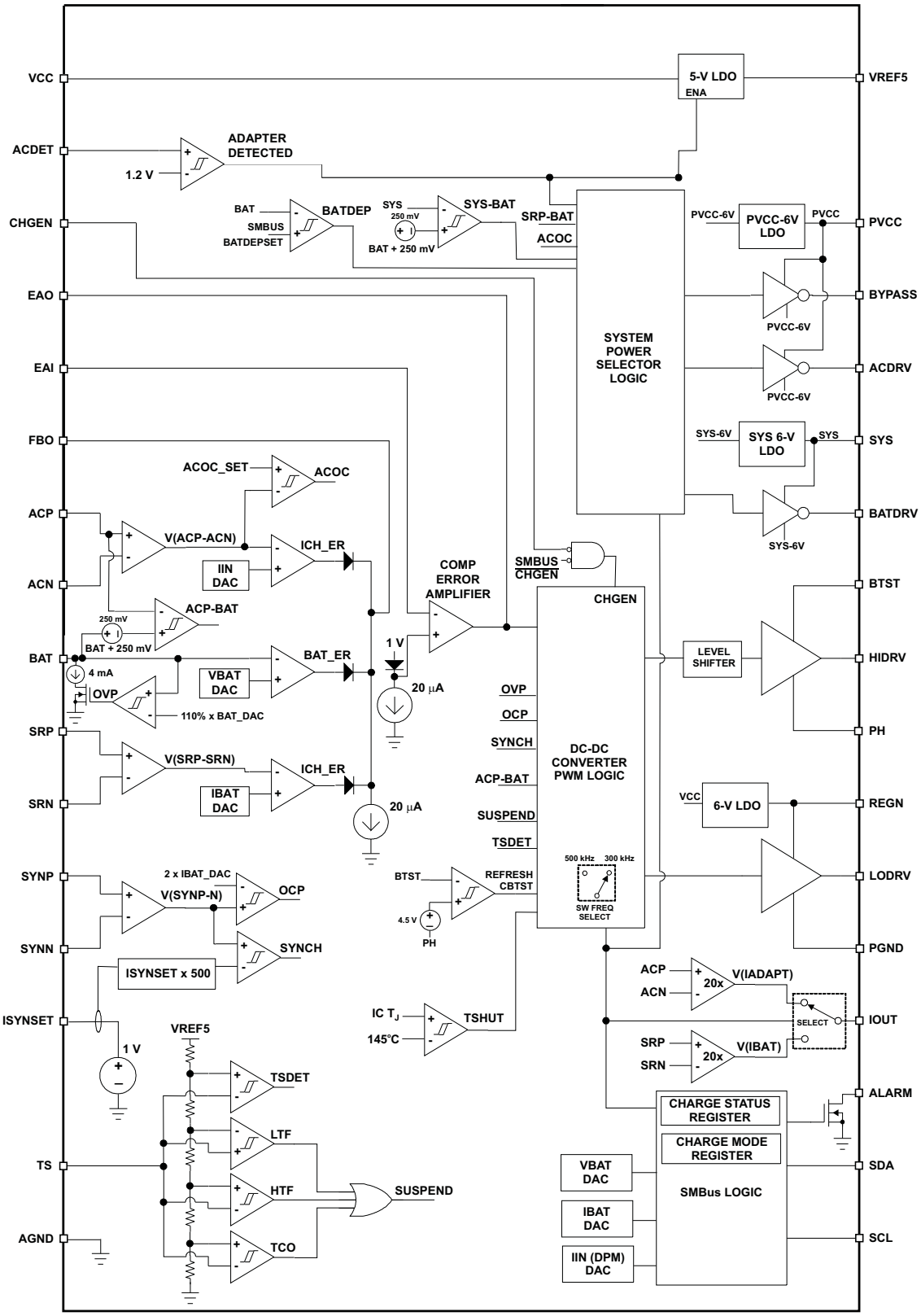


Figure 55. bq24721 Functional Block Diagram

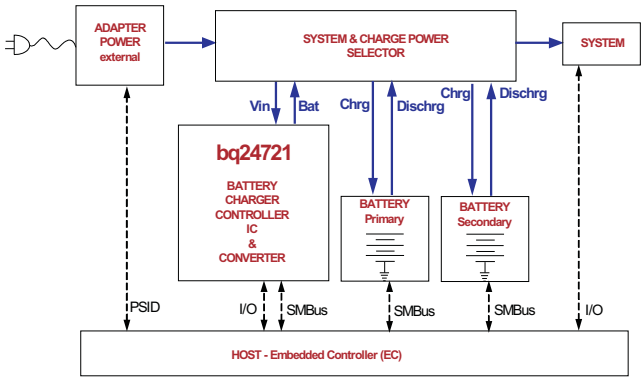


Figure 56. Host Controller

BLOCK DESCRIPTION

Detail Block Diagram

The bq24721 charge controller can be used to charge Li-Ion, NiMH, or NiCd batteries. The high efficiency synchronous buck controller uses n-channel power MOSFETs for both the high-side control device and the low-side synchronous device. The controller offers high regulation accuracy of the charge current, battery voltage, and input current limits. The low offset of the current loops allow using sense resistors with low-value, such as 10 mΩ.

An embedded controller host programs the battery voltage, charge current, and input current regulation limit thresholds through an SMBus interface using SBS-like DAC registers. The embedded host can control the operation of the charger through a Charge Control (0x12) register, and monitor the status of the charger through a Charger Status (0x13) register.

The voltage loop regulates the battery voltage to the programmed value, and prevents the voltage from exceeding that value when the battery is connected. The charge current loop regulates the battery charge current to the programmed value, and prevents the charge current from exceeding that value. Through the use of dynamic power management (DPM), the input current loop regulates the battery charge current to the programmed value, and prevents the input current from exceeding that value. The three regulation loops operate independently, yet only require a single loop compensation network.

The system power selector function selects the appropriate power source for the system load. If the adapter is detected, then the adapter is connected to the system load. When the adapter is removed, the battery is selected to power the system load. A battery learn cycle is performed when the adapter is present by setting the CONTROL(0x12) register into Learn Mode via SMBus by the embedded host. This disconnects the adapter from the system; and instead, connect the battery to the system. This is typically done for Ni-based batteries.

SMBus Interface

The bq24721 uses all the SMBus communications protocol, except for packet error correction (PEC). The charger IC address is (0x12), although it is not 100% SBS compliant. In most applications, the extra functionality provided by the differing SBS-Like interface enhances the control of the charger application, while simplifying the interface block, using only the pertinent functions. Five 16-bit registers are used to interface between the embedded host and the charge control IC. The Charging Voltage (0x15) register is used to set the battery regulation voltage. The Charging Current (0x14) register is used to set the battery charge regulation current. The Input Current (0x3F) register is used to set the input regulation current. The Charger Mode (0x12) control register is used to set the charger operating modes. Finally, the Charger Status (0x13) register is used to monitor the operating status of the charger.

BLOCK DESCRIPTION (continued)

ADDRESS	REGISTER	DESCRIPTION
0x15	Charging voltage	Used to set the battery regulation voltage.
0x14	Charging current	Used to set the battery charge regulation current.
0x3F	Input current	Used to set the input regulation current.
0x12	Charger mode	Used to set the charger operating modes.
0x13	Charger status	Used to monitor the operating status of the charger.

The SMBus communications requires only two pins besides the analog ground pin—through the SDA (data) and SCL (clock) pins. The open-drain SCL and SDA pins require pull-up resistors on the board pulling up to the host digital output voltage rail. The pins can be pulled up to any rail between 3 V to 5 V.

An alarm is sent to the host through the $\overline{\text{ALARM}}$ open drain pin. This is used to trigger an interrupt request (IRQ). A low on the $\overline{\text{ALARM}}$ pin indicates there was a change on the Charger Status (0x13) register. The $\overline{\text{ALARM}}$ pin stays low until the host reads the Charger Status (0x13) register, then the $\overline{\text{ALARM}}$ pin clears and returns to the HI state. The open-drain $\overline{\text{ALARM}}$ pin requires a pull-up resistor that pulls up to the host digital input voltage rail. The pin can be pulled up to any rail between 3 V to 5 V. The charge controller continues to operate whether the host chooses to read or not to read the Charger Status (0x13) register. There is no communications watchdog timer, so there is no need to continuously poll the Charger Status (0x13) register or have to continuously reprogram any of the other registers.

Setting Charge Voltage (VBAT DAC register)

The charge voltage can be programmed by setting Charging Voltage(0x15) register. The SBS specification asks for 16 bits to set the regulation voltage with a 1-mV LSB—giving a maximum possible voltage of 65.535 V. The bq24721 uses bits 1 through 14 only, and maps them into the closest value of an internal 7-bit DAC on a per cell basis using a 6.25-mV per cell LSB for three ranges: 9-V precharge voltage; 3 cells Li+ battery pack range; or 4 cells Li+ battery pack range. The 3 cell portion has an LSB of 18.75 mV and a range from 12 V-14.4 V; while the 4 cell portion has an LSB of 25 mV and a range from 16 V-19.2 V. Intermediate programmed voltages between the internal 7-bit DAC values are truncated to the lower value to avoid an overvoltage on the battery. Programmed voltages above 19.2 V are automatically set to the maximum 19.2-V limit. The charger is disabled for programmed voltages below 12 V (except for 9 V), and for programmed voltages between 14.4 V – 16 V. This triggers a voltage-out-of-range condition and the VOR bit of the Charger Status (0x13) register is set, and an alarm ($\overline{\text{ALARM}}$ pin pulled low) is sent to the host. The default power-up-reset voltage value is 0 V, charger disabled.

Setting Charge Current (IBAT DAC register)

The charge current can be programmed using the Charging Current (0x14) register. The SBS specification asks for 16 bits to set the charge current with a 1-mA LSB—giving a maximum possible current of 65.535 A using a 10-mΩ sense resistor. The bq24721 uses bits 7 – 14 only to limit the range within a practical operating range. The current range is 0 mA to 16.384 A with an LSB of 128 mA using a 10-mΩ sense resistor. The charger is disabled when the programmed input current is 0 A. The default power-up-reset current value is 0 A, charger disabled. Other sense resistors can be used to set the charge current—the user needs to transform the DAC current table values to the new current values by dividing the current by 10 mΩ, then multiplying by the new sense resistor value used.

Setting Input (DPM) Current (IDPM DAC register)

The input current can be similarly programmed using the Input Current (0x3F) register. The SBS specification asks for 16 bits to set the input current with a 1-mA LSB—giving a maximum possible current of 65.535 A using a 10-mΩ sense resistor. The bq24721 uses bits 7 – 14 only to limit the range within a practical operating range. The current range is 0 mA to 16.384 A with an LSB of 128 mA using a 10-mΩ sense resistor. The charger is disabled when the programmed input current is 0 A. The default power-up-reset current value is 0 A, charger disabled. Other sense resistors can be used to set the input current—the user needs to transform the DAC current table values to the new current values by dividing the current by 10 mΩ, then multiplying by the new sense resistor value used.

Power Up

When the adapter is not detected, the REGN output voltage is 4.6 V and the VREF5 LDO regulator is off, to lower the power consumption from the battery. The VREF5 LDO is pulled-down to AGND when the adapter is not detected. The REGN LDO regulator begins to regulate at 4.6 V when the input VCC voltage is greater than 6 V. The REGN output voltage is then 6 V when the adapter is detected, and the VCC is greater than 7 V. If adapter is detected, but VCC is less than 7 V, then the REGN is in dropout, and REGN output voltage depends on the VCC voltage and REGN load current. The VREF5 LDO is allowed to turn-on and regulate to 5 V, 5 ms after REGN is 6 V and the adapter is detected. There is a 500-ms delay from the time the adapter is detected, until the ACFET from the system power selector is allowed to turn-on, and until the charger is allowed to turn-on. The battery continues to be connected to the system during this 500-ms delay.

Adapter Detect

The adapter detect threshold is programmed by an external voltage divider resistor from the adapter to the ACDET pin. The internal ACDET comparator has a 1.2-V rising-edge threshold and a 15-mV falling-edge hysteresis. The adapter detect value is typically programmed to a value greater than the maximum battery voltage, and lower than the minimum allowed adapter voltage. The ACDETECT divider is placed before the BYPASS FET in order to sense the true adapter input voltage whether the BYPASS is on or off.

The VREF5 LDO output is also used to indicate when the adapter is detected, for both the bq24721 and the bq24721, since the VREF5 LDO only comes up when the adapter is detected.

System Power Selector

The bq24721 can automatically switch between adapter power or battery power to the system load. The battery is connected to the system when there is no adapter detected. The adapter is connected to the system when the adapter is detected. An automatic break-before-make logic prevents shoot-through currents when the selector switches.

When no adapter is detected the ACDRV pin is pulled to the PVCC pin to keep the external ACFET p-channel power MOSFET off, disconnecting the adapter from system. The break-before-make logic waits until the ACFET is off and the System to battery voltage comparator indicates the system voltage is within 250 mV of the Battery (SYS voltage falling-edge, with a 50-mV hysteresis SYS voltage rising-edge). This prevents shoot-through currents or large discharge currents from going into the battery. The BATDRV pin is then set to the SYS pin voltage minus 6 V by an internal regulator in order to turn on the external BATFET p-channel power MOSFET, connecting the battery pack to the system.

When adapter is detected there is a 500-ms delay; then, the BATDRV is set to the SYS pin voltage to turn off the external BATFET p-channel power MOSFET, in order to disconnect the battery. The break-before-make logic waits until the BATFET is off to prevent shoot-through currents. The ACDRV pin is then set to the PVCC pin voltage minus 6 V by an internal regulator in order to turn on the external ACFET p-channel power MOSFET, connecting the adapter to the system.

The host can override the adapter to system connection when adapter is present, by setting the charger into Learn Mode. The host can then induce a learn cycle in which the battery is allowed to discharge. A learn cycle is used to recalibrate the fuel gauge for Ni-based batteries, or for clearing the memory effect of a Ni-cd battery. After discharging the battery, Learn Mode can be disabled allowing the adapter to be reconnected to the system, then resuming a normal charge cycle.

Whenever the battery is connected to the system (whether in learn cycle with adapter present, or no adapter present), there is a Low Battery comparator that monitors the battery voltage, and alerts the host and charge controller that the battery has been depleted. The BAT_DEP threshold can be programmed through the Charger Mode control (0x12) register through bits b9-b11. The three bits can program the threshold between 2.2-V per cell to 2.9-V per cell, in 100-mV increments. The number of cells is determined by the programmed battery regulation voltage (0x15) register. If the battery voltage falls below the BAT_DEP threshold, then the battery is disconnected from the system and the adapter is connected to the system. The Battery Voltage Low bit (b11) is set in the Charger Status (0x13) register, and the $\overline{\text{ALARM}}$ pin is pulled low to alert the host. There is a 1 second deglitch time to prevent false triggering.

The Charger Status (0x13) register bits b6 and b7 also always indicate whether the battery is connected to the system (b6), or the adapter is connected to the system (b7). An alarm is triggered whenever these states change.

Asymmetrical gate drives (100 Ω turn-off; 10 kΩ turn-on) for the ACDRV and BATDRV drivers provide fast turn-off and slow turn-on of the ACFET and BATFET to help the break-before-make logic and to allow a soft-start at turn-on of either FET. The soft-start time is further increased by putting a capacitor from gate to source of the p-channel power MOSFETs.

Input Overcurrent Protection (ACOC)

For solutions using the selector functions, an input overcurrent protection function (ACOC) is provided which disconnects the ACFET by turning off the ACDRV pin, whenever the sensed input current exceeds the programmed ACOC threshold. The ACOC threshold is programmed through the SMBus Charge Mode (0x12) control register, bits b6, b7, b8. The ACOC function is automatically disabled upon power-on-reset. The host needs to enable it by setting the ACOC bit (b6) HI. The ACOC threshold is set by the SET_ACOC bits (b7, b8), to thresholds of 130%, 150%, 170%, or 190% of the input current (DPM) regulation limit threshold from the Input Current (0x3F) register.

The ACFET turns off when the sensed current exceeds the threshold after a 200-µs deglitch time. The ACFET automatically turns on after 2 ms, to limit the on-time duty cycle, and limit the power dissipation on the ACFET. Care must be taken to ensure the system load power does not exceed the power-up allowable power when the ACOC function is used.

The function is not intended for system short-circuits, as usually the adapter self protects. Instead, the function is intended for long-term overcurrent protection of the selector power devices, and to limit start-up peak current.

Bypass FET

The BYPASS pin is used to control an input FET that is off to prevent reverse discharge from the battery to the adapter, and is on during input current draw to the system or battery, to minimize the power dissipation, as compared to using a Schottky diode. If no adapter is detected, the BYPASS FET is off, by setting the BYPASS pin to the PVCC pin. When the adapter is detected there is a 500-ms delay, then an ACP-to-BAT voltage comparator is used to control the BYPASS pin. The BYPASS driver is set to the PVCC pin voltage when the adapter voltage (ACP pin) is not more than 250 mV (ACP voltage falling-edge) above the battery voltage (BAT pin), in order to turn off the external BYPASS p-channel power MOSFET. There is a 50 mV (ACP voltage rising-edge) hysteresis, to protect from noise and prevent chatter. When adapter is detected and the ACP pin voltage is greater than 300 mV above the BAT pin voltage, the BYPASS pin voltage is set to PVCC pin voltage minus 6 V, in order to turn on the external BYPASS p-channel power MOSFET.

The ACP-to-BAT comparator also prevents the battery voltage from holding-up the ACDET sensed value and falsely detecting ACDET when the adapter is removed, this prevents the system power selector from *getting stuck* in an *adapter always detected* state. When ACP gets near to BAT, the external BYPASS p-channel power MOSFET is turned off. This isolates the ACDET network from the battery, and allows the adapter input node to discharge to PGND.

The BYPASS driver has a symmetrical gate drive of 1 kΩ turn-on and turn-off and does not need to be slowed down.

Enabling Charge

Charge is only enabled 500 ms after adapter is detected. To initiate charge the $\overline{\text{CHGEN}}$ pin must be low, and the Charger Mode (0x12) register END CHARGE bit (b0) must be set LO. The power-on-reset default for the END CHARGE bit is HI, disabling charge.

The Charger Status (0x13) register NOT READY TO CHARGE bit (b0) indicates whether the charger is ready to charge. A HI indicates the charger is not ready to charge, while a LO indicates the charger is ready to charge. The NOT READY TO CHARGE bit (b0) must be LO in order for the charger to be enabled. The conditions that make the charger not ready to charge are: adapter not detected, 500-ms delay after adapter detected not over, REGN voltage not up, or VREF5 voltage not up.

The Charger Status (0x13) register CHARGER NOT ON bit (b1) indicates whether the charger is not on (HI), or the charger is on (LO). For charger to be on, the $\overline{\text{CHGEN}}$ pin must be low, the Charger Mode (0x13) register END CHARGE bit (b0) must be LO, the, IC junction temperature must be below the TSHUT threshold, overcurrent detected, or Thermistor Sense (TS) indicates battery pack is out of programmed permissible charge temperature range (bq24721 only).

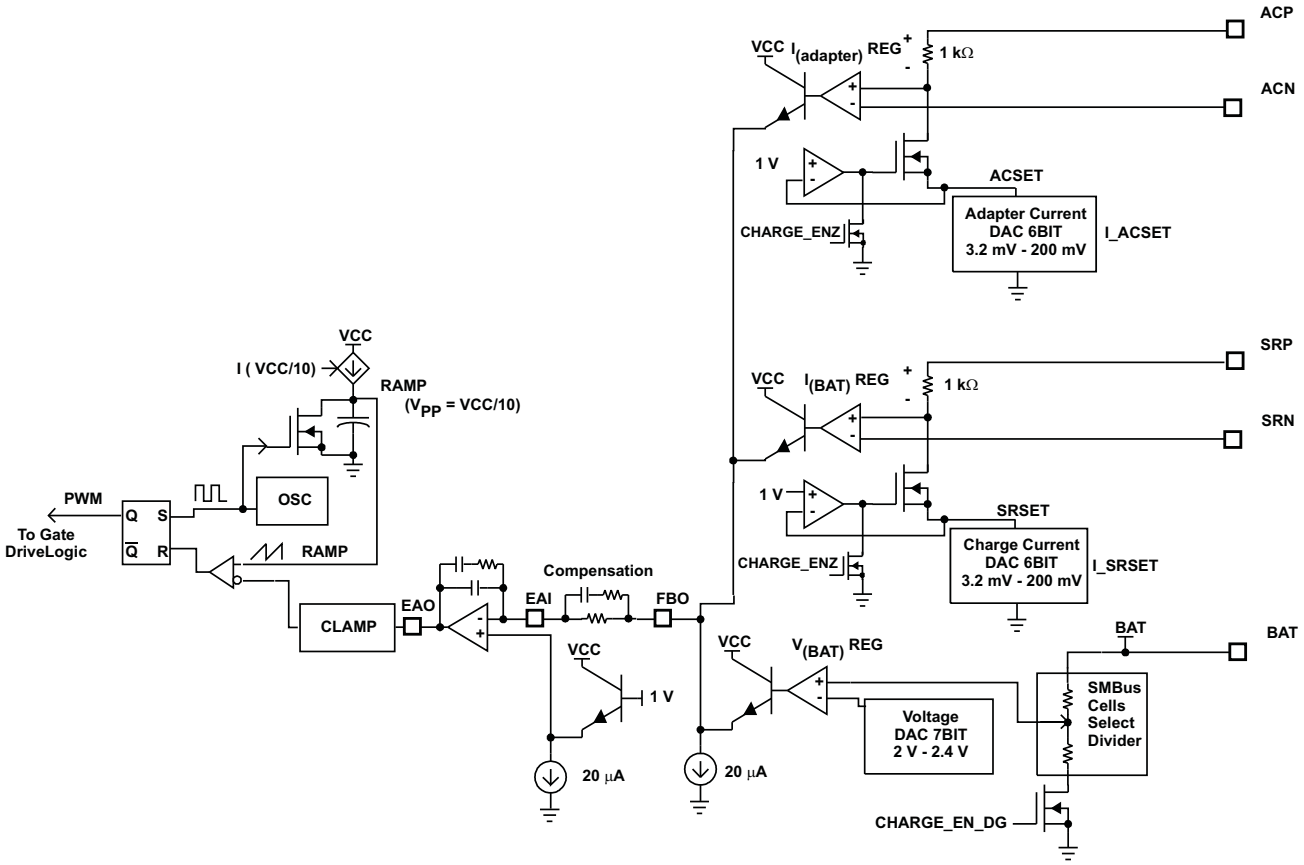


Figure 57. PWM Control Logic

Converter Operation

The synchronous buck PWM converter uses a fixed frequency voltage mode with feed-forward control scheme. A type III compensation network allows using ceramic output capacitors. The compensation input stage is connected between the feedback output (FBO) pin and the error amplifier input (EAI) pin. The feedback compensation stage is connected between the error amplifier input (EAI) pin and error amplifier output (EAO) pin.

An internal saw-tooth ramp is compared to the EAO pin error control signal to vary the duty-cycle of the converter. The ramp height is one-tenth of the input adapter voltage making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 300 mV in order to allow zero percent duty-cycle, when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.98% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4.5 V for more than 3 cycles, then the high-set n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the voltage is detected to fall low again due to leakage current discharging the BTST capacitor below the 4.5 V, and the reset pulse is reissued.

The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. The switching frequency can be changed from 300 kHz to 500 kHz by the Charger Mode (0x12) register PWM FS bit (b5) – a HI is 500 kHz, a LO is 300 kHz. The switching frequency is 300 kHs by default after power-on-reset. Typical chargers use 300 kHz, but 500 kHz allows a smaller inductance value

The charge current sense resistor should be placed with at least half or more of the total output capacitance placed before the sense resistor contacting both sense resistor and the output inductor; and the other half or remaining capacitance placed after the sense resistor. The output capacitance should be divided and placed onto both sides of the charge current sense resistor. A ratio of 50:50 percent gives the best performance; but the node in which the output inductor and sense resistor connect should have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better sense accuracy. The type III compensation is already providing phase boost near the cross-over frequency, giving sufficient phase margin.

ISYNSET

The ISYNSET pin is used to program the charge current threshold at which the charger changes from nonsynchronous operation into synchronous operation. This prevents negative inductor current. Negative inductor current may cause a *boost* effect in which the input voltage increases as power is transferred from the battery to the input capacitors—this can lead to an overvoltage on the PVCC node and potentially cause some damage to the system.

This programmable value allows setting the current threshold for any inductor current ripple, and avoiding negative inductor current. The SYNP and SYNN pins are used to sense across the charge current sense resistor.

To program the threshold, a resistor is connected from the ISYNSET pin to AGND. The minimum synchronous threshold should be set from the inductor current ripple to the full ripple current, where the inductor current ripple is given by.

$$\frac{I_{(RIPPLE_MAX)}}{2} \le I_{(SYN)} \le I_{(RIPPLE_MAX)} \quad (1)$$

where

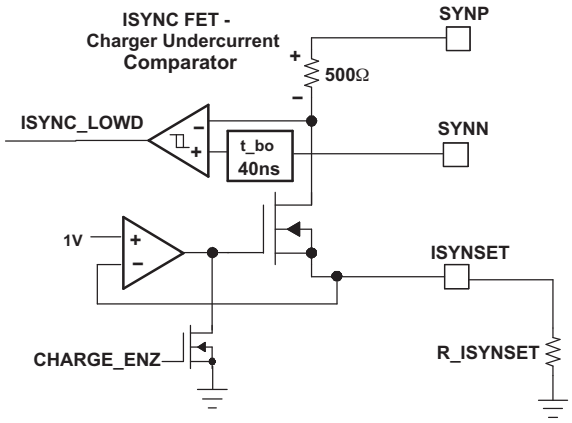
$$R_{(RIPPLE_MAX)} = \frac{\left(V_{(IN_MAX)} - V_{(BAT_MIN)}\right) \times \left(\frac{V_{(BAT_MIN)}}{V_{(IN_MAX)}}\right) \times \left(\frac{1}{f_S}\right)}{L_{(MIN)}} \quad (2)$$

$V_{(IN_MAX)}$ is the maximum adapter voltage, $V_{(BAT_MIN)}$ is the minimum battery voltage, f_S is the switching frequency, and LMIN is the minimum output inductor value.

The ISYNSET pin is internally regulated to 1 V. When the $R_{(SYNSET)}$ resistor is connected to AGND, it sets an ISYNSET current equal to 1 V/$R_{(SYNSET)}$. The ISYNSET current internally flows through a 500 Ω creating a voltage at which the voltage across $R_{(SENSE)}$ is compared. The ISYN charge current threshold is the voltage divided by the $R_{(SENSE)}$ sense resistor value. The $R_{(SYNSET)}$ resistor value is calculated by:

$$R_{(SYNSET)} = \frac{1\ V \times 500\ \Omega}{I_{(SYN)} \times R_{(SENSE)}} \quad (3)$$

where ISYN is the charge current threshold at which the converter changes to synchronous operation.



NOTE: Patent Pending

Figure 58. Synchronous to Nonsynchronous threshold, ISYNSET, Block – Charger Undercurrent (prevents negative inductor current)

Synchronous versus Nonsynchronous Operation

The charger operates in nonsynchronous mode when the sensed charge current is below the ISYNSET programmed value. When above the ISYNSET programmed value, the charger operates in synchronous mode.

During synchronous mode, the low-side n-channel power MOSFET is on, when the high-side n-channel power MOSFET is off. The internal gate drive logic ensures there is break-before-make switching to prevent shoot-through currents. During the dead-time where both FETs are off, the back-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn-on keeps the power dissipation low, and allows safely charging at high currents. During Synchronous mode the inductor current is always flowing and operates in Continuous Conduction Mode (CCM) creating a fixed two-pole system. During nonsynchronous operation: after the high-side n-channel power MOSFET turns off, and after the break-before-make dead-time, the low-side n-channel power MOSFET turns on for around 80 ns, then the low-side power MOSFET turns off and stays off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The 80 ns low-side MOSFET on-time is done to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The 80 ns low-side pulse pulls the PH node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring. The inductor current is blocked by the off low-side MOSFET, and the inductor current becomes discontinuous. This mode is called Discontinuous Conduction Mode (DCM).

During the DCM mode the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage.

At very low currents during nonsynchronous operation, there may be a small amount of negative inductor current during the 80 ns *recharge pulse*. The charge should be low enough to be absorbed by the input capacitance.

Whenever the converter goes into zero percent duty-cycle, the high-side MOSFET does not turn-on, and the low-side MOSFET does not turn-on (no 80 ns recharge pulse), so there is no discharge from the battery.

Battery Voltage Regulation Loop

The BAT pin is used to sense the battery voltage and should be connected as close to the battery as possible, or directly to the output capacitor. A 0.1-µF ceramic capacitor from BAT to AGND is recommended—added as close to the BAT pin as possible to decouple high frequency noise.

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bq24721 monitors the battery-pack voltage between the BAT and VSS pins. The regulation voltage is programmed through the SBS-like SMBus interface.

The voltage regulation DAC register input is decoded into an internal 7-bit DAC that programs the voltage on a per-cell basis, then is multiplied by the number of cells. There are a total of 128 voltage steps with a 6.25 mV step, giving a per cell range of [4 V – (4.8 V–6.25 mV)]. There are 128 steps in the 3-cell voltage range of [12 V – (14.4 V–18.75 mV)]. There are 128 steps in the 4-cell voltage range of [16 V – (19.2 V–25 mV)].

Valid voltage values are 9 V, 12 V–14.381 V, and 16 V–19.175 V. The internal voltage DAC allows programming to 9 V which is used for waking-up or closing the battery pack. A 9 V programmed voltage is interpreted as a 2-cell voltage by the BATDEP and BATSHORT thresholds. Step size for 3-cell battery programming voltage is 18.75 mV. The Charger interprets a 3-cell battery for any voltage between 12 V–14.4 V. Step size for 4-cell battery programming voltage is 25 mV. The charger interprets a 4-cell battery for any voltage programmed between 16 V–19.2 V.

Invalid DAC voltages are indicated by the VOR (voltage out of range) bit of the status register. Voltages below 12 V (except for 9 V) are out of range and keep the converter disabled. Voltages between 14.4 V–16 V (including 14.4 V, but not including 16 V) are out of range and keep the converter disabled. Voltages above 19.2 V (including 19.2 V) are out of range and allow the converter to charge, but the voltage is always set to the maximum allowable voltage of 19.175 V = (19.2 V–25 mV).

Battery Charge Current Regulation Loop

The battery charge current DAC is set for a 10-mΩ sense resistor; however, resistors of other values can also be used. The larger the sense resistance, the larger the sensed voltage, and the higher the regulation accuracy, but at the expense of higher conduction losses. The SRP and SRN pins are used to sense across the sense resistor.

The battery charge current, $I_{O(CHARGE)}$, is established by setting the external sense resistor, $R_{(SNS_CHG)}$, and the SMBus charge current DAC (0×14). In order to set the current, first $R_{(SNS_CHG)}$ should be chosen based on the regulation threshold $V_{(IREG_CHG)}$, across this resistor. The listed SBS current corresponds to a 10-mΩ sense resistor.

$$R_{(SNS_CHG)} = V_{(IREG_CHG)} / I_{O(CHARGE)}$$

Input Current Regulation Loop (DPM)

The ACP and ACN pins are used to sense across the sense resistor. The input current DAC is set for a 10-mΩ sense resistor; however, resistors of other values can also be used. The larger the sense resistance, the larger the sensed voltage, and the higher the regulation accuracy, but at the expense of higher conduction losses.

The input current, $I_{I(DPM)}$, is established by setting the external sense resistor, $R_{(SNS_DPM)}$, and the SMBus input current DAC ($0 \times 3F$). In order to set the current, first $R_{(SNS_DPM)}$ is chosen based on the regulation threshold $V_{(IREG_DPM)}$, across this resistor. The listed SBS current corresponds to a 10-mΩ sense resistor.

$$R_{(SNS_DPM)} = V_{(IREG_DPM)} / I_{O(CHARGE)}$$

Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger is enabled, in order to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into eight evenly divided steps up to the programmed charge current of register (0x14). Duration of each step is around 1 ms, for a typical rise time of 8 ms. No external components are needed for this function.

The bq24721 current regulation loop reference steps-up whenever charge is enabled, and when returning from fault/suspend mode into charge where the current regulator is turned on. The loop should take control within a few hundred micro-seconds with very little overshoot due to the LC output filter and the high compensation loop bandwidth with 300 kHz or 500 kHz operating frequency; therefore, the reference could ramp up from precharge to fast-charge within 50 µs to 500 ms. Going into fault/suspend mode, short circuit ($V_{(BAT)} < V_{(UVT)}$), Sleepmode ($V_{(ACP)} < V_{(BAT)}$), or UVLO (VCC < 3.7 V) initiates an immediate shut-off of the high-side PWM FET by setting its gate to $V_{(PH)}$. The output inductor and battery load determines the ramp-down rate as it *freewheels* through the Schottky diode.

High Accuracy Current Sense Amplifiers (CSA), IOUT pin, for Input Current and Charge Current

Industry standard, high accuracy current sense amplifiers (CSA) can be used to monitor the input current or the charge current by the host or some discrete logic through the analog voltage output of the IOUT pin. The current sense amplifier from the input current and the current sense amplifier of the charge current (voltage across SRP-SRN pins) amplifies the input sensed voltage by 20x, through the Iout pin. The IOUT output is selectable between the input current or the charge current, through a multiplexor that is controlled by the Charge Mode (0x12) control register, IOUT Select bit (b3). The default setting is LO selecting the input current CSA. Programming a HI selects the charger current CSA.

The IOUT output is a voltage source 20 times the input differential voltage. If the user wants to lower the voltage, use a sense resistor from IOUT to AGND, and still achieve accuracy overtemperature as the resistors match their thermal coefficients.

A 0.1-µF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay.

Charger Overcurrent Protection

The charger has a secondary overcurrent protection function that monitors the charge current, and prevents it from exceeding 200% of the programmed charge current. The high-side gate drive turns off and automatically resume when the current falls below the overcurrent threshold

Current Regulation Down to Zero Battery Voltage

The bq24721 charger regulates charge current and input current down to zero volts on the battery BAT voltage. If there is a drop below 2 V, then the converter immediately turns off both high-side and low-side FETs to stop current flow, then resumes regulating the current. This ensures there is no overcurrent surge that could cause damage to the battery, charger, or system.

Thermal Shutdown Protection

The QFN package has low thermal impedance which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the $T_{(SHUT)}$ threshold of 145°C. The charger stays off until the junction temperature falls below 130°C.

Battery Short-Circuit or Low Condition

The number of cells determines the value for the BATDEP threshold and for the BATSHORT threshold, as these values are programmed on a per-cell basis. The programmed regulation voltage determines the number of cells. The battery depleted (BATDEP) threshold is programmed by the control register bits b9-b11. The three bit dac sets the voltage between 2.2 V to 2.9 V per cell at 100 mV increments. The BATSHORT threshold is 1.7 V/Cell falling entering a shorted condition, and 1.9 V/Cell rising leaving shorted condition, and entering normal condition. BATSHORT has a 1 second deglitch on both edge directions to protect from transient conditions, and to allow closing deeply discharge battery packs.

The PWM duty-cycle immediately resets to zero percent when the battery voltage is sensed to drop below 2 V, then the regulation loop allows the duty-cycle to settle in the current regulation value, C. After a 1 second deglitch, the converter regulates battery current to C/8 when the battery voltage falls below 1.7 V/cell. The converter regulates back at C after a 1 second deglitch from the time the battery voltage rises above 1.9 V/cell.

Charge Termination for Li-Ion or Li-Polymer

The primary termination method for Li-Ion and Li-Polymer is minimum current. Secondary temperature termination methods is also provided for additional safety. The host controls the charge initiation and the termination. A battery pack gas gauge assists the hosts on setting the voltages and determining when to terminate based on the battery pack state of charge.

Temperature Qualification (TS pin)

The bq24721 continuously monitors battery temperature by measuring the voltage between the TS pin and AGND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The bq24721 compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the $V_{(LTF)}$ to $V_{(HTF)}$ thresholds. If battery temperature is outside of this range, the bq24721 suspends charge and waits until the battery temperature is within the $V_{(LTF)}$ to $V_{(HTF)}$ range. During the charge cycle (both precharge and fast charge) the battery temperature must be within the $V_{(LTF)}$ to $V_{(TCO)}$ thresholds. If battery temperature is outside of this range, the bq24721 suspends charge and waits until the battery temperature is within the $V_{(LTF)}$ to $V_{(HTF)}$ range. The bq24721 suspends charge by turning off the PWM charge FETs. Figure 59 summarizes this operation.

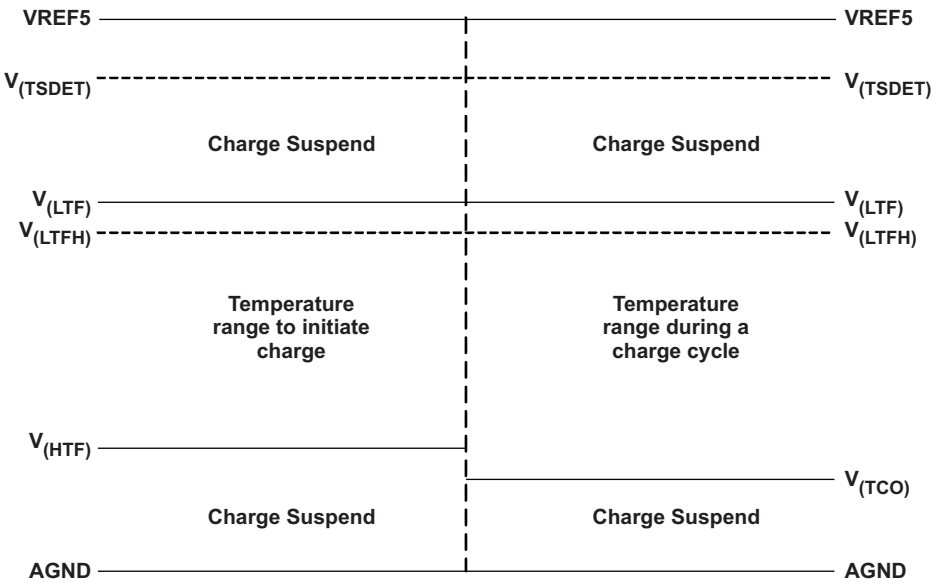


Figure 59.

SBS-Like SMBus

SBS-Like interface is not 100% SBS compliant, as control and status registers were changed to simplify and enhance the charger control device. Address 0x12 is used, but the charger should not to be used on systems requiring 100% SBS compliance. Effort was taken to use the same commands when possible. Comparison included on SBS-like vs SBS Spec.

- SBS-Like SMBus
  - SBS 1.1 protocol, slave operation only
  - No CRC
  - Address: 12 (Note SBS-Like is not 100% SBS compliant and has simplified enhancements
- Smart charger commands implemented
  - ChargingCurrent (), with modifications on data byte contents, *SBS-Like* SMBus
  - ChargingVoltage (), with modifications on data byte contents, *SBS-Like* SMBus
  - ChargerStatus (), with modifications on status bits
- Smart charger commands not implemented
  - ChargerSpecInfo (),
  - AlarmWarning ()

SBS-Like SMBus: Commands Implemented: Charge Current DAC Register

Charging Current, (0x14), Write/Read(1)

Table 1.

BIT	SBS SPEC	bq24721 SBS-Like	NOTES
0 (LSB)	1 mA	NA	Charge current limit setting 16384 mA max (162.56 mV max)
1	2 mA	NA	
2	4 mA	NA	
3	8 mA	NA	
4	16 mA	NA	
5	32 mA	NA	
6	64 mA	NA	
7	128 mA	128 mA (1.28 mV)	
8	256 mA	256 mA (2.56 mV)	
9	512 mA	512 mA (5.12 mV)	
10	1024 mA	1024 mA (10.24 mV)	
11	2048 mA	2048 mA (20.48 mV)	
12	4096 mA	4096 mA (40.96 mV)	
13	8192 mA	8192 mA (81.92 mV)	
14	16384 mA	NA	
15 (MSB)	32768 mA	NA	

(1) Note: Shunt drop voltage shown at LO/HI bit state;
DAC current value is based on using 10-mΩ sense resistor.
Max charge current with 10-mΩ sense resistor is 16.256 A.

Bit 13 allows using larger sense resistors for increasing accuracy in low charge current applications.

- Valid charge currents are 0 A–16.256 A using a 10-mΩ sense resistor. Minimum step is 128 mA.
- Programmed charge currents above max 16.256 A → Charger is enabled and the current regulation value is set to the maximum 16.256 A.
- Programmed charge current = 0 A → Charger is disabled.

SBS-Like SMBus: Commands Implemented: Input Current DAC Register

Input Current, (0x3F), Write/Read (1)

BIT	SBS SPEC	bq24721 SBS-Like	NOTES
0 (LSB)	1 mA	NA	Input DPM current limit setting 16384 mA max (162.56 mV max)
1	2 mA	NA	
2	4 mA	NA	
3	8 mA	NA	
4	16 mA	NA	
5	32 mA	NA	
6	64 mA	NA	
7	128 mA	128 mA (1.28 mV)	
8	256 mA	256 mA (2.56 mV)	
9	512 mA	512 mA (5.12 mV)	
10	1024 mA	1024 mA (10.24 mV)	
11	2048 mA	2048 mA (20.48 mV)	
12	4096 mA	4096 mA (40.96 mV)	
13	8192 mA	8192 mA (81.92 mV)	
14	16384 mA	NA	
15 (MSB)	32768 mA	NA	

(1) Note: Shunt drop voltage shown at LO/HI bit state;
DAC current value is based on using 10-mΩ sense resistor.
Max input current with 10-mΩ sense resistor is 16.256 A.

Bit 13 allows using larger sense resistors for increasing accuracy in low input current applications.

- Valid input currents are 0 A–16.256 A using a 10-mΩ sense resistor. Minimum step is 128 mA.
- Programmed input currents above max 16.256 A → Charger is enabled and the current regulation value is set to the maximum 16.256 A.
- Programmed input current = 0 A → Charger is disabled.

SBS-Like SMBus: SBS Translator Voltage DAC Commands Implemented

Charging Voltage, (0x15), Write/Read

BIT	SBS SPEC	bq24721 SBS-Like CHARGE VOLTAGE LOOK-UP TABLE	NOTES
0 (LSB)	1 mV	NA	Not used
1	2 mV	0 / 2 mV	See Notes below for valid voltage range and minimum step size (resolution(1))
2	4 mV	0 / 4 mV	
3	8 mV	0 / 8 mV	
4	16 mV	0 / 16 mV	
5	32 mV	0 / 32 mV	
6	64 mV	0 / 64 mV	
7	128 mV	0 / 128 mV	
8	256 mV	0 / 256 mV	
9	512 mV	0 / 512 mV	
10	1024 mV	0 / 1024 mV	
11	2048 mV	0 / 2048 mV	
12	4096 mV	0 / 4096 mV	
13	8192 mV	0 / 8192 mV	
14	16384 mV	0 / 16384 mV	
15 (MSB)	32768 mV	NA	Not used

(1) Note: Battery voltage range: 4 V–4.8 V per cell
3 Cell range: 12 V to (12 V–14.4 V); step size = 18.75 mV
4 Cell range: 16 V to (16 V –19.2 V) ; step size = 25 mV
a. Valid voltages are 9 V, 12 V–14.4 V, and 16 V–19.2 V. Intermediate programmed voltages between Internal DAC values are truncated to the lower value to avoid overvoltage on battery.
b. Programmed Voltages above max 19.2 V → Charger is enabled and the voltage regulation value is set to the maximum 19.2 V.
c. Programmed voltages below 12 V (except 9 V), and between 14.4 V–16 V → Charger is disabled, VOR bit is triggered, and an alarm is sent to the host.
d. Programmed 9 V (9000 mV = 2328 Hex) → Charger regulates to 9-V output for battery wakeup.

SBS-Like SMBus: IC Internal Voltage DAC for Reference Only

Internal decoder translates the SBS voltage register value into the internal closest value. Values are truncated to the lower valid setting.

Charging Voltage, IC Internal Only

BIT	bq24721 SBS-Like CHARGE VOLTAGE INTERNAL DECODER DAC		NOTES
0 (LSB)	0/18.75 mV	0/25 mV	Offset that can be added to *dc* level See the following notes for valid voltage range and minimum step size (resolution) (1)
1	0 / 37.5 mV	0 / 50 mV	
2	0 / 75 mV	0 / 100 mV	
3	0 / 150 mV	0 / 200 mV	
4	0 / 300 mV	0 / 400 mV	
5	0 / 600 mV	0 / 800 mV	
6 (MSB)	0 / 1.2 V	0 / 1.6 V	
	LO – 12 V	HI – 16 V	3 Cell or 4 Cell *dc* level select

(1) Note: Battery voltage range: 4 V–4.8 V per cell
3 Cell range: 12 V to (12 V–14.4 V); step size = 18.75 mV
4 Cell range: 16 V to (16 V –19.2 V) ; step size = 25 mV
a. Valid voltages are 9 V, 12 V–14.4 V, and 16 V–19.2 V. Intermediate programmed voltages between Internal DAC values are truncated to the lower value to avoid overvoltage on battery.
b. Programmed Voltages above max 19.2 V → Charger is enabled and the voltage regulation value is set to the maximum 19.2 V.
c. Programmed voltages below 12 V (except 9 V), and between 14.4 V–16 V → Charger is disabled, VOR bit is triggered, and an alarm is sent to the host.
d. Programmed 9 V (9000 mV = 2328 Hex) → Charger regulates to 9 V output for battery wake-up.

Programmed Voltage Value Difference Between Li-Ion and NiMH Battery Pack Charging

- Li-Ion based battery packs require both current regulation and voltage regulation loops – where constant-current and constant voltage is needed to fully charge the battery pack.
- NiMH batteries require only a constant current for charging. Thereby, the voltage regulation loop is not needed. To accomplish this, set the regulation voltage at a value greater than the maximum battery pack voltage. This does not allow the voltage regulation loop to become active. The maximum value of 19.2 V is set for most NiMH battery packs.

SBS-Like SMBus: Commands Implemented: Control Register

Charger Mode, (0x12), Write-Only [Default POR and Reset Value in BOLD TYPE]

BIT	SBS SPEC	bq24721 SBS-Like	
0 (LSB)	INHIBIT CHARGE	END CHARGE (1)	
		1: Disable Charger	0: Enable Charger
		This affects STATUS register 0x13, bit 1.	
1	ENABLE POLLING	RESERVED: Not Used. Bit always resets to zero.	
2	POR_RESET	RESET: (Return to POR values) Charger disabled, DPM active, PWM at 300 kHz, V_O = 0, CHARGE CURR = 0, IDPM = 0	
		1: Reset	**0: No Reset**
3	RESET_TO_ZERO	IOUT Select: Current Sense Amplifier Output select	
		1: Charge current is the 20x amplifier output at IOUT pin	
		0: Adapter current is the 20x amplifier output at IOUT pin	
		The IOUT pin is multiplexed to either the charge current or the input current sense amplifiers. The Input current (ac) is the default upon power up.	
4	RESERVED	LEARN CYCLE	
		1: Connect Battery to system (learn cycle) even when adapter connected	
		0: Connect AC adapter to system (no learn) when adapter connected	
		This bit affects STATUS register 0x13, bits 6 and 7.	
5	RESERVED	PWM FS: Switching Frequency Select	
		1: PWM at 500 kHz	**0: PWM at 300 kHz**
6	RESERVED	ACOC – AC (adapter) Overcurrent	
		1: ACOC protection enabled	**0: ACOC protection disabled**
7	RESERVED	SET_ACOC <1:0>	
8	RESERVED	00: ACOC=DPM × 1.3	**01: ACOC=DPM × 1.5**
		10: ACOC=DPM × 1.7	11: ACOC=DPM × 1.9
		Bit 6 of this Control register 0×12 needs to be high for these bits to take effect.	
		ACOC threshold is a percentage of the DPM (input current) regulation threshold programmed by the DPM register 0×3F.	
9	RESERVED	SET_BAT_DEPL <2:0> Battery depleted threshold	
10	RESERVED	Value set per cell	
11	RESERVED	**000: [2.2V]**, 001:[2.3V], 010:[2.4V], 011:[2.5V] 100:[2.6V], 101:[2.7V], 110:[2.8V], 111:[2.9V] These bits affect STATUS register 0×13, bits 11, 6 and 7.	
12	RESERVED	RESERVED: Not Used. Bit always resets to zero.	
13–15(MSB)	RESERVED	RESERVED: Not Used. Bit always resets to zero.	

(1) END_CHARGE bit must be LO AND the $\overline{\text{CHRGEN}}$ pin must be LO to enable the charger. If the END_CHARGE bit is HI or the $\overline{\text{CHRGEN}}$ pin is HI, then the charger is disabled.

SBS-Like SMBus: Commands Implemented: Status Register

Charger Status, (0x13), Read-Only

All Status register bits are automatically updated by the IC whenever the system state changes, some bits have an 8 ms deglitch to prevent false alerts. Whenever a status bit changes, the $\overline{\text{ALARM}}$ open drain output pulls down to alert the host of a change in the status register. The $\overline{\text{ALARM}}$ stays low until the host performs a STATUS register (0×13) read, afterward, the $\overline{\text{ALARM}}$ clears and goes high impedance. An external pull-up resistor is needed at the $\overline{\text{ALARM}}$ pin.

BIT	SBS SPEC	bq24721 SBS-Like
0 (LSB)	CHARGE_INHIBITED	NOT READY TO CHARGE 1 = Charger is not ready to charge (IC comes up in this state) 0 = Charger is ready to charge (Note: Same logic polarity as SBS spec, but added Feature, Not part of SBS spec.) This bit indicates all the conditions are met to allow the charger to start charging. Precursers are Power-on-Reset is completed; adapter is detected, and REGN driver rail is ready.
1	MASTER MODE	CHARGER NOT ON 1 = Charger is Not On (IC comes up in this state) 0 = Charger is On (Note: same logic polarity and different bit, from SBS spec bit 0) Hi on this bit indicates that the charger is on . If Low, the charger is off. This bit allows the user to determine if there is a fault that disable the charger. Bits in this STATUS register 0x13 are used in conjunction with this bit to determine the source of charger turning off.
2	VOLTAGE_NOTREG	CHARGE VOLTAGE LOOP NOT ACTIVE 1 = Charge Voltage Loop Not Active (IC comes up in this state, and in this state when charger is not enabled) 0 = Charge Voltage Loop Active (Note: same logic polarity as SBS spec bit 2). A Lo on this bit indicates the battery voltage regulation loop is active and is influencing the charger regulation. There is an overlap as one loop transitions to another loop to allow for a soft transition knee. This overlap alerts that another loop is getting close to its limit and is influencing the output.
3	CURRENT_NOTREG	CHARGE CURRENT LOOP NOT ACTIVE 1 = Charge Current Loop Not Active (IC comes up in this state, and in this state when charger is not enabled) 0 = Charge Current Loop Active (Note: same logic polarity from SBS spec bit 3) A LO on this bit indicates the charge current regulation loop is active and is influencing the charger regulation. There is an overlap as one loop transitions to another loop to allow for a soft transition knee. This overlap alerts that another loop is getting close to its limit and is influencing the output.
4	LEVEL2	DPM INPUT CURRENT LOOP NOT ACTIVE 1 = DPM Input Current Loop Not Active (IC comes up in this state, and in this state when charger is not enabled) 0 = DPM Input Current Loop Active (Note: Added Feature, Not part of SBS spec. Same logic polarity from bits 2 and 3 of SBS spec) Dynamic Power Management (DPM) dynamically reduces the charge current when the system current increases enough to cause the total input current to reach the input power limit. This gives power delivery precedence to the system current over the charge current. A LO on this bit indicates the input current regulation loop is active and is influencing the charger regulation. There is an overlap as one loop transitions to another loop to allow for a soft transition knee. This overlap can alert that another loop is getting close to its limit and is influencing the output.
5	LEVEL3	CHARGE OVERCURRENT FAULT (Note: Added Feature, Not part of SBS spec.) HI indicates the charge current was higher than the charge overcurrent limit (SROC) which is 1.7 times the charge regulation setting. This is to protect from shorts or large load transients at the output. If SROC is detected, the high-side FET is immediately turned-off, and an alarm is sent out. The charger retres again, allowing the high-side FET to turn-on the next cycle. This fault current limit continues until the fault is removed.

BIT	SBS SPEC	bq24721 SBS-Like
6	CURRENT_OR	BATTERY CONNECTED TO SYSTEM (by selector BATDRV) (Note: Added Feature, Not part of SBS spec.) HI indicates the battery is connected to the system output. LO indicates battery is not connected. During this HI state, the BATDRV pin is pulled 6V below the SYS pin voltage to turn on the external PMOS BAT FET. When in LO state, the BATDRV pin voltage is pulled-up to the SYS pin voltage. Battery is connected to system when ac is not present, or when ac is present and LEARN CYCLE is set at the control register. FEATURE: If in learn cycle and the battery falls below the BATDEP threshold (programmed by the control register), then the IC automatically switches from battery power to ac adapter power. FEATURE: Also, in all cases if system (SYS) voltage is more than 150 mV above the battery (BAT) voltage then the BAT FET is kept off until SYS discharges to within 150 mV to prevent the system capacitors from discharging into the battery. This feature protects the battery from extended high surge currents.
7	VOLTAGE_OR	ADAPTER CONNECTED TO SYSTEM (by selector ACDRV) (Note: Added Feature, Not part of SBS spec.) HI indicates the adapter is connected to the system output. LO indicates adapter is not connected. During this HI state, the ACDRV pin is pulled 6 V below the PVCC pin voltage to turn on the external PMOS AC FET. When in LO state, the ACDRV pin voltage is pulled-up to the PVCC pin voltage. AC is connected to system when adapter is present (ACDET voltage is above threshold) and LEARN CYCLE is not set at the control register. FEATURE: If in learn cycle and the battery falls below the BATDEP threshold (programmed by the control register), then the IC automatically switches from battery power to ac adapter power. FEATURE: If there is an adapter overcurrent (ACOC) is detected, then the AC FET is turned off immediately to prevent a short-circuit condition or a surge current. This feature protects the battery from extended high surge currents.
8	THERMISTOR_OR	IC THERMAL SHUTDOWN FAULT (Note: Added Feature, Not part of SBS spec.) A HI indicates the IC temperature is too high, and had to turn-off the charger. LO indicates temperature is safe. FAULT DETECTION AND PROTECTION FEATURE: The IC monitors its own junction temperature. If the IC junction temperature exceeds 145°C, then the IC automatically shuts down the charger and an $\overline{\text{ALARM}}$ is triggered. SMBus communications continues to function. The charger remains off until the IC junction temperature falls below 130°C. The charger automatically restarts once the temperature falls below the hysteresis at 130°C.
9	THERMISTOR_COLD	[THERMISTOR COLD HI indicates the thermistor temperature is too cold to allow charging. The TS pin voltage threshold is higher than the TS cold voltage threshold when this bit is HI. A LO means the TS voltage is below the TS cold voltage threshold. Programmed by a voltage divider pulled up to the VREF5 pin. Note: VREF5 only comes up when ac is detected to conserve battery power, since no charging would be required.
10	THERMISTOR_HOT	THERMISTOR HOT (start) or (operating) HI indicates the thermistor temperature is too hot to allow charging. The TS pin voltage threshold is lower than the TS hot voltage threshold when this bit is HI. A LO means the TS voltage is above the TS hot voltage threshold. There is a different voltage threshold before starting charge than during charging (operating). Programmed by a voltage divider pulled up to the VREF5 pin. Note: VREF5 only comes up when AC is detected to conserve battery power, since no charging is required.

BIT	SBS SPEC	bq24721 SBS-Like
11	THERMISTOR_UR	BATTERY VOLTAGE LOW (battery depleted) (Note: Added Feature, Not part of SBS spec.) This bit goes HI when the sensed BAT voltage is below the Battery Depleted threshold programmed by the CONTROL register 0x12, bits 9, 10, and 11. The programmed voltage is per cell; therefore, multiply by the number of cells set by the programmed battery voltage regulation DAC, register 0x15. [3 cell for voltages between 12 V-14.4 V; and 4 cell for voltages between 16 V-19.2 V]. FEATURE: the BATDRV is turned off when the battery voltage falls below the BATDEP threshold, and the AC DRV is turned on if adapter is connected, and had previously been in LEARN Cycle (bit 4 of CONTROL register, 0x12).
12	ALARM_INHIBITED	VOR, VOLTAGE OUT OF RANGE (Note: moved function from bit7 of SBS spec) A HI indicates the voltage DAC value from register 0x15 is out of the valid DAC voltage range. The IC either disables the charge if below, or stays at the maximum possible programmed voltage (19.2 V) according to the following. Valid voltage DAC range and effect. • Valid voltages are 9 V, 12 V –14.4 V, and 16 V–19.2 V. Intermediate programmed voltages between Internal DAC values are truncated to the lower value to avoid overvoltage on battery. • Programmed Voltages above max 19.2 V → Charger is enabled and the voltage regulation value is set to the maximum 19.2 V. • Programmed voltages below 12 V (except 9 V), and between 14.4 V–16 V → Charger is disabled, VOR bit is triggered, and an alarm sent to host. • Programmed 9 V (9000 mV = 2328 Hex) → Charger regulates to 9-V output for battery wake-up.
13	POWER_FAIL	ADAPTER VOLTAGE BELOW BATTERY PACK VOLTAGE (Note: Added Feature, Not part of SBS spec.) A HI on this bit indicates the battery voltage is above the adapter voltage (BAT pin > ACP pin). FEATURE: If the input falls below 150 mV above the Battery voltage, the BYPASS FET immediately turns off to prevent reverse discharge of the battery into the adapter. There is an 8 ms deglitch and 100 mV to hysteresis before allowing the BYPASS FET to turn-on.
14	BATTERY PRESENT	BATTERY DETECTED (through thermistor pin) FEATURE: HI indicates a battery is detected through the TS pin. The TS pin voltage threshold is lower than the TS battery detect threshold when this bit is HI. A LO means the TS voltage is above the TS battery detect threshold. A resistor to ground inside the battery is used to distinguish a good battery from a bad battery as well. Programmed by a voltage divider pulled up to the VREF5 pin. Note: VREF5 only comes up when ac is detected to conserve battery power, since no charging is required. (Note: Added Feature. This is used for detecting proper battery connected by selecting the proper valid resistance. This is need to be *ORed* for dual battery pack chargers to make feature optimal. This feature also is used as a safety feature to stop charge immediately when the battery pack is not detected – this allows a faster response time by autonomously terminating charge when no battery is detected, as opposed to waiting until the host detects the battery is removed and then alerting the charger.
15 (MSB)	AC_PRESENT	AC ADAPTOR DETECTED This bit is HI when the adapter is detected (ACDET pin voltage is above the acdetect threshold of 2.4V). The voltage can be programmed by an external resistor divider from adapter input to ground. Charge is not allowed until the ACDET threshold is exceeded. VREF5 LDO output only turns on when the ACDET threshold is exceeded (adapter detected). REGN POR and SMBus communication begins soon after the ACDET threshold is above 1.2 V and the VCC is above 6.5 V.

ELECTRICAL CHARACTERISTICS

7 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, –20°C < T_J < 125°C, ref = AGND (unless otherwise noted).

PARAMETER		MIN	TYP	MAX	UNIT
SMBus TIMING CHARACTERISTICS					
t_R	SCLK/SDATA rise time			1	µs
t_F	SCLK/SDATA fall time			300	ns
$t_{W(H)}$	SCLK pulse width high	4		50	µs
$t_{W(L)}$	SCLK Pulse Width Low	4.7			µs
$t_{SU(STA)}$	Setup time for START condition	4.7			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	4			µs
$t_{SU(DAT)}$	Data setup time	250			ns
$t_{H(DAT)}$	Data hold time	300			ns
$t_{SU(STOP)}$	Setup time for STOP condition	4			µs
$t_{(BUF)}$	Bus free time between START and STOP condition	4.7			µs
$F_{S(CL)}$	Clock Frequency	10		100	kHz
ALARM LOGIC TIMING CHARACTERISTICS					
t_{ALM}	Time delay from status register bit toggling to ALERT: LO → HI transition	6		10	ms
HOST COMMUNICATION FAILURE					
$t_{timeout}$	SMBus bus release timeout	25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal		10		ms
t_{WDI}	Watchdog timeout period	140	170	200	s
OUTPUT BUFFER CHARACTERISTICS					
$V_{(SDAL)}$	Output LO voltage at SDA, $I_{(SDA)}$ = 3 mA			0.4	V

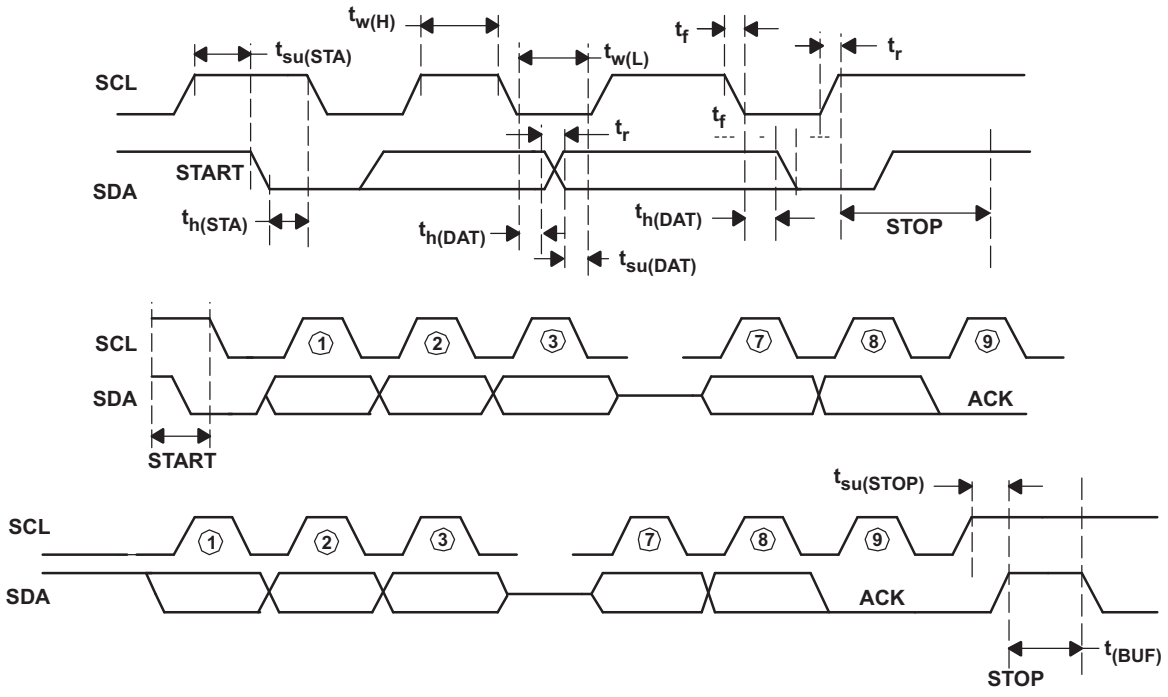


Figure 60.

FUNCTIONAL DESCRIPTION

SMBus Overview

An SMBus communication port provides a simple way for an SMBus compatible host to access system status information and reset fault modes. Functioning as a SLAVE port enables SMBus compatible hosts to WRITE to internal registers or READ from internal registers. The bq24721 SMBus port is a 2-wire bidirectional interface using SCL (clock) and SDA (data) pins; the SDA pin is open drain and requires an external pull-up. The SMBus is designed to operate at SCL frequencies up to 100 kHz. The standard 8 bit command is supported, the CMD part of the sequence is the 8 bit register address which is READ from or WRITE to. The bq24721 does not support packet error correction, PEC, as a mechanism to confirm proper communication between it and the host.

SMBus Address

The SMBus specification contains several global addresses, to which the slaves on the bus are required to respond. The bq24721 responds to the SBS charger addresses of 0×12 for writes and 0×13 for reads. The bq24721 only responds (ACK) to the above listed addresses, and does (NACK) not respond to any other address.

BYTE	BIT							
	MSB	6	5	4	3	2	1	LSB
bq24721 SMBus WRITE ADDRESS SBS Charger	0	0	0	1	0	0	1	0
bq24721 SMBus READ ADDRESS SBS Charger	0	0	0	1	0	0	1	1
COMMAND	0	0	0	1	C3	C2	C1	C0
I/O DATA BUS	D7	D6	D5	D4	D3	D2	D1	D0

Internal Register Map

The status data and control data is referenced by the following Commands.

COMMAND	R/W	REGISTER DESCRIPTION
0x12	R/W	Charger Mode
0x13	R	Charger Status
0x14	R/W	Charging Current
0x15	R/W	Charging Voltage
0x3F	R/W	Input Current

SMBus Bus Release

The bq24721 SMBus engine does not create START or STOP states on the SMBus bus during normal operation. However, if a 2 second (typical) SDA low timeout is exceeded the bq24721 releases the bus, thus creating a stop condition.

SMBus Communication Protocol

The following conventions is used when describing the communication protocol.

CONDITION	CODE
START sent from host	S
STOP sent from host	P
bq24721 SMBus slave address sent from host, bus direction set from host to bq24721 (WRITE)	hA0
bq24721 register address sent from bq24721, bus direction is from bq24721 to host (READ)	hA1
Non-valid SMBus slave address sent from host	hA_N
Valid bq24721 register address sent from host	HCMD
Nonvalid bq24721 register address sent from host	HCMD_N
I/O data byte (8 bits) sent from host to bq24721	hDATA
I/O data byte (8 bits) sent from bq24721 to host	bqDATA

CONDITION	CODE
Acknowledge (ACK) from host	hA
Not acknowledge (NACK) from host	hN
Acknowledge (ACK) from bq24721	bqA
Not acknowledge (NACK) from bq24721	bqN
Repeated Start	R

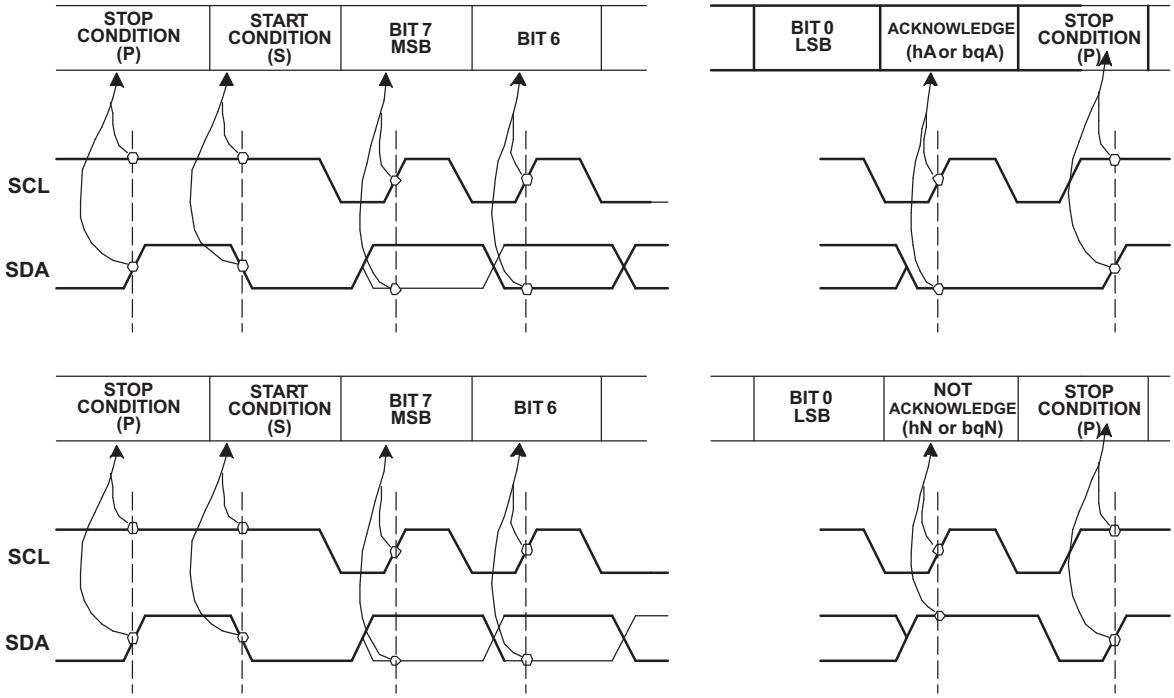


Figure 61.

SMBus Read/Write Sequences

The bq24721 supports the standard SMBus Word Write, as well as the SMBus Word READ. The basic SMBus word read protocol has the following steps:

1. Host sends a start and bq24721 SMBus slave write address
2. bq24721 ACKs that this is a valid SMBus address and that the bus is configured for write
3. Host sends bq24721 command
4. bq24721 ACKs that this is a valid command and stores the command for a possible read
5. Host sends a repeated start and bq24721 SMBus slave read address, reconfiguring the bus for read
6. bq24721 ACKs that this is a valid address and that bus is reconfigured
7. Bus is in read mode, bq24721 starts sending 2 bytes of data chosen by the command.

The SMBus write protocol is similar to the read, without the need for a repeated start and bus being set in write mode. If the address sent by host is not a valid address , the command is NACKed. The host can complete a READ or a WRITE sequence with either a STOP or a START. In a WRITE it is not necessary to end each word WRITE command with a STOP, a START has the same effect (repeated start).

Valid Write Sequences

The bq24721 always ACKs its own address. If the CMD points to an allowable READ or WRITE data bq24721 writes the command into its command register and send an ACK. If the CMD points to an nonallowed command bq24721 does NOT write the command into its command register and sends a NACK.

S	hA0	bqA

S	hA0	bqA	hCMD_N	bqN

Word Write

The data is written to a control register at the end of the ACK after the second byte in the sequence. If an word write sequence is intrupted by a STOP or START, no data is written to the device. The host can cancel a WRITE by sending a STOP or START before the trailing edge of ACK clock pulse.

S	hA0	bqA	hCMD	bqA	hDATA	bqA	hDATA	bqA	P

Valid Read Sequences

The bq24721 only ACKs its READ address if it occurs following a repeated start where the high SCL clock time is less then the $t_{W(H)}$, MAX of 50 µs. Upon receiving hA1, bq24721 outputs 2 bytes of data as indicated by the preceding command. The command sequence is terminated by a STOP. The START and the STOP both act as priority interrupts. If the host has been interrupted and is not sure where it left off, it sends a STOP and resets the bq24721 state machine to the Idle state. Once in idle state, bq24721 ignores all activity on the SCL and SDA lines until it receives a START. If a read sequence is terminated early by a START or STOP, the entire sequence must be restarted by the host for valid data.

S	hA0	bqA	hCMD	bqA	R	hA1	bqA	bqDATA	hA	bqDATA	hN	P

SMBus Word Read

A valid Command is required to write to the bq24721, and a valid Command is required to specify the data to be read. Once a read command is received the register data for the specified command is output to the host.

Nonvalid Sequences

START and non-hA0 or non-hA1 Address

A START followed by an address which is not bqA0 or bqA1 is NACKED.

Attempt to Specify Nonallowed Command

If the CMD points to a nonallowed command (reserved registers) , bq24721 sends a NACK back to the host. Note that bq24721 NACKS whether a stop is sent or not.

S	hA0	bqA	hCMD_N	bqN

S	hA_N	bqN

Status and Control Registers

The SMBUS-Like communication engine allows easy access to system status data contained in internal registers that contain information on current status for system power selection, charger mode and fault conditions. Any change on the state of those bits generates an interrupt request to the host ($\overline{ALARM}$ pin = HI).

Table 2. Status Register Latched Bits

ACOC/CHGOC LATCHES		
SET	**RESET**	**CONTROL LOGIC ACTION AT DETECTION**
Charger overcurrent detected	Host read register	Latches data going to status register, disables further updates on status register CHGOC bit until reset.
AC adapter overcurrent detected	Host read register	Latches data going to status register, disables further updates on ACOC bit until reset.

DESIGN CALCULATIONS EXAMPLE

System Requirements (See Figure 52)

For a system using a 20 V, ±5%, 80-W adapter, use a 12.6-V (3-cell) or 16.8-V (4-cell) battery, with a charge current regulation threshold of 4 A, and a precharge/wake-up current of 300 mA. The battery pack voltage varies from a deeply discharged voltage of 3-V per cell, and up to a regulation voltage of 4.2-V per cell— giving ranges of 9-V to 12.6-V for 3-cell batteries, and 12-V to 16.8-V for 4-cell batteries.

Select the Sense Resistors

The SBS specification was done based on a 10-mΩ sense resistor. The charger operates with low resistance. If the thermal dissipation is tolerable, a larger sense resistor (such as 20 mΩ) is used to provide greater accuracy in the regulation and current sense amplifier.

For this design example, a 10-mΩ sense resistor is selected for both the input current and output charge current sense resistors.

The power dissipation for each sense resistor is:

$$P_{(RSENSE_INPUT)} = R_{(SENSE_DPM)} \times I_{(INPUT_REG)}{}^{2} = 10\ m\Omega \times \left(\frac{80\ W}{19\ V}\right)^{2} = 177\ mW \quad (4)$$

where the maximum input current is the input power limit divided by the input voltage.

$$P_{(RSENSE_CHRG)} = R_{(SENSE_CHRG)} \times I_{(INPUT_REG)}{}^{2} = 10\ m\Omega \times (4A)^{2} = 160\ mW \quad (5)$$

A 1 W, 2010 rating provides sufficient margin.

Select Switching Frequency:

Select switching frequency = 300 kHz.

Selecting the Output Inductor

Inductor is designed for current ripple 40% of the 4-A regulation threshold ($I_{(RIPPLE)}$ = 1.6 A).

$$L_{out} = \frac{\left(V_I max - V_{(BAT)} min\right) \times \left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)}{40\% \times I_{(CHRG_REG)}} \quad (6)$$

Where the $V_I$max is the maximum input voltage, $V_{(BAT)}$min is the minimum battery voltage, and f_{SW} is the switching frequency.

DESIGN CALCULATIONS EXAMPLE (continued)

$$L_{out} = \frac{(21\ V - 9\ V) \times \left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{40\% \times 4A} \quad (7)$$

L_{OUT} = 11 µH ≈ 10 µH, a standard 10-µH part is selected.

Selecting the Output Capacitor

The rule for selecting ceramic capacitors as the bulk output capacitor is to select 10 µF per 1 A of charge current. In this case, a 4-A charge regulation current requires 40-µF output capacitance. Four 10-µF X5R 25-V ceramic capacitors are recommended instead of 22 µF, because of a better trade-off with the voltage rating, size, capacitance variation, and cost.

The output capacitors is divided evenly. Place the charge current sense resistor between the capacitors. This provides filtering and a higher phase margin for accurate current sensing and regulation.

With this output capacitance, the steady state output ripple voltage is:

$$V_{O(RIPPLE)} = \frac{I_{(RIPPLE)} \times \left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)}{C_O} + \left(\frac{ESR}{2} \times \frac{I_{(RIPPLE)}}{2} + \left(\frac{ESR}{2} + R_{(SENSE)}\right) \times \frac{I_{(RIPPLE)}}{2}\right) + ESL \times \frac{I_{(RIPPLE)}}{\left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)} \quad (8)$$

where ESR is the equivalent series resistance of the capacitors (10 mΩ each giving 5 mΩ for two capacitors before the sense resistor and 5 mΩ for two capacitors after the sense resistor), and ESL is the equivalent series inductance of the capacitors (0.5 nH).

$$V_{O(RIPPLE)} = \frac{1.6\ A \times \left(\frac{9V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{40\ \mu F} + (5\ m\Omega \times 0.7\ A + 15\ m\Omega \times 0.7\ A) + \left[0.5\ nH \times \frac{1.6\ A}{\left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}\right] \quad (9)$$

$V_{(OUT_RIPPLE)}$ = 57 mV + 14 mV + 0.56 mV = 72 mV ripple voltage (which equals 0.6% of 12.6 V) worst case peak-to-peak steady state ripple when the battery is removed and the charger is on.

Selecting the Input Capacitor

The input capacitance is at a minimum the same as the output capacitance. Lower capacitance is used directly at the converter input when the input is tied directly to the system load while charging. The capacitors are placed as close as possible to the high-side FET drain (PVCC) and low-side FET source (PGND). A rule for selecting ceramic capacitors as the bulk output capacitor is to select 10 µF per 1 A of charge current. In this case, a 4-A charge regulation current requires 40-µF output capacitance. Four 10-µF X5R 25-V ceramic capacitors are recommended instead of 22 µF, because of a better trade-off with the voltage rating, size, capacitance variation, and cost. The input ripple voltage is usually larger because the input current ripple through the capacitor is the full charge current.

$$V_{I(RIPPLE)} = \frac{I_{(CHRG)} \times \left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)}{C_I} + \left(\frac{ESR}{4} \times I_{(CHRG)}\right) + ESL \times \frac{I_{(CHRG)}}{\left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)} \quad (10)$$

where $I_{(CHRG)}$ is the charge regulation current.

DESIGN CALCULATIONS EXAMPLE (continued)

$$V_{I(RIPPLE)} = \frac{4\ A \times \left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{40\ \mu F} + \left(\frac{10\ m\Omega}{4} \times 4\ A\right) + 0.5\ nH \times \frac{4\ A}{\left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)} \quad (11)$$

$V_{I(RIPPLE)}$ = 143 mV + 10 mV + 1.4 mV = 154 mV which is 0.77% of the nominal 20-V input voltage.

Note that a single 10-µF capacitor is used from PVCC (close to the drain of the high-side FET) to PGND, when the system load is connected to PVCC, because the capacitors on the system rail provide the hold-up capacitance needed.

Selecting the High-Side Power MOSFET, Q3

The high-side power MOSFET should be an NMOS power MOSFET with a standard voltage rating of 30 V to support the 20-V input voltage. The current carrying capability should be at least 2x the maximum charge current. Both the $r_{DS(on)}$ and the gate charge contribute to the power dissipation, while the worst case condition occurs at max duty cycle (minimum input voltage and maximum battery voltage). The gate drive losses are the only component that directly dissipate heat in the charger IC.

The FDS6680A was selected. The FDS6680A is a NMOS, 30-V, 12-mΩ device in an SO-8 package.

The conduction losses equal:

$$P_{(CON)} = I_{(CHRG)}{}^2 \times \left[\sqrt{\frac{V_{(BAT)}\,max}{V_I\,min}}\right] \times \left(r_{DS(on)}\right) \quad (12)$$

where the charger's 6-V gate drive voltage helps reduce the $r_{DS(on)}$ for lower conduction losses.

The first order approximation switching losses equal:

$$P_{(SW)} = I_{(CHRG)} \times V_I\,min \times \left[\frac{\left(Q_{(GS)} + Q_{(GD)}\right)}{i_{(G)}}\right] \times f_{SW} \quad (13)$$

and the gate drive losses are:

$P_{(GD)} = Q_{(GTOT)} \times V_I mim \times f_{SW}$.

Where $G_{(GS)}$ is the gate charge from threshold current conducts until full charge current conducts; $Q_{(GD)}$ is the miller charge where the drain voltage drops, and the $Q_{(GTOT)}$ is the total gate charge form off to fully-enhanced on. The full input voltage is used for gate drive calculation because the internal gate drive regulator dissipates the drop from input voltage to the 6-V output voltage which must be added to charging the gates to 6-V every cycle.

$$P_{(CON)} = (4A)^2 \times \left(\sqrt{\frac{16.8\ V}{19\ V}}\right) \times (12\ m\Omega) = 180\ mW$$

$$P_{(SW)} = 4\ A \times 19\ V \times \left(\frac{(5\ nC + 7\ nC)}{IA}\right) \times 300\ kHz = 274\ mW$$

$$P_{(GD)} = 18\ nC \times 19\ V \times 300\ kHz = 103\ mW \quad (14)$$

Selecting the Low-Side Power MOSFET, Q4

The low-side power MOSFET should be an NMOS power MOSFET with a standard voltage rating of 30 V to support the 20-V input voltage. The current carrying capability should be at least 2x the maximum charge current. By nature of the synchronous rectifier operation, the drain-to-source voltage is always low at full charge current when the low-side FET turns on—this makes switching losses insignificant, except for the reverse

DESIGN CALCULATIONS EXAMPLE (continued)

recovery and dead-time contributors that arise from letting the body-diode conduct. The conduction losses and gate drive losses are the dominant power dissipation; while, the worst case condition occurs at minimum duty cycle (maximum input voltage and minimum battery voltage). The gate drive losses are the only component that directly dissipate heat in the charger IC. Note that the reverse recovery losses are included in this calculation, but the dissipation occurs in the high-side power MOSFET.

The FDS6670A was selected. The FDS6670A is an NMOS, 30-V, 12-mΩ device in an SO-8 package.

The conduction losses equal:

$$P_{(CON)} = I_{(CHRG)}^{2} \times \left(\sqrt{\frac{V_{(BAT)}\,max}{V_I\,min}} \right) \times \left(r_{DS(on)} \right) \tag{15}$$

where the charger's 6-V gate drive voltage helps reduce the $r_{DS(on)}$ for lower conduction losses.

The first order approximation switching losses are dominated by reverse recovery losses and dead-time losses given by:

$$P_{(SW)} = V_I max \times Q_{(RR)} \times f_{SW} + I_{(CGRG)} \times V_{(F)} \times 2 \times t_{(dead\text{-}time)} \times f_{SW}$$

and the gate drive losses are :

$$P_{(GD)} = Q_{(GTOT)} \times V_I mim \times f_{SW}.$$

Where $t_{(dead\text{-}time)}$ is the dead-time where both FETs are off on either edge, $Q_{(RR)}$ is the reverse recovery charge, $Q_{(GTOT)}$ is the total gate charge form off to fully-enhanced on. The full input voltage is used for gate drive calculation because the internal gate drive regulator dissipates the drop from input voltage to the 6-V output voltage which must be added to charging the gates to 6 V every cycle.

$$P_{(CON)} = (4A)^2 \times \left(\sqrt{1 - \frac{9\ V}{21\ V}} \right) \times (9\ m\Omega) = 109\ mW$$

$$P_{(SW)} = 21\ V \times 21\ nC \times 300\ kHz + 4\ A \times 0.8\ V \times 2 \times 30\ ns \times 300\ kHz = 132\ mW + 57.6\ mW = 190\ mW$$

$$P_{(GD)} = 26\ nC \times 21\ V \times 300\ kHz = 164\ mW \tag{16}$$

Power MOSFET Thermal Limit Verification

The thermal limit verification allows for a 40°C temperature rise from 85°C ambient to 124°C silicon junction temperatures. For SO-9, the $R\theta_{JA}$ is 50°C/W.

The low-side power FET expected temperature rise is:

$$\Delta T_{(LOW-SIDE)} = R_{thetaJA} \times P_{(LOSS_LOW_SIDE)} = \frac{50^oC}{W} \times (109\ mW + 57.6\ mW + 164\ mW) = 16^oC \tag{17}$$

The high-side power FET expected temperature rise is:

$$\Delta T_{(HIGH-SIDE)} = R_\theta JA \times P_{(LOSS_HIGH_SIDE)} = \frac{50^oC}{W} \times (180\ mW + 274\ mW + 103\ mW + 134\ mW) = 35^oC \tag{18}$$

Optional Schottky Diode across Low-Side FET

An optional Schottky diode can be used across the low-side power MOSFET (with cathode to drain and anode to source) to help reduce both the $V_{(F)}$ losses and reverse recovery losses. The Schottky diode is selected on the basis of the $V_{(F)}$ at $I_{(CHRG)}$, but a power rating for the full current is not required since the Schottky primarily conducts during the dead-times, which is a fraction of the total switching period.

Power loss for the Schottky are:

$$P_{(SW)} = I_{(CHRG)} \times V_F \times 2 \times t_{(dead\text{-}time)} \times f_{SW} = 4\ A \times 0.5\ V \times 2 \times 30\ ns \times 300\ kHz = 36\ mW$$

DESIGN CALCULATIONS EXAMPLE (continued)

Selecting the System Power Selector Power MOSFETs, Q1, Q2, Q5

The system power selector power MOSFETs (Q1, Q2, Q5) must be PMOS power MOSFETs with a standard voltage rating of 30 V to support the 20-V input voltage, and must have a low $r_{DS(on)}$ to minimize conduction losses. The continuous current carrying capability should be at least 2x the maximum charge current. Both the $r_{DS(on)}$ and the gate charge contribute to the power dissipation, while the worst case condition occurs at max duty cycle (minimum input voltage and maximum battery voltage). The gate drive losses are the only component that directly dissipate heat in the charger IC.

The SI4435 was selected for Q1, Q2, and Q5. The SI4435 is a PMOS, 30-V, 35-mΩ device in an SO-8 package.

The conduction losses equal:

$P_{(CON)} = I_{(RMS)}^2 \times r_{DS(on)}$,

$I_{(RMS_Q1)} = I_{(RMS_Q2)} = I_{(RMS_Q5)} = I_{(SYS)}max$

where $I_{(RMS)}$ is the RMS current expected for each MOSFET, and $I_{(SYS)}max$ is the maximum continuous system current.

Note that for Q1, the charge current is not used because the charge current drops to zero as the system current ($I_{(SYS)}max$) equals or exceeds the programmed input current DAC threshold (IDPM). This is assuming the typical case where $I_{(SYS)}max > I_{(DPM)}$.

The system power selector's -6-V gate drive voltage helps reduce the $r_{DS(on)}$ for lower conduction losses.

Calculate the Bootstrap Capacitor

The minimum bootstrap capacitor is calculated by the high-side turn-on charge requirements per cycle and the gate drive voltage required. The total gate charge for the FDS6680A high-side power FET is $Q_{(GTOT)}$ = 18 nC, and the maximum gate drive voltage drop allowed is $V_{(DROP)}$ = 0.5 V. The switching frequency of 300 kHz gives a cycle period of 3.33 µs.

$$C_{(BTST)}\,min = \frac{Q_{(GTOT)}}{V_{(DROP)}\,max} = \frac{18\ nC}{0.5\ V} = 36\ nF \tag{19}$$

Select $C_{(BTST)}$ = C12 = 100 nF = 0.1 µF. Connect C12 between the PH and the BTST pins. Also connect a bootstrap Schottky diode, D2 , from the REGN pin to the BTST pin. The current rating for the bootstrap diode, D2, is determined by:

$$I_{(DBTST_RATING)}\,min = \frac{Q_{(GTOT)}}{T_S} = \frac{18\ nC}{3.33\ \mu s} = 5.4\ mA \tag{20}$$

Use a 100-mA rated Schottky diode.

An optional 4.7-Ω bootstrap resistor is placed between the BTST pin and the node where C12 and D2 are connected, in order to minimize ringing by lowering slew rate on the PH node voltage. For lower gate charge FETs, a larger resistor value can be used up to 10 Ω or 15 Ω. Using larger resistor values increase the switching losses, and lower the efficiency.

Calculate the ACDET Programming Resistors

The adapter is detected when the ACDET pin voltage (sensed adapter input voltage scaled down by resistor divider) exceeds the 1.2 V. The adapter voltage threshold is set to a value less than the minimum adapter voltage, and higher than the maximum battery pack voltage. [Important: don't set the value less than the maximum battery pack voltage, otherwise adapter removal is never detected when the battery is connected, and the battery pack could potentially be drained when no adapter is present]. For this design example, $V_I$min = 19 V, $V_{(BAT)}$ = 16.8 V; therefore, select an adapter detect voltage of $V_{(ADAPT_DET)}$ = 18 V.

Using the equation: $V_{(ADAPT_DET)} = 1.2\ V \times \frac{R3 + R4}{R4}$

and setting $V_{(ADAPT_DET)}$ = 18 V, and selecting (R3 + R4) ≈ 500 Ω.

Calculate the standard 1% resistor values of R4 = 33.2 kΩ, and R4 = 464 kΩ.

DESIGN CALCULATIONS EXAMPLE (continued)

Calculate the ISYNSET Programming Resistor

The inductor current ripple is defined by:

$$\Delta I_L = \frac{\left(V_I max - V_{(BAT)} min\right) \times \left(\frac{V_{(BAT)}{}^{min}}{V_I{}^{max}}\right) \times \left(\frac{1}{f_{SW}}\right)}{L_{out}} \quad (21)$$

where the $V_I$max is the maximum input voltage, $V_{(BAT)}$min is the minimum battery voltage, and f_{SW} is the switching frequency.

$$\Delta I_L = \frac{(21\ V - 9\ V) \times \left(\frac{9\ V}{21\ V}\right) \times \left(\frac{1}{300\ kHz}\right)}{10\ \mu H} \quad (22)$$

The worst case inductor current ripple is ΔI_L = 1.71 A. To set the $I_{(SYNSET)}$ threshold to a value between $\frac{\Delta I_L}{2}$ and ΔI_L . Set $I_{(SYNSET)}$ = 1.5 A. $R_{(SYNSET)}$ is calculated by the following equation:

$$R12 = R_{(SYNSET)} = \frac{1\ V \times 500\ \Omega}{I_{(SYNSET)} \times R_{(SENSE)}} = \frac{1\ V \times 500\ \Omega}{1.5\ A \times 10\ m\Omega} = 33\ k\Omega. \quad (23)$$

Calculate the Thermistor Sense, TS, Programming Resistors

The TS comparator programming resistors need the cold pack temperature to disable charge defined, and the hot pack temperature to disable charge defined. The battery cell manufacturer defines the limits. For this example, the pack charging temperature limits are: cold temperature = $T_{(COLD)}$ = 0°C, and hot temperature $T_{(HOT)}$ = 45°C. The charger is not allowed to charge at these temperatures and outside this range, to protect the battery pack.

Using an industry standard Semitec 202AT NTC Thermistor, the thermistor cold temperature resistance is $R_{(TH_C)}$ = 64.88 kΩ; and the thermistor hot temperature resistance of $R_{(TH_H)}$ = 8.716 kΩ. These values are found in the 202AT thermistor manufacturer's data sheet.

The comparator voltage cold limit threshold is $V_{(LTF)}$ = 73.5% of VREF5 = 0.735 × 5 V = 3.675 V, where VREF5 = 5 V. Likewise, the comparator voltage hot limit threshold is $V_{(HTF)}$ = 34.4% of VREF5 = 0.344 × 5 V = 1.72 V.

Since the internal references are with respect to VREF5, R5 is connected from the VREF5 pin to the TS pin, and connect R13 from the TS pin to the AGND pin. The R5 and R13 resistor values are calculated by solving the following two equations:

$$R_{(VREF_TS)} = R5 = \frac{R_{(TH_C)} \times R_{(TH_H)} \times VREF5 \times \left(V_{(LTF)} - V_{(HTF)}\right)}{V_{(LTF)} \times V_{(HTF)} \times \left(R_{(TH_C)} - R_{(TH_H)}\right)} \quad (24)$$

$$R_{(TS_AGND)} = R_{13} = \frac{R_{(TH_C)} \times R_{(TH_H)} \times VREF5 \times \left(V_{(HTF)} - V_{(LTF)}\right)}{\left(R_{(TH_H)} \times V_{(LTF)} \times VREF5\right) + \left(R_{(TH_C)} \times V_{(LTF)} \times V_{(HTF)}\right) - \left(R_{(TH_C)} \times V_{(HTF)} \times VREF5\right) + \left(R_{(TH_H)} \times V_{(LTF)} \times V_{(HTF)}\right)} \quad (25)$$

giving standard 1% resistor values of R5 = 15.8 kΩ, and R13 = 130 kΩ.

Using these programming, check that when the battery pack is removed (i.e. the Thermistor is disconnected), the TS voltage is pulled-above the battery detect threshold ($V_{(TSDET)}$ = 0.85 × 5 V = 4.25 V).

$$V_{(NO_PACK)} = \frac{VREF5 \times R13}{(R5 + R13)} = \frac{5\ V \times 130\ k\Omega}{(15.8\ k\Omega + 130\ k\Omega)} = 4.458\ V. \quad (26)$$

$V_{(NO_PACK)} > V_{(TSDET)}$ allowing for proper battery detect.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24721CRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24721CRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24721CRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24721CRHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24721RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24721RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24721RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24721RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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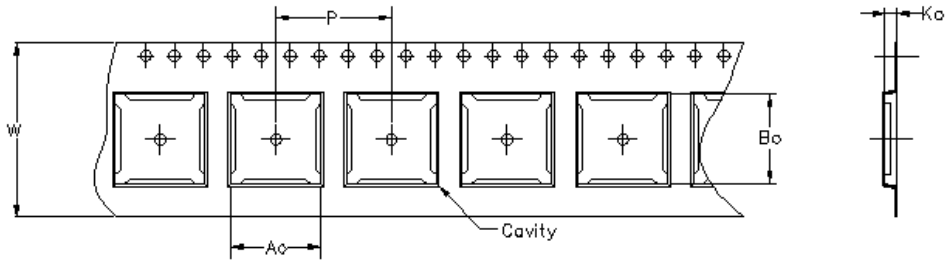
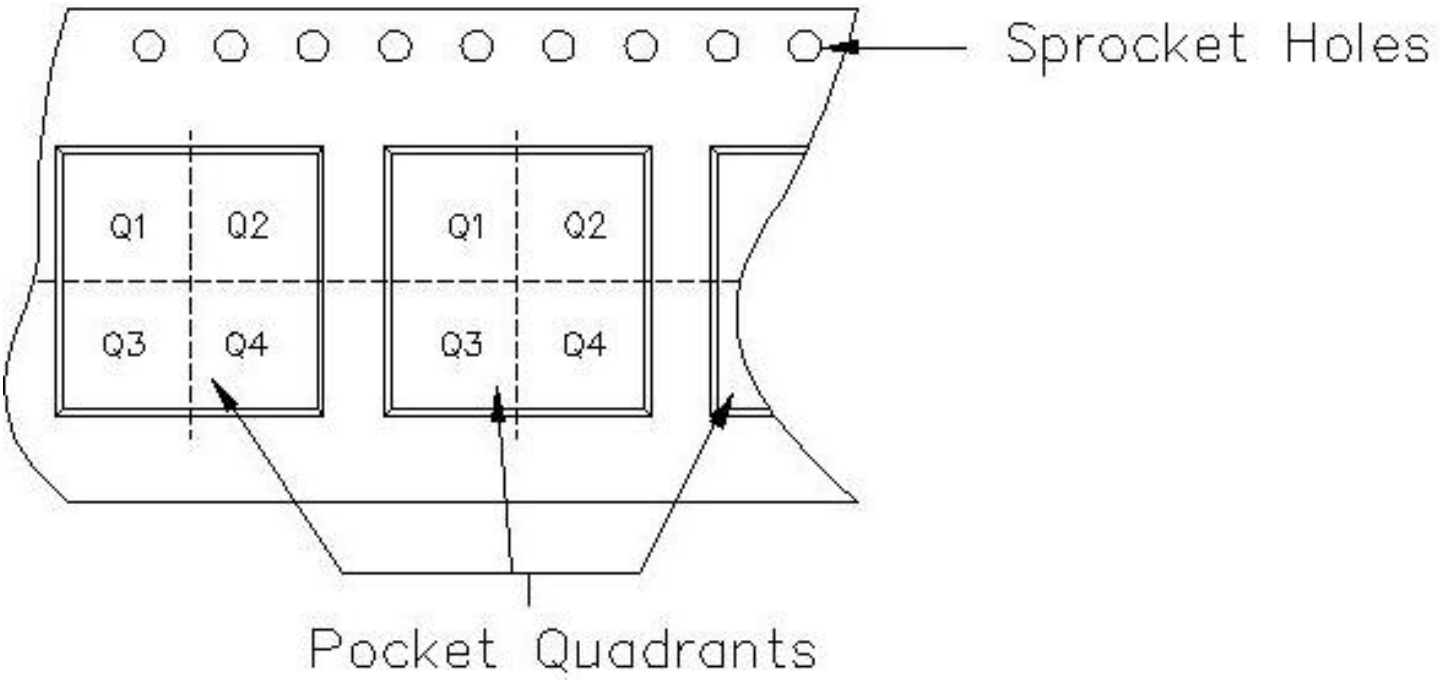


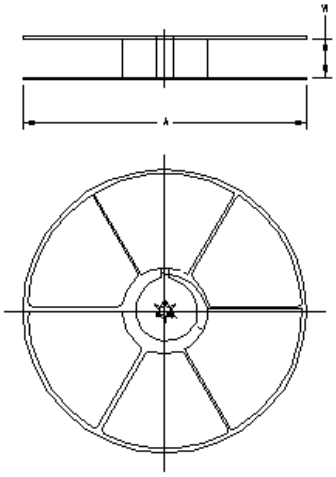
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



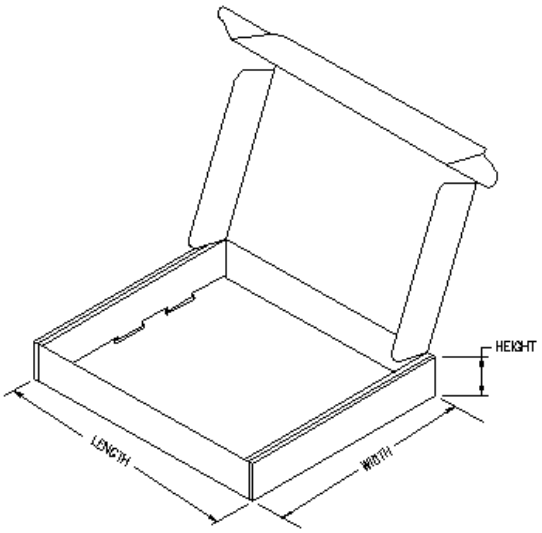
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24721CRHBR	RHB	32	MLA	330	12	5.3	5.3	1.5	8	12	PKGORNT2TR-MSP
BQ24721CRHBT	RHB	32	MLA	180	12	5.3	5.3	1.5	8	12	PKGORNT2TR-MSP
BQ24721RHBT	RHB	32	MLA	180	12	5.3	5.3	1.5	8	12	PKGORNT2TR-MSP

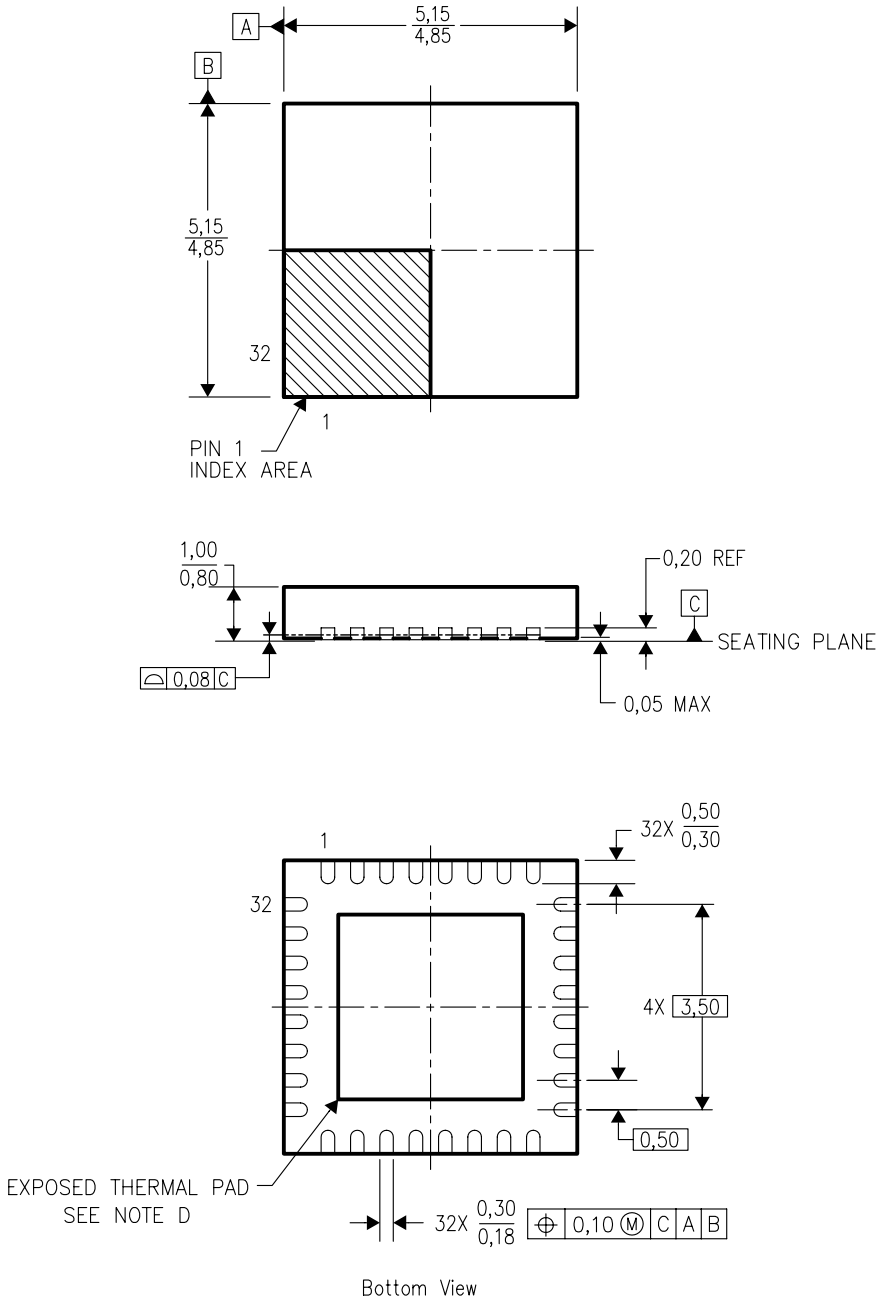


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
BQ24721CRHBR	RHB	32	MLA	346.0	346.0	29.0
BQ24721CRHBT	RHB	32	MLA	190.0	212.7	31.75
BQ24721RHBT	RHB	32	MLA	190.0	212.7	31.75


HEIGHT
LENGTH
WIDTH

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

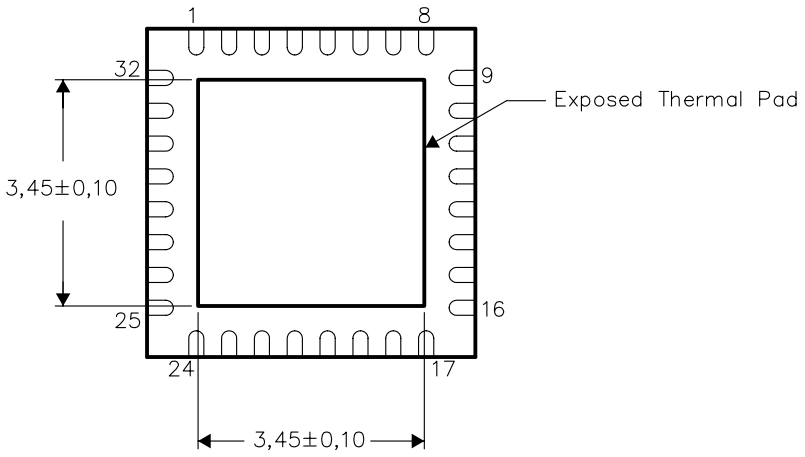
RHB (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

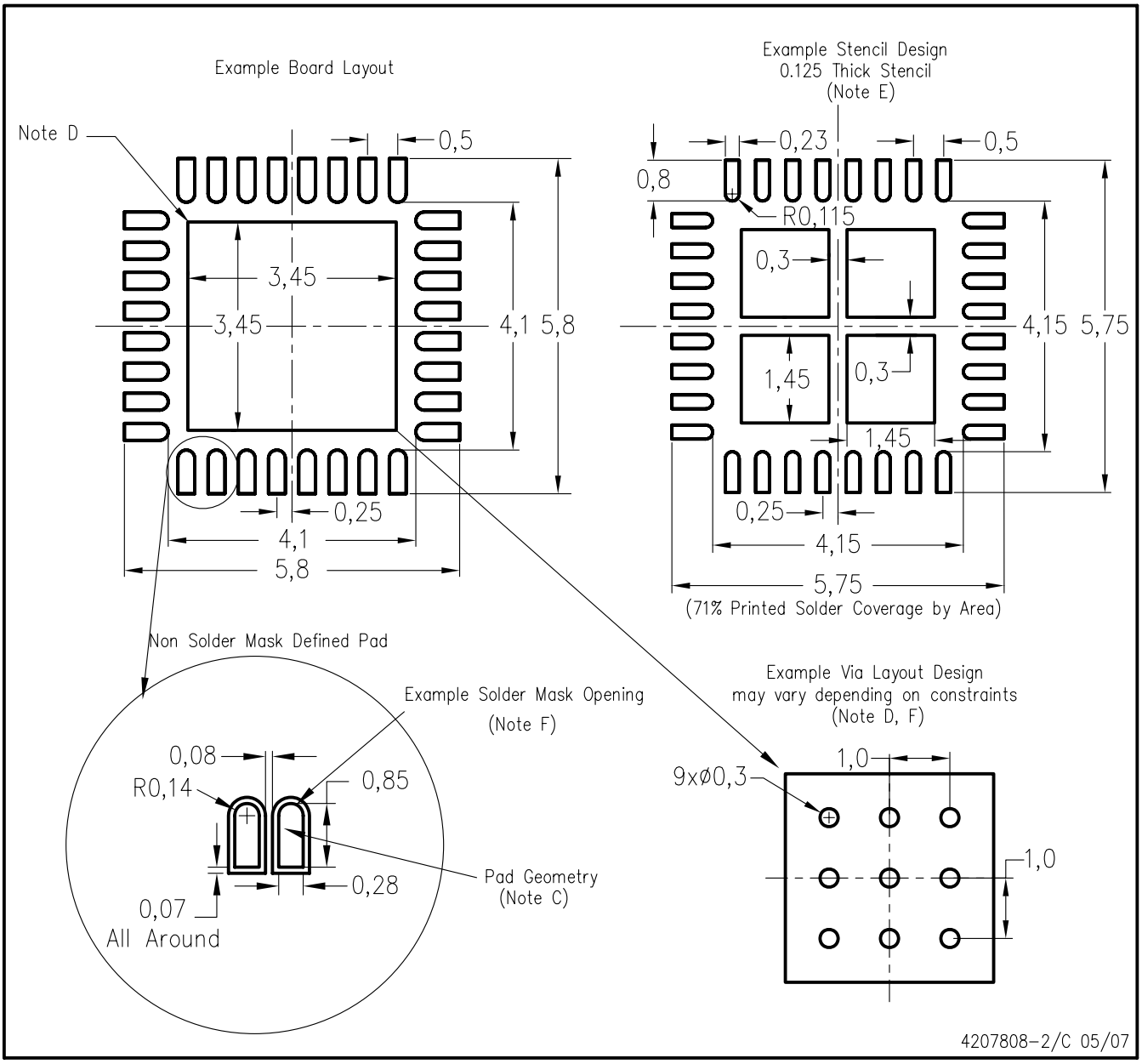


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S–PQFP–N32)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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