3 Channel DC-DC Converters +LDO +LSW PMIC with I²C Interface for Industrial and Automotive Application

General Description

The RT2070T is a highly-integrated low-power high-performance analog SOC with PMIC (Power Management IC) in one single chip designed for Industrial/Automotive applications.

The RT2070T PMIC includes one high voltage synchronous step-down DC-DC converter, two low voltage synchronous step-down DC-DC converters, one low dropout LDO and one load switch with soft-start control and current limit. All MOSFETs are integrated, and compensation networks are built-in.

The RT2070T also uses I²C interface to set timing of power on/off, sequence and discharge function, and includes power good indicator (PGOOD).

The RT2070T is an Automotive-Grade Product that is AEC-Q100 Grade 1 Qualified and provides fault condition protections, including over-current protection, under-voltage lockout, over-voltage protection and over-temperature protection.

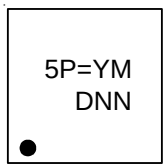
Applications

- Industrial/Automotive Camera Module
- Car Infotainment

Features

- **Input Voltage Operating Range is 4.5V to 15V**
- **CH1 HV-Step-Down Regulator : V_{IN} Range is 4.5V to 15V**
  - **Support Up to 2A Loading With Up to 90% Efficiency**
  - **Switching Frequency is 2MHz**
- **CH2/3 LV Step-Down Regulator : V_{IN} Range is 2.7V to 5.5V**
  - **Support Up to 1A Loading, With Up to 90% Efficiency**
  - **Switching Frequency is 2MHz**
- **Linear Regulator : V_{IN} Range is 2.7V to 5.5V**
  - **Max Loading 0.5A**
- **Load Switch (LSW) : V_{IN} Range is 2.7V to 5.5V**
  - **Max Loading 0.5A**
- **Sequence Can be Controlled by Setting the Resistances of the SEQ Pin**
- **AEC-Q100 Grade 1 Qualified**

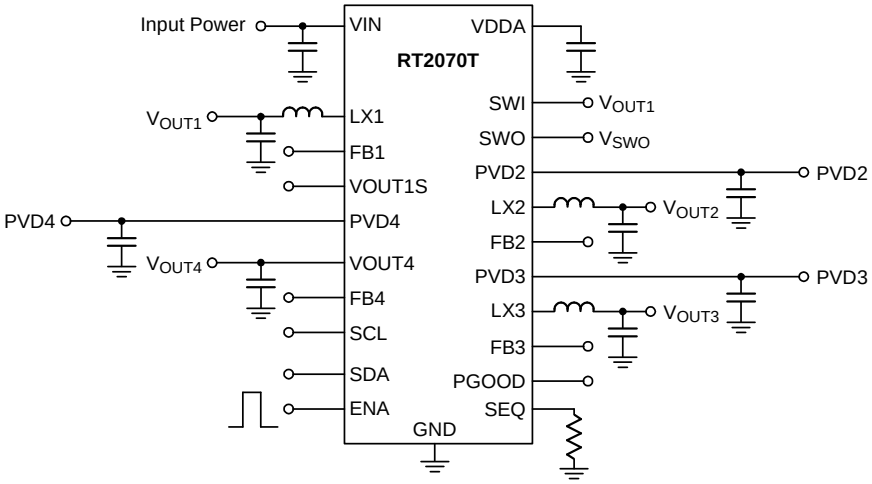
Marking Information



5P= : Product Code

YMDNN : Date Code

Simplified Application Circuit



Ordering Information

RT2070T □ □

- Package Type
  - QW : WQFN-24L 4x4 (W-Type)
    (Exposed Pad-Option 1)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

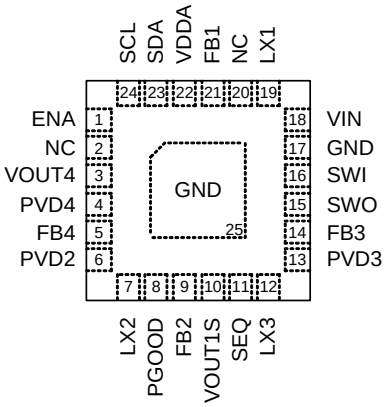
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)

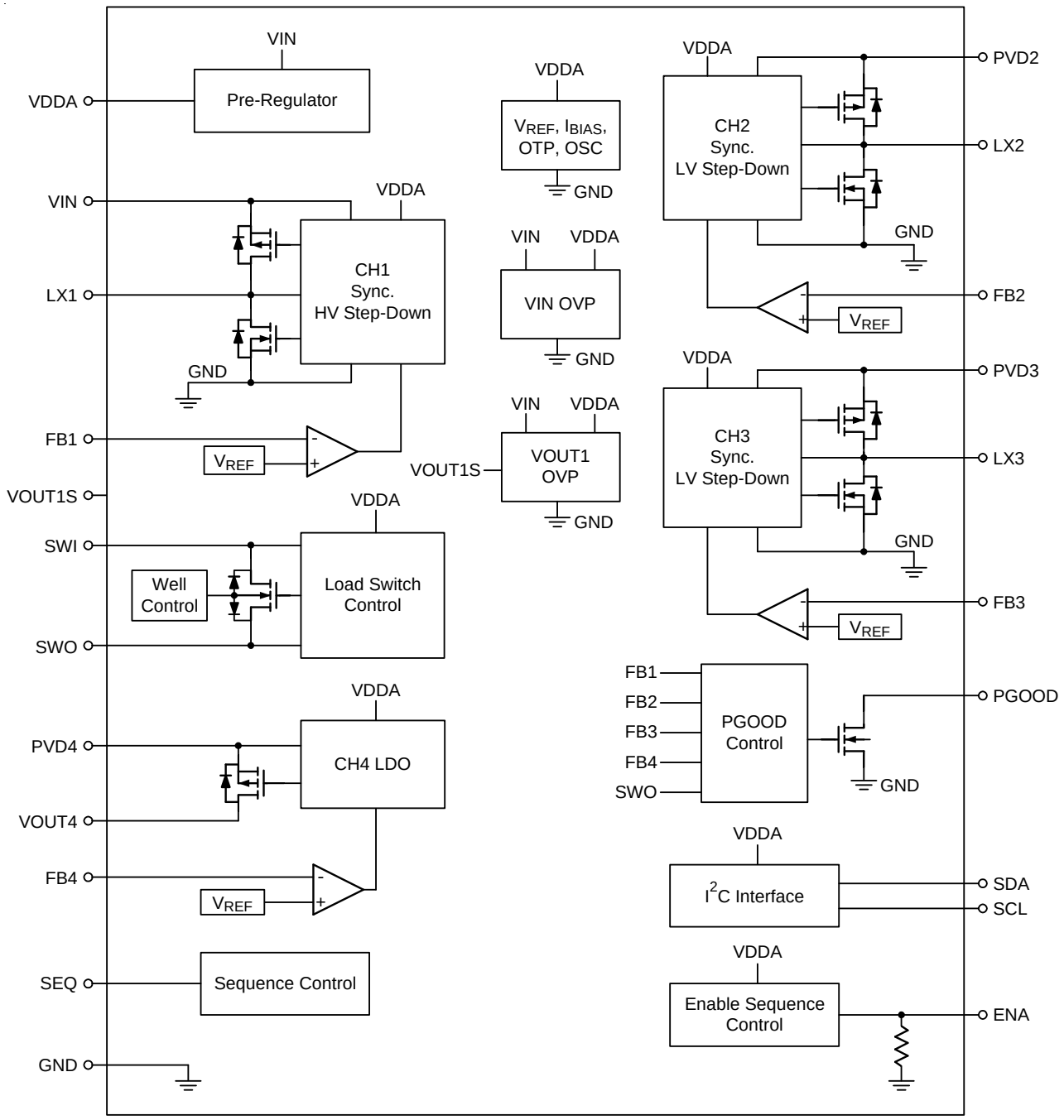


WQFN-24L 4X4

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	ENA	IC enable control input. Hi active. Internal pull-down resister (100kΩ).
2, 20	NC	No internal connection.
3	VOUT4	Output voltage regulation node for LDO4.
4	PVD4	Power input for LDO4.
5	FB4	Feedback voltage input for LDO4
6	PVD2	Power input for Buck2.
7	LX2	Switch node of Buck2.
8	PGOOD	Buck1 to Buck 3, LDO4 and LSW PGOOD output node by open drain. Hi active.
9	FB2	Feedback voltage input for Buck2.
10	VOUT1S	HV buck output voltage for OVP detection. Input HV buck (CH1) output.
11	SEQ	Power sequence selection.
12	LX3	Switch node of Buck3.
13	PVD3	Power input for Buck3.
14	FB3	Feedback voltage input for Buck3.
15	SWO	Load switch output.
16	SWI	Load switch input.
17, 25 (Exposed Pad)	GND	IC power ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation and current flow.
18	VIN	Power input for Buck1.
19	LX1	Switch node of Buck1.
21	FB1	Feedback voltage input for Buck1.
22	VDDA	IC internal analog power output 4.45V (typ.). Only 1μF and SCL/SDA pull up resister can be connected.
23	SDA	I^2C data input/output.
24	SCL	I^2C clock input.

Functional Block Diagram



Operation

The RT2070T is a highly-integrated solution for automotive systems, including a 1-CH HV step-down DC-DC converter, 2-CH LV step-down DC-DC converter and 1-CH LDO. The RT2070T application mechanism will be introduced in later sections.

The power-on and power-off sequences are detected in the SEQ pin. Additionally, users control the next power on/off sequence by setting I^2C registers from A01 to A12 when VDDA exists.

When the ENA pin is at Hi level, the PMIC follows the power-on sequence to turn on channels.

The IC turns on base and calibrates. Time is less than 500μs; during this time, the IC doesn't allow users to set I^2C data.

Pre-Regulator

This HV regulator is designed to handle input operation range of 4.5V to 15V. The regulator provides low voltage power to supply the internal control circuits and avoid connecting any load from VDDA pin. In noisy environments, a 1μF decoupling capacitor must be connected between VDDA and GND.

The I^2C compatible interface remains fully functional if VIN and VDDA are present. If the VDDA is under the threshold voltage, all internal registers are reset to their default values.

Over-Temperature Protection

An Over-Temperature Protection (OTP) is featured in the device. The protection is triggered to force device shutdown when the junction temperature exceeds 160°C typically. If OTP is set to Hiccup once the junction temperature drops below the hysteresis 20°C typically, the device is re-enabled and automatically reinstated the power-on sequence.

Input Over-Voltage Protection

The device provides an input Over-Voltage Protection (OVP) once the input voltage exceeds 15.5V typically; the OVP function is started and all channels will be turned off after 5ms. If OVP is set to Hiccup, once the input voltage drops below the hysteresis 2V typically, the device is re-enabled and automatically reinstates the power-on sequence. This OVP feature can easily minimize the input overshoot.

ENA : IC Enable Pin

The ENA pin is a device enable input. Pulling the ENA pin to logic low that is typically less than the set threshold voltage 1.2V shuts the device down and it enters a low quiescent current state of about 20μA. The regulator starts switching again once the ENA pin voltage exceeds the threshold voltage of 2V. In addition, the ENA pin features an internal 100kΩ pull-low resistor.

Power Good (PGOOD) Control

The power good output is an open-drain output and needs to be connected to a voltage source with a pull-up 10kΩ resistor to avoid PGOOD floating. Each channel turns on according to power-on sequence. When the last channel reaches 90% of its target voltage, PMU (Power Management Unit) starts counting t_{PGOOD} = 5ms (Power Good Delay Time) then pulls PGOOD Hi until ENA is pulled low or any other protection happens.

Absolute Maximum Ratings (Note 1)

- Analog Base Input Voltage, VIN ---------- –0.3V to 20V
- Control Output Voltage, PGOOD ---------- –0.3V to 6V
- Control Input Voltage, ENA ---------- –0.3V to 15V
- HV Buck Power Switch (DC), LX1 ---------- –0.3V to 15V
- LV Buck Input Voltage, PVD2/3 ---------- –0.3V to 6V
- LV Buck Power Switch (DC), LX2, LX3 ---------- –0.3V to 6V
- LV Buck Power Switch (Spike Voltage < 200ns), LX2, LX3 ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 4x4 ---------- 4.46W
- Package Thermal Resistance (Note 2) (Note 3)
  WQFN-24L 4x4, θ_{JA} ---------- 28°C/W
  WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 5)

- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(Note 8)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Operation Voltage Range			4.5	--	15	V
Quiescent Current	I_Q	V_{IN} = 5V, Bucks and LDOs are ON with no load, HVBuck switching, LVBucks are in FCCM mode.	8	10	12	mA
	I_{Q_PSM}	V_{IN} = 5V, Bucks and LDOs are ON with no load, HVBuck non-switching, LVBucks are in PSM mode.	600	1000	1200	µA
Shutdown Current	I_{SHD}	V_{IN} = 5V, ENA = 0V, LDOs, Bucks are OFF.	2	7	20	µA
Over-Temperature Protection	OTP		150	160	170	°C
OTP Hysteresis (Note 6)	OTP_HYS		10	20	30	°C
VIN OVP (Hysteresis High)	OVP		14.5	15.5	16.5	V
VIN OVP Hysteresis (Gap) (Note 7)	OVP_HYS		1.5	2	2.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN UVLO2	UVLO2		3.7	3.9	4.1	V
UVLO2 Hysteresis (Gap)	UVLO2_HYS		0.4	0.5	0.6	V
VDDA Voltage			4.2	4.5	4.8	V
Switching Frequency (CH1/CH2/CH3)	f_{SW}		2 –10%	2	2 +10%	MHz
CH1 HV-Buck						
Input Voltage Range	V_{IN}		4.5	--	15	V
Output Voltage Range	V_{OUT}		1.6	--	5	V
Feedback Voltage Accuracy	FB1		0.8 – 3%	0.8	0.8 + 3%	V
FB1 Under-Voltage Protection	FB1_UVP	FB1 = FB1 x 0.5 (50%)	0.3	0.4	0.5	V
Suggest Inductor	L_{HVBuck}	Refer to Typical Application Circuit	--	4.7	--	µH
Current Limit	CL1	T_A = 25℃	3 – 15%	3	3 + 15%	A
	CL1_T	–40℃ ≤ T_A ≤ 125℃	3 – 25%	3	3 + 25%	
Load Regulation		T_A = 25℃, V_{IN} = 6V, V_{OUT} = 3.3V, Load = 0mA to 2000mA Refer to Typical Operating Characteristics	–1	--	1	%
Line Regulation		T_A = 25℃, V_{IN} = 5V to 15V, V_{OUT} = 3.3V, Load = 1000mA Refer to Typical Operating Characteristics	–1	--	1	%
P-MOSFET On-Resistance	$R_{DS\_ON\_P}$	V_{IN} = 5V, I_{LX1} = 800mA	230	330	470	mΩ
N-MOSFET On-Resistance	$R_{DS\_ON\_N}$	V_{IN} = 5V, I_{LX1} = 800mA	100	150	250	mΩ
Soft-Start Time	t_{r1}	V_{OUT1} ≥ 0.9 x V_{Target}, I_{OUT} = 0mA	0.8	1.1	1.5	ms
Discharge Resistance		V_{IN} = 5V, V_{OUT} = 3.3V	870	970	1070	Ω
Load Switch (LSW)						
Supply Voltage	V_{swi}		2.7	--	5.5	V
MOSFET On-Resistance	R_{DS_ON}	SWI = 3.3V, I_{OUT} = 500mA	60	85	120	mΩ
Current Limit	CLSW	T_A = 25℃	750 – 15%	750	750 + 15%	mA
	CLSW_T	–40℃ ≤ T_A ≤ 125℃	750 – 20%	750	750 + 20%	
Under-Voltage Threshold	UVP_sw	V_{SWI} – V_{SWO}	0.5	0.7	0.9	V
Soft-Start Time	t_{r_sw}	V_{OUT} ≥ 0.9 x V_{Target}, I_{OUT} = 0mA	0.9	1.3	1.8	ms
Discharge Resistance		V_{OUT1} = 3.3V, SWO = 3.3V	400	440	480	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Buck2 to Buck3						
Input Voltage Range	PVD2/PVD3		2.7	--	5.5	V
Output Voltage Range	V_{OUT}		1	--	3.6	V
Feedback Voltage Accuracy	FB2/3		0.8 – 3%	0.8	0.8 + 3%	V
Efficiency Peak	E_{ff}	V_{OUT} = 1.8V, V_{IN} = 3.3V, I_{LOAD} = 300mA Refer to Typical Operating Characteristics	--	92	--	%
Suggest Inductor	L_{Buck}	Refer to Typical Application Circuit	--	2.2	--	µH
Current Limit	CL2/3	T_A = 25℃	1300 – 15%	1300	1300 + 15%	mA
	CL2/3_T	–40℃ ≤ T_A ≤ 125℃	1300 – 25%	1300	1300 + 25%	
FB2/3 Under-Voltage Protection	UVP2/3	FB2/3 = FB2/3 x 0.5 (50%)	--	0.4	--	V
Load Regulation		T_A = 25℃, PVD2/3 = 3.3V, V_{OUT} = 1.2V, Load = 0mA to 1000mA Refer to Typical Operating Characteristics	–1	--	1	%
Line Regulation		T_A = 25℃, PVD2/3 = 3V to 5.5V, V_{OUT} = 1.2V, Load = 1000mA Refer to Typical Operating Characteristics	–1	--	1	%
P-MOSFET On-Resistance	$R_{DS\_ON\_P}$	PVD2/3 = 3.3V	180	270	370	mΩ
N-MOSFET On-Resistance	$R_{DS\_ON\_N}$	PVD2/3 = 3.3V	100	175	250	mΩ
Soft-Start Time	$t_{r2/3}$	$V_{OUT2/3}$ ≥ 0.9 x V_{Target}, I_{OUT} = 0mA	0.8	1	1.5	ms
Discharge Resistance		PVD2 = 3.3V, V_{OUT} = 1.2V	5	6	7	Ω
		PVD3 = 3.3V, V_{OUT} = 1.8V	6	7	8	
CH4 LDO						
Input Voltage for PVD4	PVD4		2.7	--	5.5	V
Output Voltage Range	V_{OUT}		1	--	3.6	V
Feedback Voltage Accuracy	FB4		0.8 – 3%	0.8	0.8 + 3%	V
Current Limit	CL4	T_A = 25℃	750 – 15%	750	750 + 15%	mA
	CL4_T	–40℃ ≤ T_A ≤ 125℃	750 – 30%	750	750 + 35%	
Dropout Voltage (PVD4 – V_{OUT4})	V_{DROP}	I_{OUT} = 150mA, PVD4 = V_{OUT4} – 0.1V	0.01	--	0.15	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation		LiR	T_A = 25℃, PVD4 = 3V to 5V, V_{OUT4} = 2.7V, Load = 100mA Refer to Typical Operating Characteristics	–0.5	--	0.5	%
Load Regulation		LoR	T_A = 25℃,PVD4 = 3.3V, Load 10mA to 500mA Refer to Typical Operating Characteristics	0	0.1	1	%
FB4 Under-Voltage Protection		FB4_UVP	FB4 = 0.8V x 0.4 (40%)	0.2	0.3	0.4	V
PSRR			Feq = 1kHz, I_{OUT} = 10mA, V_{OUT} = 2.7V Refer to Typical Operating Characteristics	--	60	--	dB
Soft-Start Time		t_{r4}	$V_{OUT4} \geq 0.9 \times V_{Target}$, I_{OUT} = 0mA	0.6	1	1.5	ms
Discharge Resistance			PVD4 = 3.3V, V_{OUT} = 2.7V	380	450	520	Ω
Power Good							
Power Good Pull-Down Voltage		PGOOD	PGOOD current equal to 5mA	--	200	--	mV
Power Good Delay Time		t_{PGOOD}		--	5	--	ms
Control							
ENA Input Voltage	Logic-High			2	--	--	V
	Logic-Low			--	--	0.5	
ENA Pull High Current		I_{PULL}	V_{IN} = 5V, Temperature = –40°C to 125°C	20	37	55	µA

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. The junction temperature(T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in watts) according to the formula : $T_J = T_A + (P_D \times \theta_{JA})$ where θ_{JA} (in °C/W) in the package thermal impedance. Another, $P_{IN} – P_O = P_D$ and $P_O = \eta \times P_{IN} \rightarrow P_D = (1 / \eta – 1) \times P_O$ where P_{IN} is the total input power and Po is the total output power.

Note 4. Devices are ESD sensitive. Handling precaution is recommended.

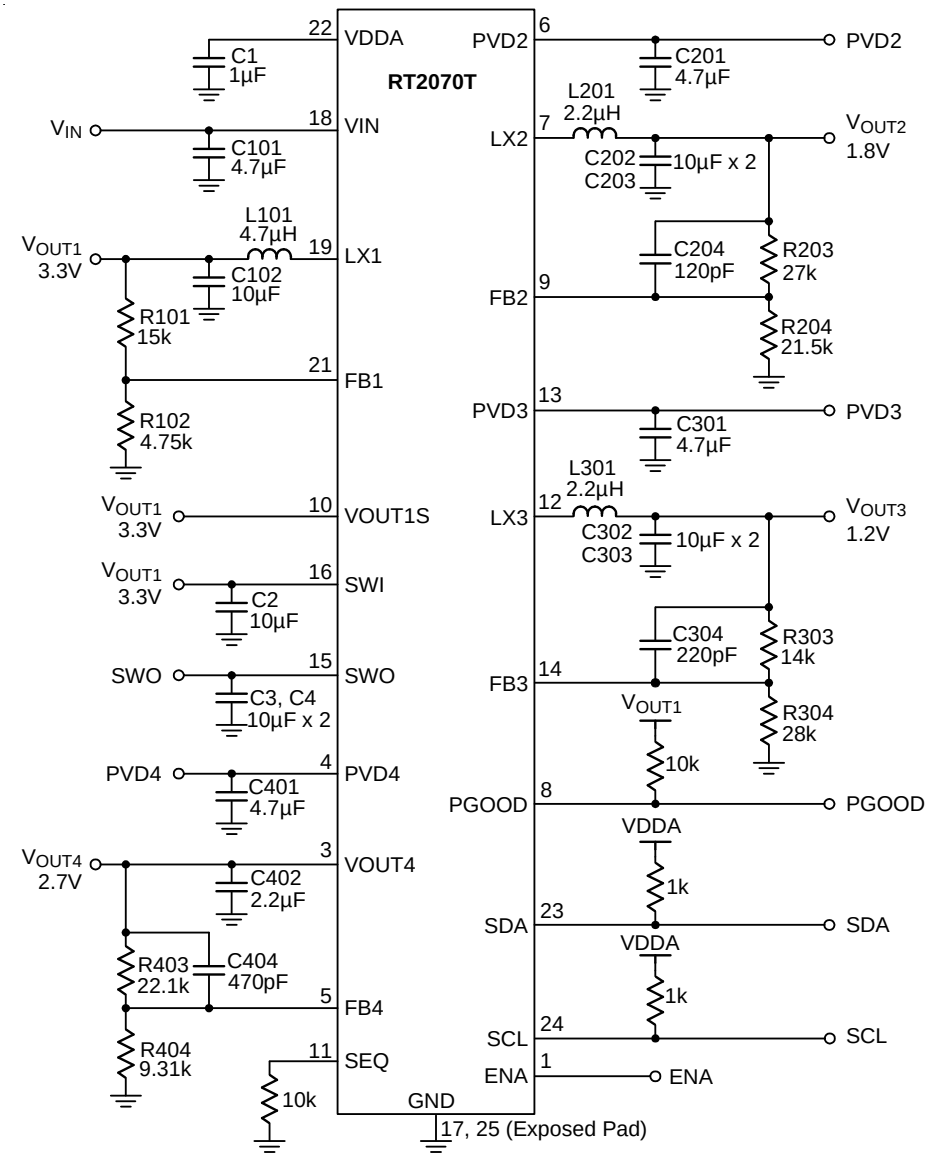
Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. When OTP is set to Hiccup by I^2C.

Note 7. When VIN OVP is set to Hiccup by I^2C

Note 8. Limits apply to the recommended V_{IN} = 4.5V to 15V, T_A = –40°C to 125°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.

Typical Application Circuit



If there is any CHx is not used that external components still must be existed and keep original application circuit.

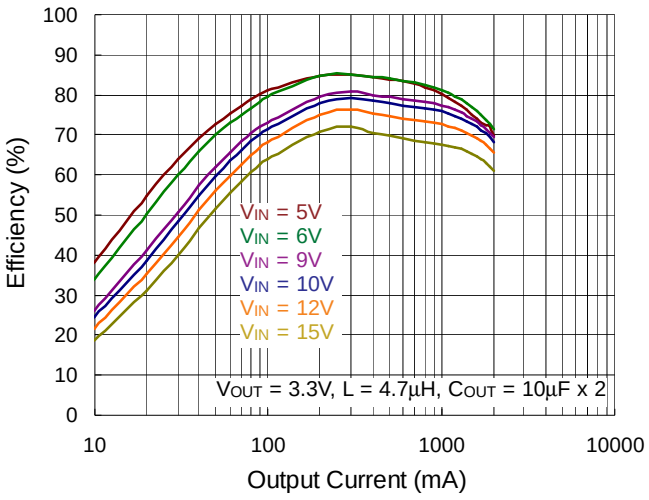
If LSW isn't used, user can remove C2, C3 and C4, but the SWI pin must connect to VOUT1 and floating the SWO pin.

Table 1. Suggested Components for Typical Application Circuit

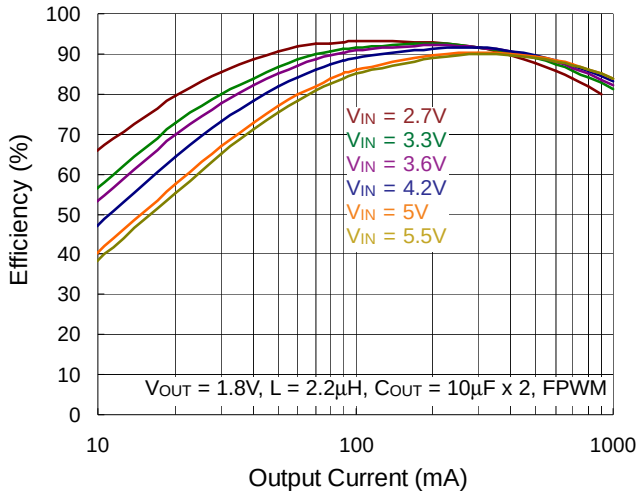
Reference	Q'ty	P/N	Description	Manufacturer
C1	1	GCM188R61A105KA37D	1µF/10V/X5R	MURATA
C2, C3, C4, C102, C202, C203, C302, C303	8	GCM21BR71A106KE22L	10µF/10V/X7R	MURATA
C101	1	GRM31CR71E475KA40	4.7µF/25V/X7S	MURATA
C201, C301, C401	3	GCM21BC71A475KA73L	4.7µF/10V/X7S	MURATA
C402	1	GCM21BR71A225KA01	2.2µF/10V/X7R	MURATA
C204	1	GCM1885C1H121JA16#	120pF/50V/C0G	MURATA
C304	1	GCM1885C1H221JA16D	220pF/50V/C0G	MURATA
C404	1	GCM1885C1H470JA16D	470pF/50V/C0G	MURATA
L101	1	LQH5BPB4R7NT0L	4.7µH	MURATA
L201, L301	2	LQH32PB2R2NN0L	2.2µH	MURATA
R101	1	RM06FTN1502	15k/1%	TA-I
R102	1	RM06FTN4751	4.75k/1%	TA-I
R203	1	RM06FTN2702	27k/1%	TA-I
R204	1	RM06FTN2152	21.5k/1%	TA-I
R303	1	RM06FTN1402	14k/1%	TA-I
R304	1	RM06FTN2802	28k/1%	TA-I
R403	1	RM06FTN2212	22.1k/1%	TA-I
R404	1	RM06FTN9311	9.31k/1%	TA-I

Typical Operating Characteristics

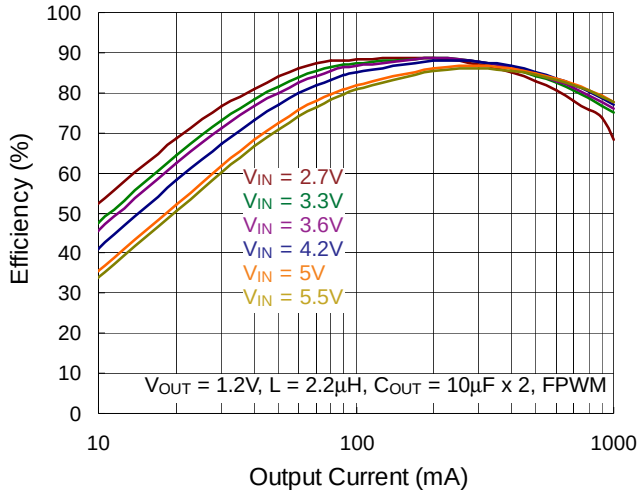
CH1 HV Buck Efficiency vs. Output Current



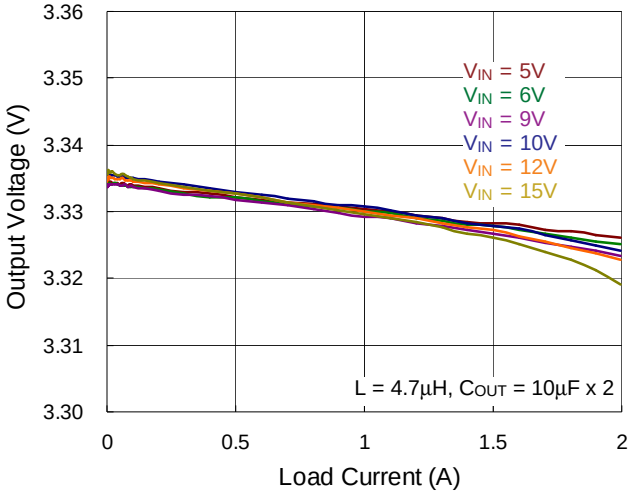
CH2 Buck Efficiency vs. Output Current



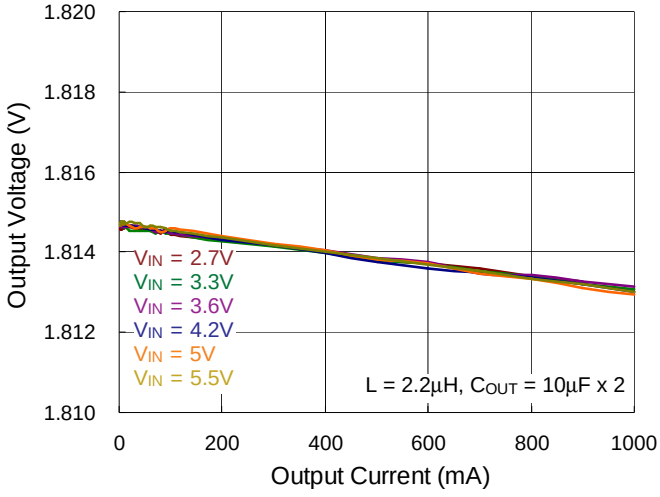
CH3 Buck Efficiency vs. Output Current



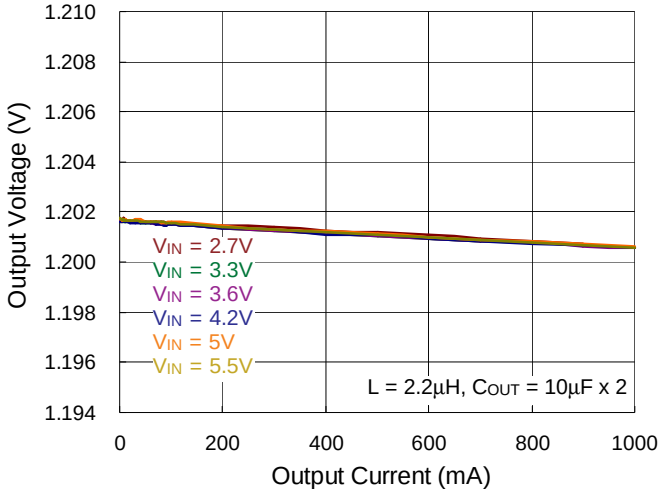
CH1 HV Buck Output Voltage vs. Output Current



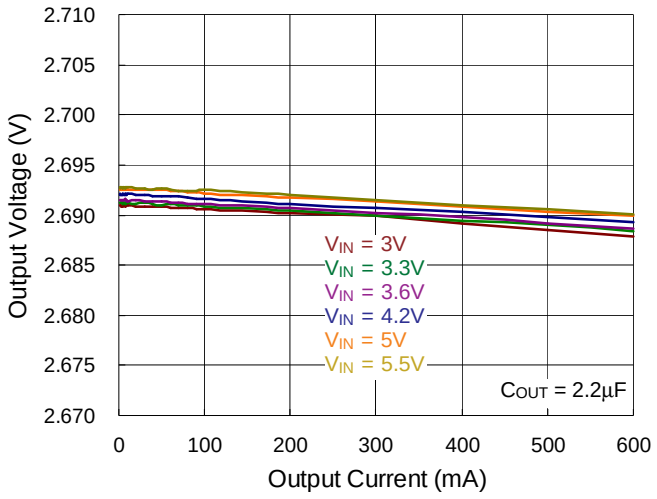
CH2 Buck Output Voltage vs. Output Current



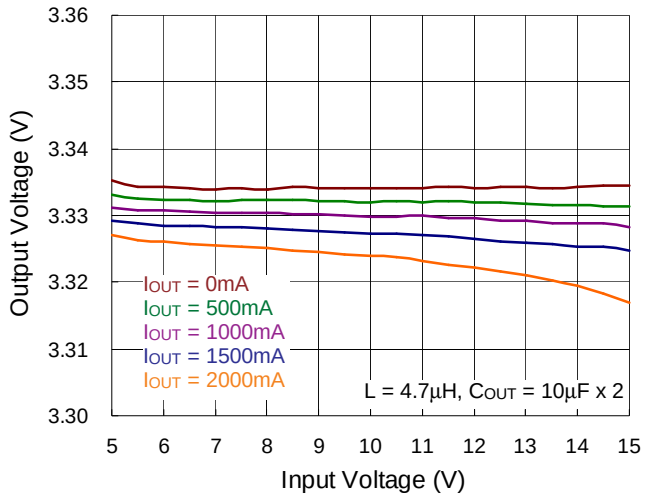
CH3 Buck Output Voltage vs. Output Current



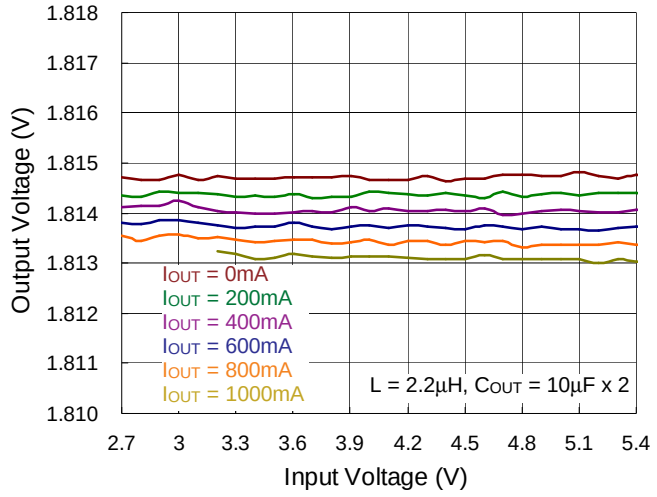
CH4 LDO Output Voltage vs. Output Current



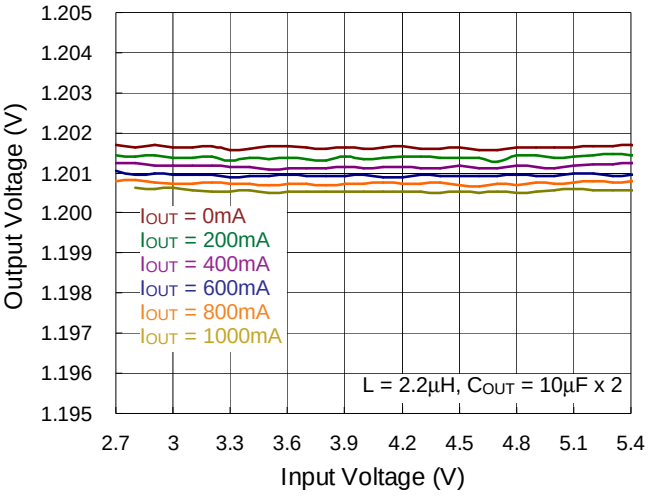
CH1 HV Buck Output Voltage vs. Input Voltage



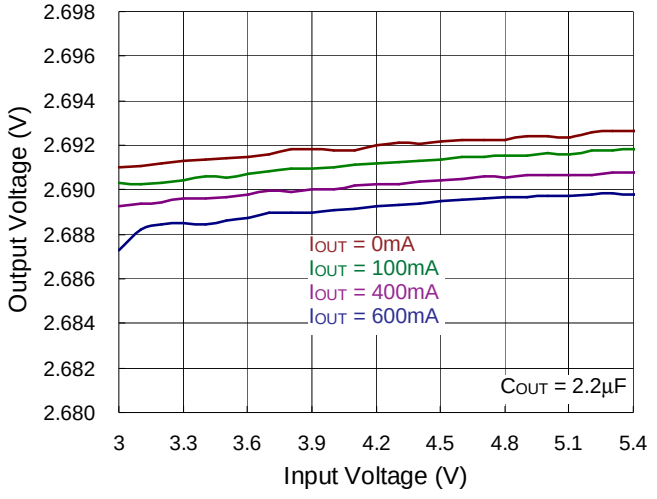
CH2 Buck Output Voltage vs. Input Voltage



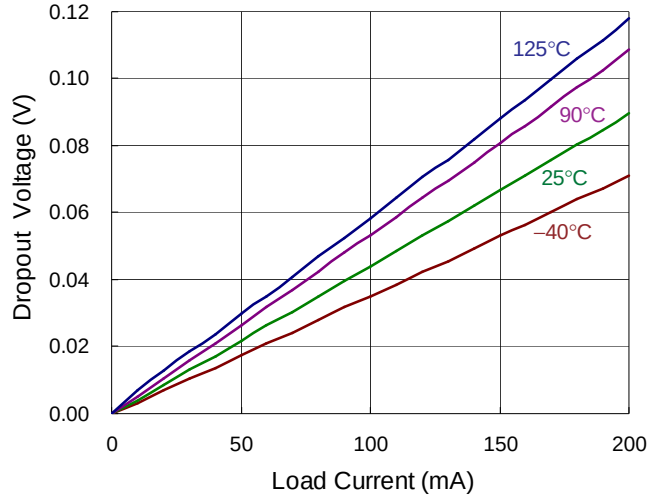
CH3 Buck Output Voltage vs. Input Voltage

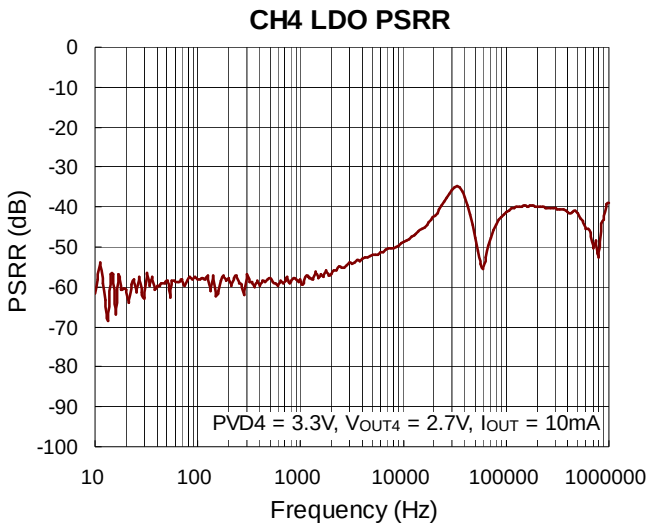


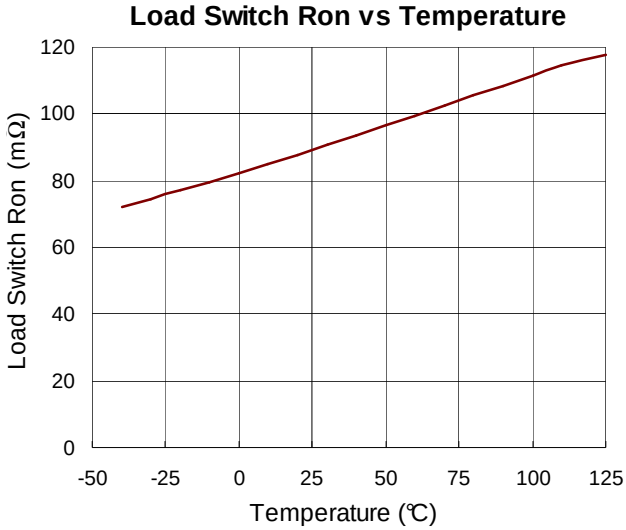
CH4 LDO Output Voltage vs. Input Voltage

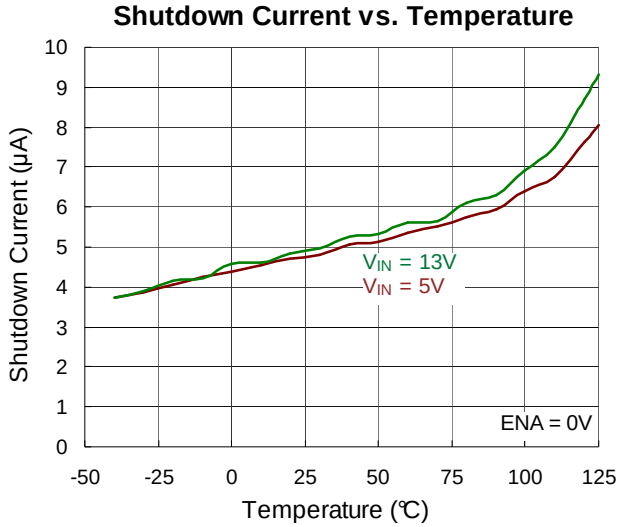


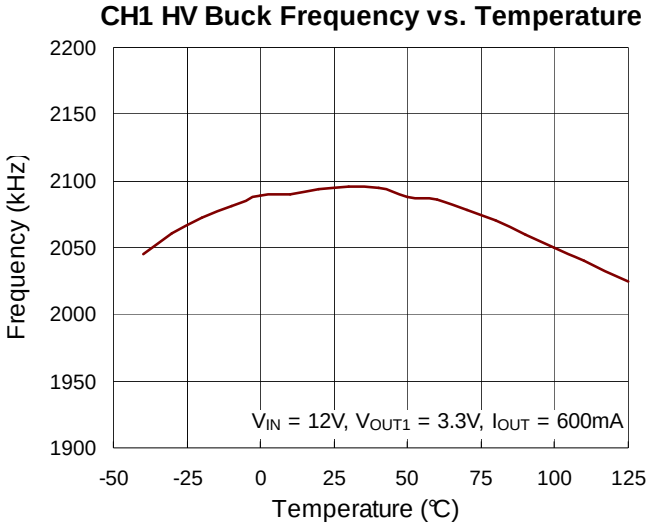
CH4 LDO Dropout Voltage vs. Load Current











Applications Information

The RT2070T is a highly integrated automotive system Power Management IC that contains 3-CH switching DC-DC converters and one generic LDO and one load switch.

CH1 : HV Step-Down DC-DC Converter

CH1 is a HV step-down converter for LV DC-DC converter power. The current-mode PWM converter with integrated internal MOSFETs and compensation network operates at fixed frequency. The output voltage of CH1 is set by external feedback resistors, as expressed in the following equation :

$VOUT1 = (1 + R101 / R102) \times V_{FB1}$

Where V_{FB1} is 0.8V typically and suggested value for R101 is 10k to 500k.

CH2 : Synchronous Step-Down DC-DC Converter

CH2 is a synchronous step-down converter for I/F power and it operates with typically 2MHz fixed frequency Pulse Width Modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter Power Save Mode and operates in PFM mode which can be set by I^2C interface.

The converter output voltage is externally adjustable using a resistor divider at FB2.

The output voltage of CH2 is set by external feedback resistors, as expressed in the following equation :

$VOUT2 = (1 + R203 / R204) \times V_{FB2}$

Where V_{FB2} is 0.8V typically and suggested value for R203 is 10k to 600k.

CH3 : Synchronous Step-Down DC-DC Converter

CH3 is suitable for logic power. The converter with integrated internal MOSFETs and compensation network operates at synchronous PSM or fixed frequency PWM current mode which can be set by the I^2C interface. The output voltage of CH3 is set by external feedback resistors, as expressed in the following equation :

$VOUT3 = (1 + R303 / R304) \times V_{FB3}$

Where V_{FB3} is 0.8V typically and suggested value for R303 is 10k to 600k.

For CH2 and CH3, to improve control performance using a feedforward capacitor in parallel to R203 or R303 is recommended, the value for the feedforward capacitor can be calculated using below formula :

$$\text{For CH2, } C_{FF} = \frac{3.16\mu s}{R203}$$

$$\text{For CH3, } C_{FF} = \frac{3.16\mu s}{R303}$$

CH4 : Generic LDO

CH4 is a low-dropout (LDO) voltage regulator which offers benefits of high input voltage and low-dropout voltage for sensor power. The output voltage of CH4 is set by external feedback resistors, as expressed in the following equation :

$VOUT4 = (1 + R403 / R404) \times V_{FB4}$

Where V_{FB4} is 0.8V typically and suggested value for R403 is 5k to 500k.

To improve control performance using a feedforward capacitor in parallel to R403 is recommended, the value for the feedforward capacitor can be calculated using below formula :

$$C_{FF} = \frac{10.4\mu s}{R403}$$

Load Switch : Load Switch

The load switch for core power is equipped with soft-start control and current limit function.

If LSW isn't used, user can remove C2, C3 and C4, but the SWI pin must connect to VOUT1 and floating the SWO pin.

Input and Output Capacitors Selection

The RT2070T is designed to work with low ESR ceramic capacitors. The *effective* value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have a large voltage coefficient, in addition to normal tolerances and temperature coefficients. Under D.C. bias, the capacitance value drops considerably. Larger case sizes or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum effective capacitance up to the desired value.

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. A low ESR input capacitor with larger ripple current rating should be used for the maximum RMS current. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to either further derate the capacitor or choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design. The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple, load step transients, and the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be examined by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 f C_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since DIL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Suggestion ESR Range of output capacitor

Application	C_{OUT} ESR Range
CH1 C_{OUT}	5 to 15mΩ
CH2 C_{OUT}	5 to 15mΩ
CH3 C_{OUT}	5 to 15mΩ
CH4 C_{OUT}	5 to 10mΩ

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part. Table 1 shows the nominal values of input/output capacitance recommenced for the RT2070T.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance :

$$\Delta I_L = \left[\frac{V_{OUT}}{f_{OSC} \times L} \right] \times \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4 (I_{MAX})$. The largest ripple current occurs at the

highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f_{OSC} \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or permalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. However, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation.

Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded.

This results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depend on the price vs. size requirements and any radiated field/EMI requirements.

Power On/Off Control

The register value will be recovered to default value as VIN plug in. In normal operation, users can set the power on/off relative setting by I^2C for next ENA power on. The RT2070T support 6 sets power on/off sequence selected by the SEQ pin. The sequence detection operation only work as VIN plug in. The RT2070T includes 6 sets power on/off sequence and the default value is decided by factory trim.

In the RT2070T, users can plan the next power on/off sequence by setting register A01/A02. The register value means the power on location, and "000" means this channel is power off. The RT2070T doesn't allow missing power on code or discrete code occurs.

SEQ0 to SEQ5			
	Output Voltage Setting	**Soft-Start End Delay Time (A01.Bit [7:6])**	**Discharge Finish Delay Time (A02.Bit [7:6])**
LSW	SEQX_LSW [2:0]	[00]	[00]
	[001]		
Buck2	SEQX_Buk2 [2:0]		
	[010]		
Buck3	SEQX_Buk3 [2:0]		
	[011]		
LDO4	SEQX_LDO [2:0]		
	[100]		

Note :

The default value will be decided in factory trim.

Define :

[000] means channel always turn off.

[001] means firstly turn on channel.

---

[100] means the finally turn on channel.

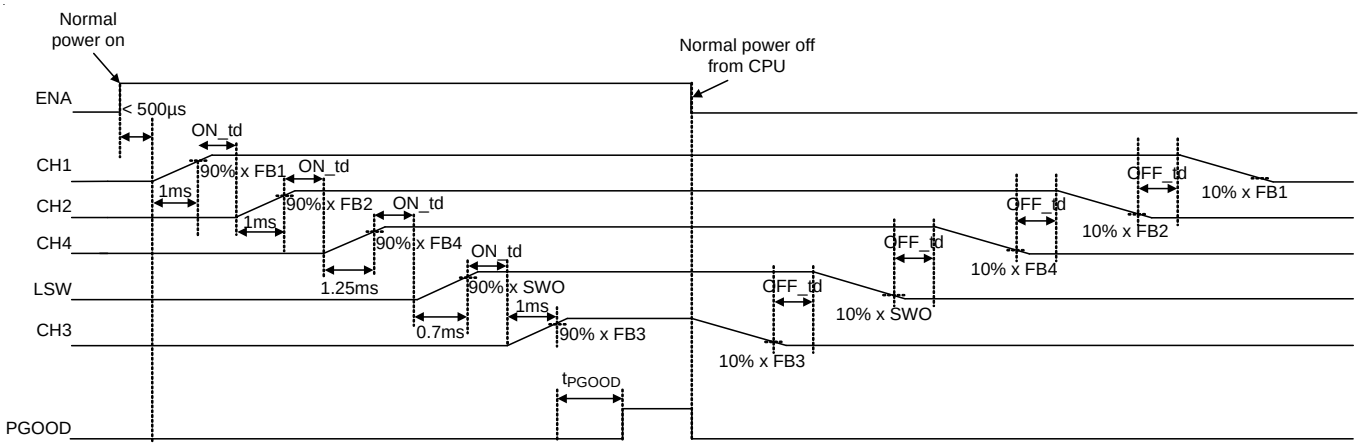
Example :

In above setting, the power on sequence is as below :

LSW (001) → Buck2 (010) → Buck3 (011) → LDO4 (100).

Normally Power ON/OFF Sequence

In the RT2070T, the power on sequence of the channels are decided by SEQ setting. The off sequence will follow first-on-last-off rule to turn off channels.



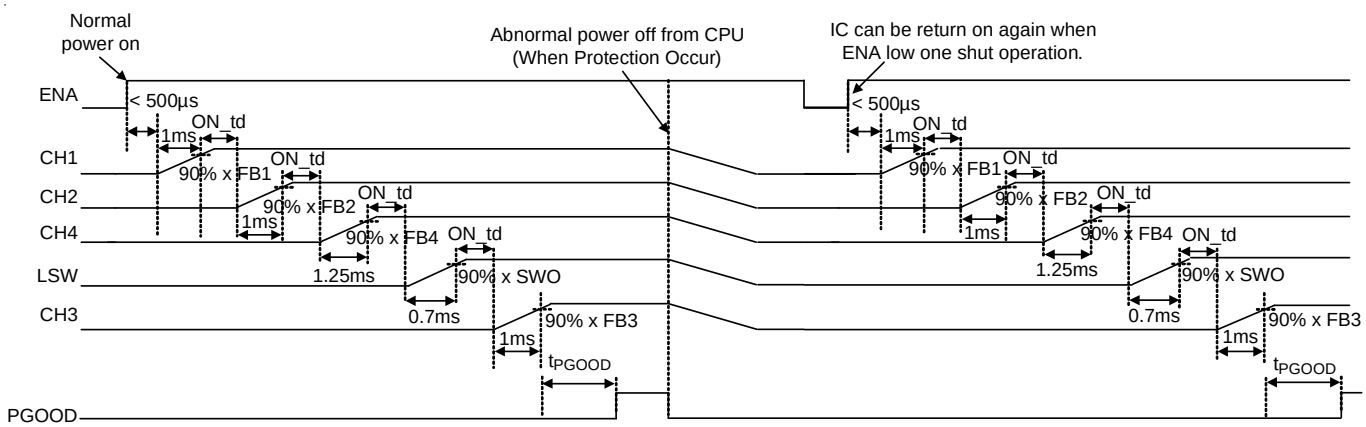
Note : ON_td and OFF_td time control by Register ON_td <1:0> and OFF_td <1:0>, default setting <00> = 0ms, and t_{PGOOD} = 5ms.

Figure 1. Sequence Example : CH1 → CH2 → CH4 → LSW → CH3

Abnormal Off

When the abnormal event occurs, all channels turns off immediately.

If users want to turn on again, users must pull ENA low to reset state then pull high to turn on again.



Note : ON_td and OFF_td time control by Register ON_td <1:0> and OFF_td <1:0> , default setting <00> = 0ms, and t_{PGOOD} = 5ms.

Figure 2. Protection Example : Each Channel Shutdown at the Same Time

When output channel take time to discharge over 64ms and ENA keep low level, all channels turn off at 64ms after starting Power Off Sequence.

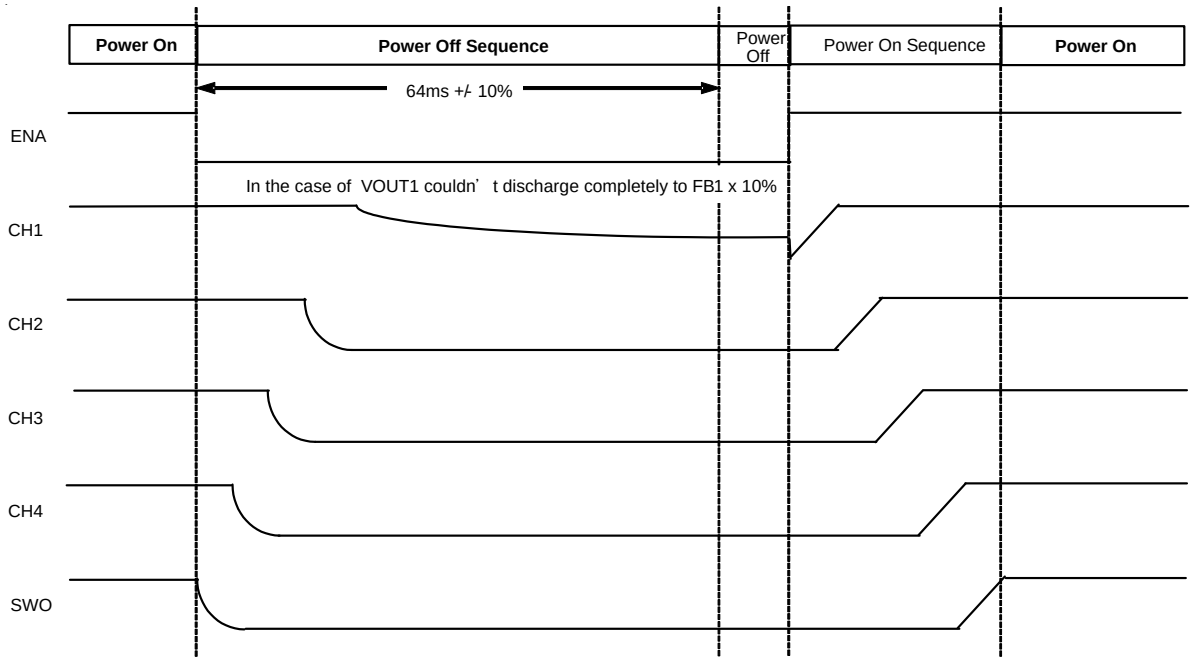


Figure 3. Sequence Example : Power ON (CH1→ CH2→ CH3→ CH4→ LSW), Power OFF (LSW→CH4→CH3→CH2→CH1)

When output channel take time to discharge over 64ms and ENA goes high level at 64ms after starting Power Off Sequence, the RT2070T re-start immediately.

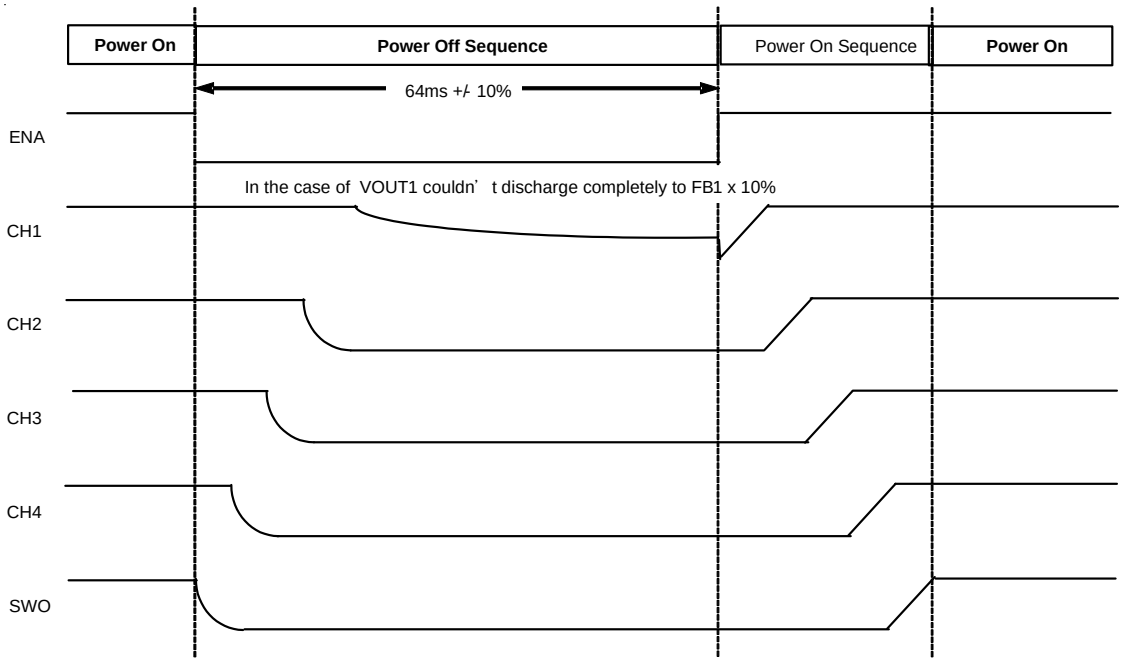


Figure 4. Sequence Example : Power ON (CH1→ CH2→ CH3→ CH4→ LSW), Power OFF (LSW →CH4 →CH3 →CH2 →CH1)

When output channel take time to discharge over 64ms and ENA keep high level at 64ms after starting Power Off Sequence, the RT2070T re-start immediately.

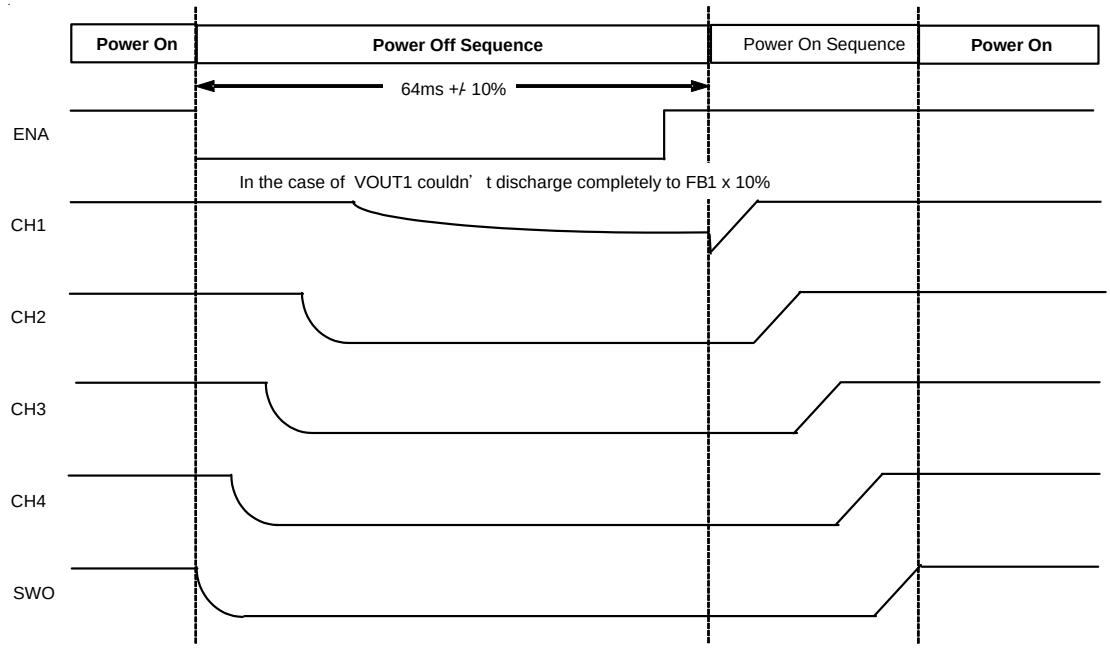
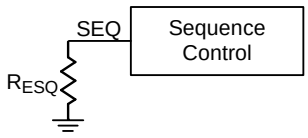


Figure 5. Sequence Example : Power ON (CH1→ CH2→ CH3→ CH4→ LSW), Power OFF (LSW →CH4 →CH3 →CH2 →CH1)

PMU On/Off Sequence Setting by SEQ

The SEQ pull-down resistance is used to define power on/off sequence (SEQ1 to SEQ5).

The RT2070T will do sequence detection as VIN plug in. Enable sequence will be executed when detection phase finish. If users don't change the sequence setting by I^2C in register A01 to A12, the IC will follow default value to turn on IC set by factory trim. If there is any CHx is not used that external components still must be existed and keep original application circuit.



SEQ	RSEQ Range	Typical R_{SEQ}
SEQ0	Short to VDDA	
SEQ1	64kΩ > R_{SEQ} > 30kΩ	47kΩ
SEQ2	16kΩ > R_{SEQ} > 6.8kΩ	10kΩ
SEQ3	3.9kΩ > R_{SEQ} > 1.6kΩ	2.4kΩ
SEQ4	Short to GND	
SEQ5	200kΩ > R_{SEQ} > 110kΩ	160kΩ

Users can plan the combination of six sequences (SEQ0 to SEQ5).

SEQ0	CH1	CH2	LSW	CH3	CH4
SEQ1	CH1	LSW	CH4	CH3	CH2
SEQ2	CH1	CH4	CH3	CH2	LSW
SEQ3	CH1	CH2	CH3	LSW	CH4
SEQ4	CH2	CH1	CH3	CH4	LSW
SEQ5	CH1	LSW	CH2	CH4	CH3

VIN UVLO2 Operation

If VIN is smaller than 3.9V, all channels will be turned off after 32μs.

Next, V_{IN} is larger than 4.4V, the system will be sequence turn on by setting.

Max Load of Every Channel

Purpose	RT2070T	Peak Current Limit	Max Loading (I_{OUT})*	Condition ($V_{IN} \rightarrow V_{OUT}$)
HV to LV	CH1_HV Buck	3000mA	2000mA	5V → 3.3V
$V_{I/O}$	CH2_LV Buck	1300mA	900mA	3.3V → 1.8V
V_{CORE}	CH3_LV Buck	1300mA	1000mA	3.3V → 1.2V
V_{SENSOR}	CH4_LDO	750mA	500mA	3.3V → 2.7V
Load SW	LSW	750mA	500mA	3.3V → 3.3V

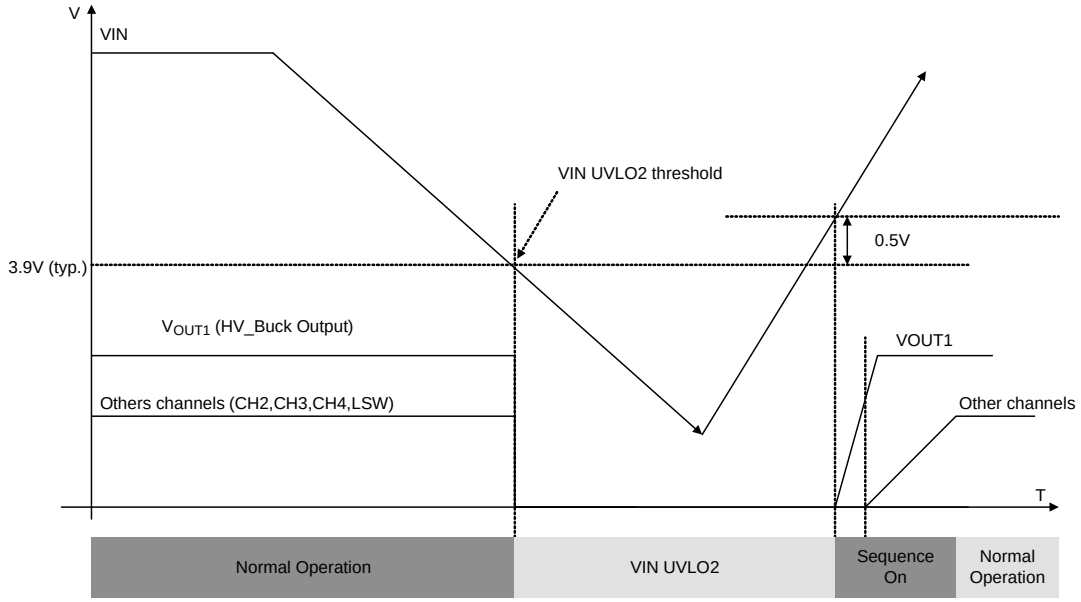
* Buck converter V_{IN}/V_{OUT} levels will affect the max loading

Higher max loading current

Higher step-down ratio (V_{IN}/V_{OUT}) results in shorter switch on-time (t_{ON}), hence lower peak switch current.

Lower max loading current

Lower step down ratio (V_{IN} closer to V_{OUT}) results a lower differential inductor voltage, so the slope of the inductor current during the ramp-up period is reduced.



Note : 0.5V is hysteresis voltage.

Figure 6. UVLO2 Diagram

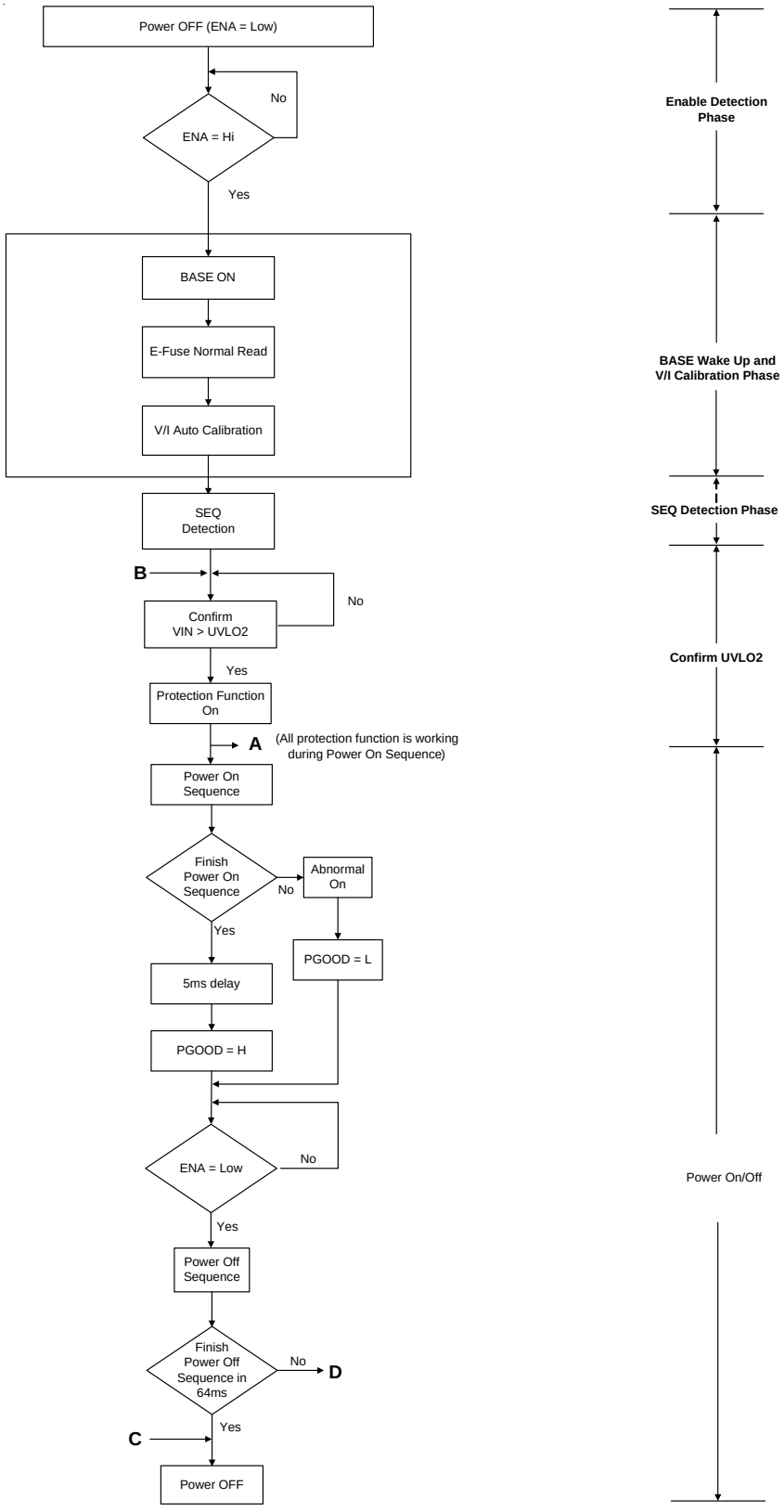
Protection Act

	UVLO2
Protection Action	Hiccup
Vth_R(V)	4.4
Vth_F(V)	3.9
Power On Confirm	YES
Detect Power Pin	VIN

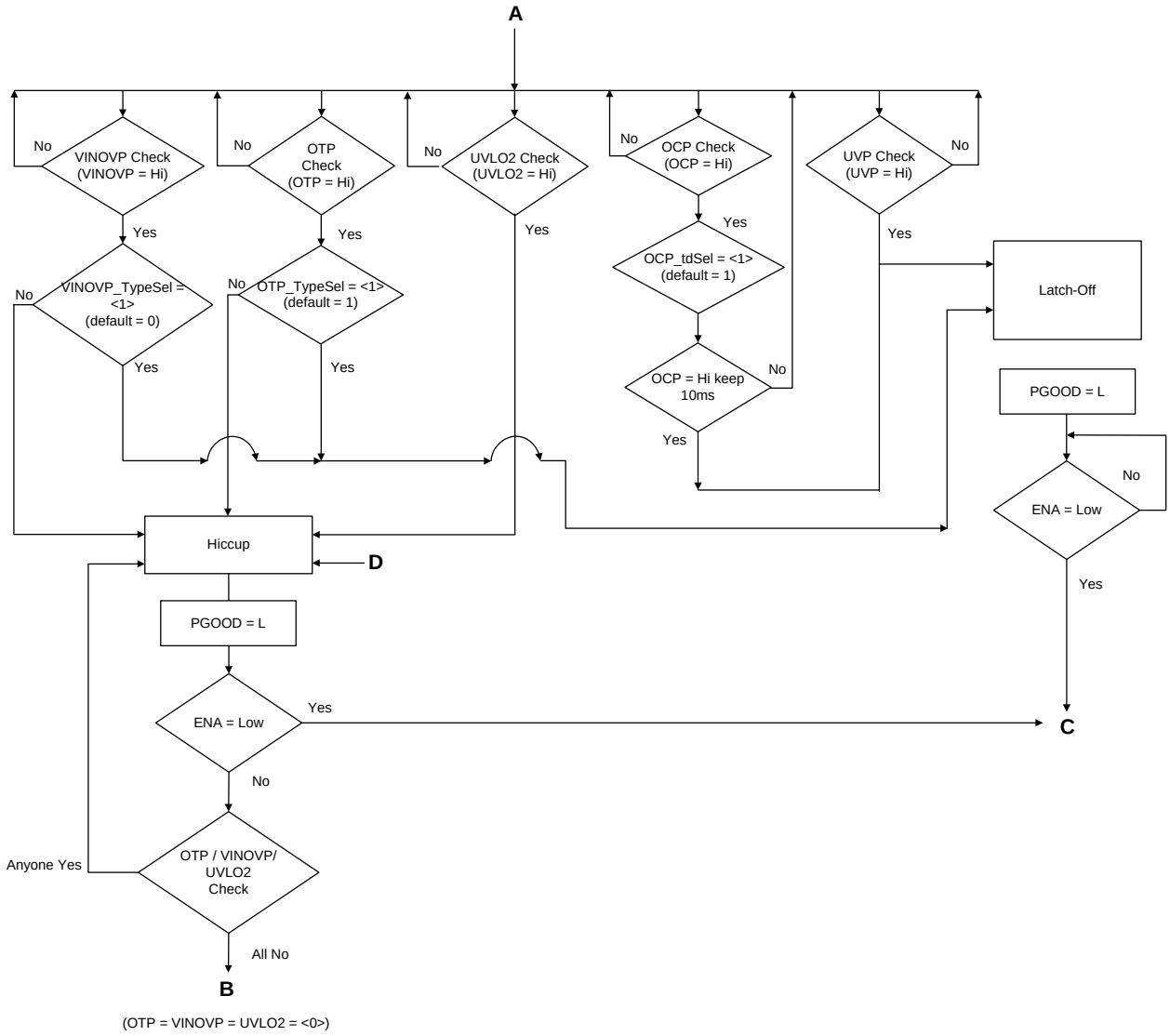
*Hiccup : Recover automatically.

Flow Chart

Power ON/OFF Operation

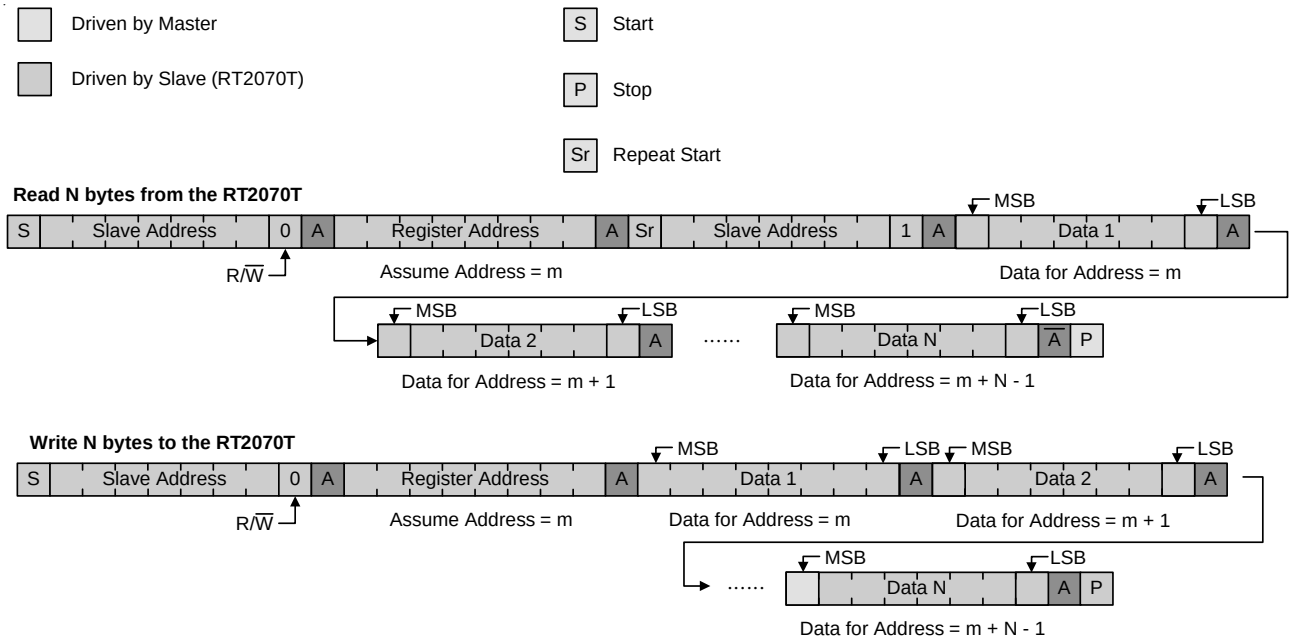


Flow Chart of Protection



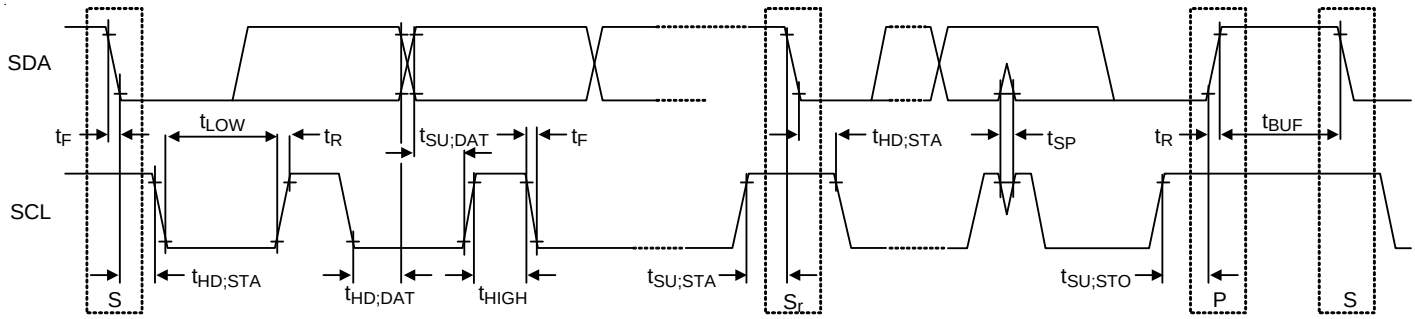
I²C Interface

The RT2070T I²C interface bus power must be supplied by VDDA or equal potential node. If I²C interface isn't used, SDA and SCL must be connected to GND. The RT2070T I²C slave address = 0110100 (7bits). I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :



Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C Interface Electrical Characteristics						
Pull Up Voltage Range			1.8	--	VDDA	V
SCLK Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated	$t_{HD;STA}$		0.6	--	--	µs
LOW Period of the SCL Clock	t_{LOW}		1.3	--	--	µs
HIGH Period of the SCL Clock	t_{HIGH}		0.6	--	--	µs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	µs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	µs
Data Set-Up Time	$t_{SU;DAT}$		100	--	--	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	--	--	µs
Rise Time of Both SDA and SCL Signals	t_R		20	--	300	ns
Fall Time of Both SDA and SCL Signals	t_F		20	--	300	ns
SDA and SCL Output Low Sink Current	I_{OL}	SDA or SCL voltage = 0.4V	2	--	--	mA

I²C Waveform Information



I²C Register Table

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A00	0x00	Function	Buck Function Trim							
		Meaning	Reserved	FPWM3	FPWM2	EnDis_ LDO	EnDis_ buck3	EnDis_ buck2	Reserved	Reserved
		Default	0	1	1	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
FPWM3			Define the Buck3 switching operation mode							
			0 : Automatic PWM/PSM switching operation 1 : Force PWM							
FPWM2			Define the Buck2 switching operation mode							
			0 : Automatic PWM/PSM switching operation 1 : Force PWM							
EnDis_LDO			LDO power off discharge enable control							
			0 : Won't discharge when LDO power off 1 : Discharge when LDO power off							
EnDis_buck3			Buck3 power off discharge enable control							
			0 : Won't discharge when Buck3 power off 1 : Discharge when Buck3 power off							
EnDis_buck2			Buck2 power off discharge enable control							
			0 : Won't discharge when Buck2 power off 1 : Discharge when Buck2 power off							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A01	0x01	Function	SEQ0 Trim							
		Meaning	ON_td <1:0>		SEQ0_Buk2 <2:0>			SEQ0_LSW <2:0>		
		Default	0	0	0	0	1	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ON_td <1:0>			Define the interval between soft-start finish and the next channel enabled							
			11 : 2ms 10 : 1ms 01 : 0.5ms 00 : 0ms							
SEQ0_Buck2 <2:0>			Define Buck2 power on sequence in SEQ0 (Note : every channel can't choose the same code except <000> in SEQ0)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ0_LSW <2:0>			Define LSW power on sequence in SEQ0 (Note : every channel can't choose the same code except <000> in SEQ0)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A02	0x02	Function	SEQ0 Trim							
		Meaning	OFF_td <1:0>		SEQ0_LDO <2:0>			SEQ0_Buk3 <2:0>		
		Default	0	0	1	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OFF_td <1:0>			Define the interval between shut-down OK and the next channel disabled							
			11 : 2ms 10 : 1ms 01 : 0.5ms 00 : 0ms							
SEQ0_Buck3 <2:0>			Define Buck3 power on sequence in SEQ0 (Note : every channel can't choose the same code except <000> in SEQ0)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ0_LDO <2:0>			Define LDO power on sequence in SEQ0 (Note : every channel can't choose the same code except <000> in SEQ0)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A03	0x03	Function	SEQ1 Trim							
		Meaning	Reserved	Reserved	SEQ1_Buk2 <2:0>			SEQ1_LSW <2:0>		
		Default	0	0	1	0	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ1_Buck2 <2:0>			Define Buck2 power on sequence in SEQ1 (Note : every channel can't choose the same code except <000> in SEQ1)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ1_LSW <2:0>			Define LSW power on sequence in SEQ1 (Note : every channel can't choose the same code except <000> in SEQ1)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A04	0x04	Function	SEQ1 Trim							
		Meaning	Reserved	Reserved	SEQ1_LDO <2:0>			SEQ1_Buk3 <2:0>		
		Default	1	0	0	1	0	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ1_LDO <2:0>			Define LDO power on sequence in SEQ1 (Note : every channel can't choose the same code except <000> in SEQ1)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ1_Buck3 <2:0>			Define Buck3 power on sequence in SEQ1 (Note : every channel can't choose the same code except <000> in SEQ1)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A05	0x05	Function	SEQ2 Trim							
		Meaning	Reserved	Reserved	SEQ2_Buk2 <2:0>			SEQ2_LSW <2:0>		
		Default	0	0	0	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ2_Buck2 <2:0>			Define Buck2 power on sequence in SEQ2 (Note : every channel can't choose the same code except <000> in SEQ2)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ2_LSW <2:0>			Define LSW power on sequence in SEQ2 (Note : every channel can't choose the same code except <000> in SEQ2)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A06	0x06	Function	SEQ2 Trim							
		Meaning	Reserved	Reserved	SEQ2_LDO <2:0>			SEQ2_Buk3 <2:0>		
		Default	0	0	0	0	1	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ2_LDO <2:0>			Define LDO power on sequence in SEQ2 (Note : every channel can't choose the same code except <000> in SEQ2)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ2_Buck3 <2:0>			Define Buck3 power on sequence in SEQ2 (Note : every channel can't choose the same code except <000> in SEQ2)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A07	0x07	Function	SEQ3 Trim							
		Meaning	Reserved	Reserved	SEQ3_Buk2 <2:0>			SEQ3_LSW <2:0>		
		Default	0	0	0	0	1	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ3_Buck2 <2:0>			Define Buck2 power on sequence in SEQ3 (Note : every channel can't choose the same code except <000> in SEQ3)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ3_LSW <2:0>			Define LSW power on sequence in SEQ3 (Note : every channel can't choose the same code except <000> in SEQ3)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A08	0x08	Function	SEQ3 Trim							
		Meaning	Reserved	Reserved	SEQ3_LDO <2:0>			SEQ3_Buk3 <2:0>		
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ3_LDO <2:0>			Define LDO power on sequence in SEQ3 (Note : every channel can't choose the same code except <000> in SEQ3)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ3_Buck3 <2:0>			Define Buck3 power on sequence in SEQ3 (Note : every channel can't choose the same code except <000> in SEQ3)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A09	0x09	Function	SEQ4 Trim							
		Meaning	Reserved	Reserved	SEQ4_Buk2 <2:0>			SEQ4_LSW <2:0>		
		Default	0	0	0	0	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ4_Buck2 <2:0>			Define Buck2 power on sequence in SEQ4 (Note : every channel can't choose the same code except <000> in SEQ4)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ4_LSW <2:0>			Define LSW power on sequence in SEQ4 (Note : every channel can't choose the same code except <000> in SEQ4)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A10	0x0A	Function	SEQ4 Trim							
		Meaning	Reserved	Reserved	SEQ4_LDO <2:0>			SEQ4_Buk3 <2:0>		
		Default	0	0	0	1	1	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ4_LDO <2:0>			Define LDO power on sequence in SEQ4 (Note : every channel can't choose the same code except <000> in SEQ4)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ4_Buck3 <2:0>			Define Buck3 power on sequence in SEQ4 (Note : every channel can't choose the same code except <000> in SEQ4)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A11	0x0B	Function	SEQ5 Trim							
		Meaning	Reserved	Reserved	SEQ5_Buk2 <2:0>			SEQ5_LSW <2:0>		
		Default	0	0	0	1	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ5_Buck2 <2:0>			Define Buck2 power on sequence in SEQ5 (Note : every channel can't choose the same code except <000> in SEQ5)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							
SEQ5_LSW <2:0>			Define LSW power on sequence in SEQ5 (Note : every channel can't choose the same code except <000> in SEQ5)							
			100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable							

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A12	0x0C	Function	SEQ5 Trim							
		Meaning	Reserved	Reserved	SEQ5_LDO <2:0>			SEQ5_Buk3 <2:0>		
		Default	0	0	0	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SEQ5_LDO <2:0>	Define LDO power on sequence in SEQ5 (Note : every channel can't choose the same code except <000> in SEQ5)
	100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable
SEQ5_Buck3 <2:0>	Define Buck3 power on sequence in SEQ5 (Note : every channel can't choose the same code except <000> in SEQ5)
	100 : the last turn on 011 : the third turn on 010 : the second turn on 001 : the first turn on 000 : disable

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A13	0x0D	Function	OTP/OVP Function Level Trim							
		Meaning	OTP_ TypeSel	Reserved	Reserved	Reserved	Reserved	VINOVP_ TypeSel	VINOVP_ TDSEL <1:0>	
		Default	1	1	0	0	1	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OTP_TypeSel	Define OTP protection operation mode.
	0 : Hiccup protection 1 : Latch-off protection
VINOVP_TypeSel	Define OVP protection operation mode.
	0 : Hiccup protection 1 : Latch-off protection
VINOVP_TDSEL <1:0>	Define OVP deglitch time
	11 : 10ms 10 : 5ms 01 : 1ms 00 : 0ms

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A14	0x0E	Function	Buck2/3 Performance Trim							
		Meaning	Buck3MP_Cur <1:0>		Buck3Drv <1:0>		Buck2MP_Cur <1:0>		Buck2Drv <1:0>	
		Default	1	0	1	0	1	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Buck3MP_Cur <1:0>	Define the Buck3 minimum peak current level
	11 : Minimum Peak Current Level = 210mA 10 : Minimum Peak Current Level = 170mA 01 : Minimum Peak Current Level = 110mA 00 : Minimum Peak Current Level = 70mA
Buck3Drv <1:0>	Define Buck3 driver ability
	11 : stronger 10 : middle 01 : weaker 00 : weakest
Buck2MP_Cur <1:0>	Define the Buck2 minimum peak current level
	11 : Minimum Peak Current Level = 210mA 10 : Minimum Peak Current Level = 170mA 01 : Minimum Peak Current Level = 110mA 00 : Minimum Peak Current Level = 70mA
Buck2Drv <1:0>	Define Buck2 driver ability
	11 : stronger 10 : middle 01 : weaker 00 : weakest

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A15	0x0F	Function	HVBuck f_{SW} Selection / Error Information							
		Meaning	HVBuck_OSC <1:0>		Err_Base	Err_ HVBuck	Err_LSW	Err_ Buck2	Err_ Buck3	Err_LDO
		Default	1	1	0	0	0	0	0	0
		Read/Write	R/W	R/W	R	R	R	R	R	R

HVBuck_OSC <1:0>	Define HVBuck switching frequency
	11 : 2MHz 10 : 2MHz 01 : 1MHz 00 : 500kHz
Err_Base	Mark Base protection happen, reset when ENA = <0> and Hiccup recycle to power on sequence
	1 : Happen VINUVLO or VINOVP or OTP or sequence time too long 0 : Didn't happen VINUVLO, VINOVP, OTP and sequence time too long
Err_HVBuck	Mark HVBuck protection happen, reset when ENA = <0> and Hiccup recycle to power on sequence
	1 : Happen HVBuck UVP or OCP 0 : Didn't happen HVBuck UVP and OCP
Err_LSW	Mark LSW protection happen, reset when ENA = <0> and Hiccup recycle to power on sequence
	1 : Happen LSW UVP or OCP 0 : Didn't happen LSW UVP and OCP
Err_Buck2	Mark Buck2 protection happen, reset when ENA = <0> and Hiccup recycle to power on sequence
	1 : Happen Buck2 UVP or OCP 0 : Didn't happen Buck2 UVP and OCP
Err_Buck3	Mark Buck3 protection happen, reset when ENA = <0> and Hiccup recycle to power on sequence
	1 : Happen Buck3 UVP or OCP 0 : Didn't happen Buck3 UVP and OCP
Err_LDO	Mark LDO protection happen, reset when ENA = <0> and Hiccup recycle to power on sequence
	1 : Happen LDO UVP or OCP 0 : Didn't happen LDO UVP and OCP

Address Name	Register Address	Description	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A16	0x10	Function	Disable Normal Read / Reload Default Setting / Error Function Information							
		Meaning	DIS_NR	RELOAD	Reserved	Err_UVLO2	Err_OVP	Err_OTP	Err_UVP	Err_OCP
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R	R	R	R	R	R

DIS_NR	Disable normal read control
	1 : Didn't load normal read data while power on (ENA = Hi) again. Hold original register setting of sRG0x00 to sRG0x0E and sRG0x0F <7:6>. 0 : Enable normal read while power on (ENA = Hi), reset register sRG0x00 to sRG0x0E and sRG0x0F <7:6>
RELOAD	Reload default register setting control
	1 : Reload normal read result into register table and can't write register when RELOAD = <1> 0 : register can be wrote
Err_UVLO2	Mark UVLO2 protection happen, reset when ENA = <0> or hiccup recycle to power on sequence
	1 : Happen UVLO2 0 : Didn't happen UVLO2
Err_OVP	Mark VINOVP protection happen, reset when ENA = <0> or hiccup recycle to power on sequence
	1 : Happen VINOVP 0 : Didn't happen VINOVP
Err_OTP	Mark OTP protection happen, reset when ENA = <0> or hiccup recycle to power on sequence
	1 : Happen OTP 0 : Didn't happen OTP
Err_UVP	Mark UVP protection happen, reset when ENA = <0>
	1 : Happen UVP 0 : Didn't happen UVP
Err_OCP	Mark OCP protection happen, reset when ENA = <0>
	1 : Happen OCP 0 : Didn't happen OCP

Protections List

	Protection Type	Threshold (Typical Value)	Mask Time	Protection Method	Reset Method
VIN	UVLO2	VIN < 3.9V	32µs	Disable all channels	Hiccup protection, restart if VIN > 4.4V and EN = Hi
	OVP	VIN > 15.5V	5ms	Disable all channels	Hiccup protection, restart if VIN < 13.5V and EN = Hi
CH1	OCP	PMOS current > 3A	10ms	Cycle-by-Cycle detection then disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
	UVP	VOUT1 < VOUT1 x 0.5 (50%)	No mask	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
	VOUT1 OVP	VOUT1 > 5.5V	No mask	Disable CH1	Hiccup Until fail event to be solved
CH2	OCP	PMOS current > 1.3A	10ms	Cycle-by-Cycle detection then disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
	UVP	VOUT2 < VOUT2 x 0.5 (50%)	No mask	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
CH3	OCP	PMOS current > 1.3A	10ms	Cycle-by-Cycle detection then disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
	UVP	VOUT3 < VOUT3 x 0.5 (50%)	No mask	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
CH4	OCP	PMOS current > 0.75A	10ms*	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
	UVP	VOUT4 < VOUT4 x 0.4 (40%)	No mask	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
LSW	Current Limit	NMOS current > 0.75A	No mask	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
	UVP	VSWI - VSWO > 0.7V	No mask	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
		VSWO < 0.85V	No mask	Disable all channels	Latch-off protection, VDDA < 1.6V or EN = low
Thermal	Thermal Shutdown	Temperature > 160℃	No mask	Disable all channels	Latch-off protection, EN = High and Temperature < 140℃

* When current limit is working, VOUT4 drops and UVP trigger less than 10ms.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24L 4x4 package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 4.46W for a WQFN-24L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

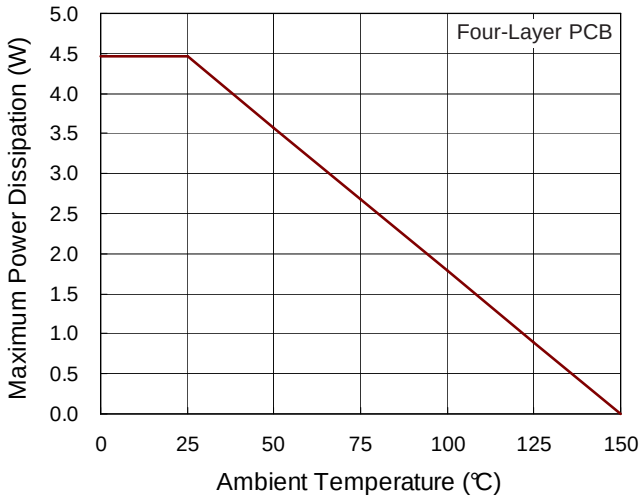


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT2070T, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FBx pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

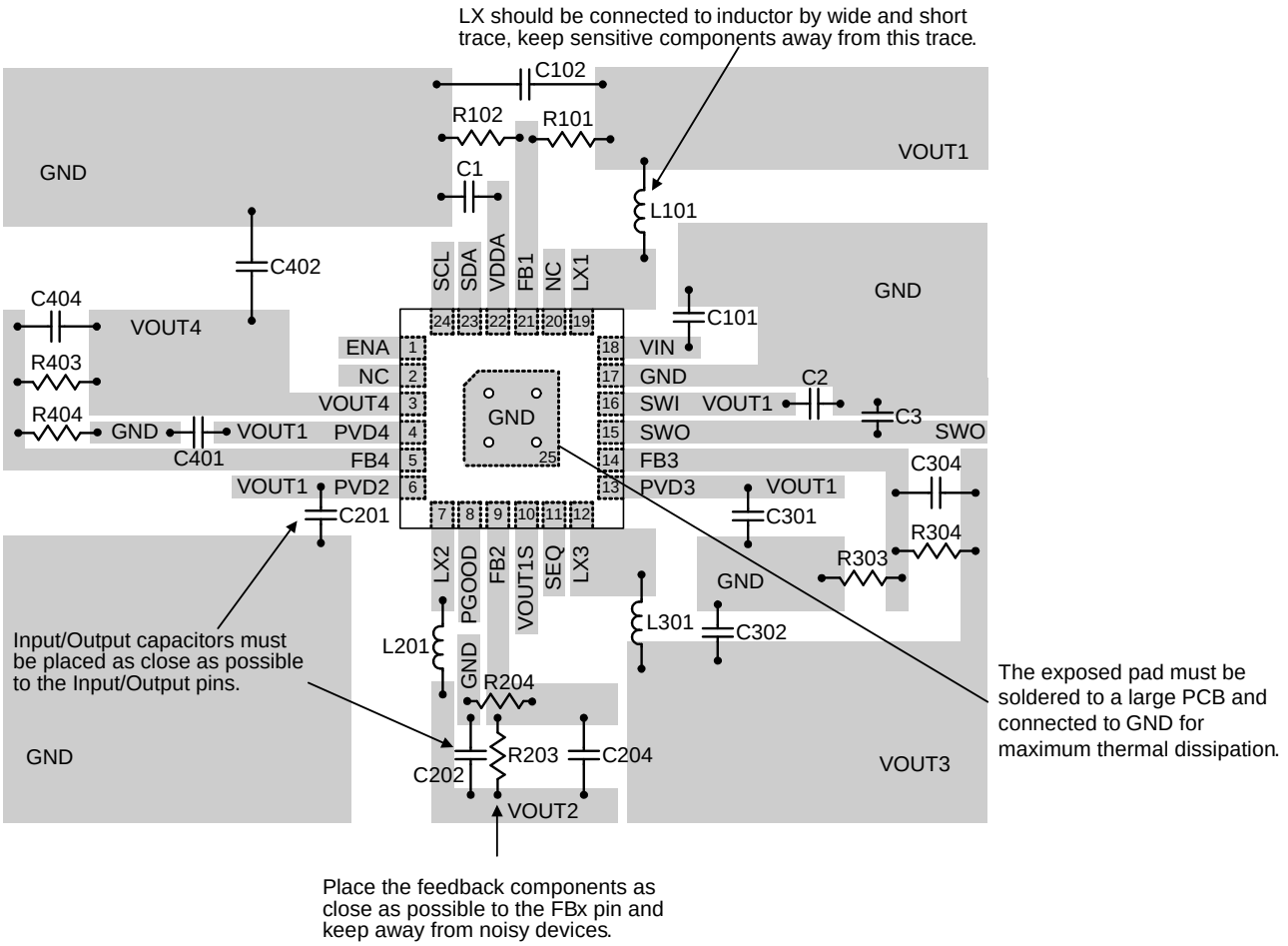
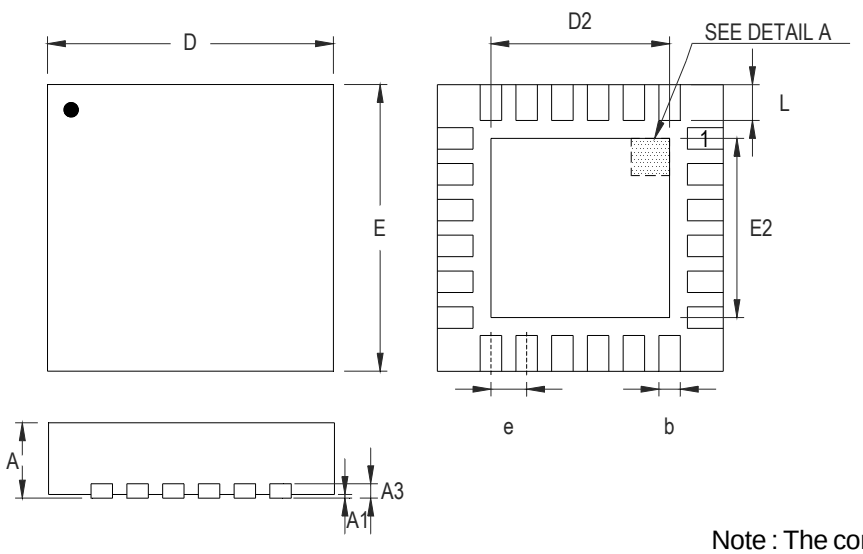
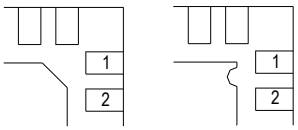


Figure 8. PCB Layout Guide

Outline Dimension





DETAIL A

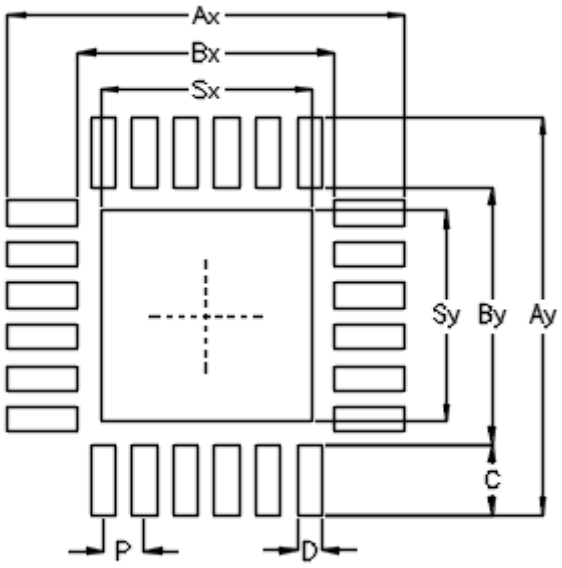
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-24	Option1	24	0.50	4.80	4.80	3.10	3.10	0.85	0.30	2.55	2.55	±0.05
	Option2									2.60	2.60	

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