Single Phase PWM Controller for CPU Core Power Supply

General Description

The RT8153C/D is a single phase PWM controller with integrated MOSFET drivers. Moreover, it is compliant with Intel IMVP6.5 Voltage Regulator Specification to fulfill its mobile CPU core and Render core voltage regulator requirements. The RT8153C/D adopts G-NAVP (Green Native AVP), which is a Richtek proprietary topology derived from finite DC gain compensator constant on-time mode, making it an easy setting PWM controller which meets all Intel AVP (Active Voltage Positioning) mobile CPU/Render requirements. The output voltage of the RT8153C/D is set by a 7-bit VID code. The built in high accuracy DAC converts the VID code into a voltage ranging from 0V to 1.5V with 12.5mV per step. The system accuracy of the controller can reach 1.5%.

The part supports VID on the fly and mode change on the fly functions that are fully compliant with IMVP6.5 specification. It operates in single phase and diode emulation modes. It can reach up to 90% efficiency in different modes according to different loading conditions.

The RT8153C/D includes power good and thermal throttling indicator and an additional clock enabling for CPU core specification. The soft-start and output transition slew rate is programmable by an external capacitor. It also features complete fault protection functions including over voltage, under voltage, negative voltage, over current and thermal shutdown. The RT8153C/D is available in WQFN-32L 5x5 and WQFN-32L 4x4 small foot print packages.

Applications

- IMVP 6.5 V_{CORE}/Render
- AVP Step-Down Converter
- Notebook / Desktop Computer / Servers

Features

- **Single Phase PWM Controller with Integrated MOSFET Driver**
- **G-NAVP™ Control Topology**
- **7-bit DAC with 0.8% DAC Accuracy**
- **1.5% or 11.5mV System Accuracy**
- **Fixed V_{BOOT} 1.1V (Only for RT8153C CPU Core Only)**
- **Fixed V_{BOOT} 1.2V (Only for RT8153D CPU Core Only)**
- **Current Monitor Output**
- **Built-in Offset Programming for Platform**
- **Differential Remote Voltage Sensing**
- **Diode Emulation Mode at Light Load Condition**
- **Programmable Output Transition Slew Rate Control**
- **System Thermal Compensated AVP**
- **Fast Transient Response**
- **Load Line Enable/Disable**
- **Power Good Indicator**
- **Clock Enable Output (For CPU Core Only)**
- **Thermal Throttling**
- **Switching Frequency Up to 1MHz**
- **OVP, UVP, OCP, OTP, UVLO, NVP**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT8153C/D□□□

- Package Type
  - QW : WQFN-32L 5x5 (W-Type)
  - QW : WQFN-32L 4x4 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
  - Z : ECO (Ecological Element with Halogen Free and Pb free)
- Package Size
  - L : 5x5
  - S : 4x4
- V_{BOOT}
  - C : 1.1V
  - D : 1.2V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8153CLGQW

RT8153CLGQW : Product Number
YMDNN : Date Code

RT8153DLGQW

RT8153DLGQW : Product Number
YMDNN : Date Code

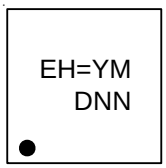
RT8153CLZQW

RT8153CLZQW : Product Number
YMDNN : Date Code

RT8153DLZQW

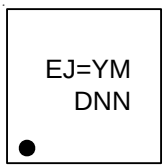
RT8153DLZQW : Product Number
YMDNN : Date Code

RT8153CSGQW



EH= : Product Code
YMDNN : Date Code

RT8153DSGQW



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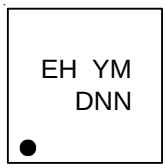
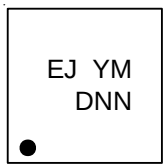
RT8153CSZQW



EH : Product Code
YMDNN : Date Code

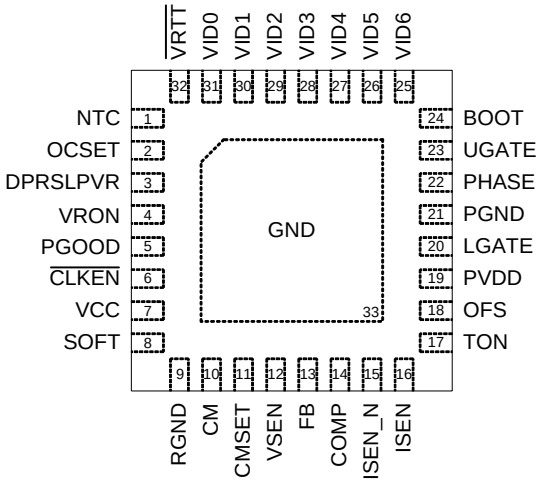
RT8153DSZQW



EJ : Product Code
YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-32L 5x5 / WQFN-32L 4x4

Typical Application Circuit

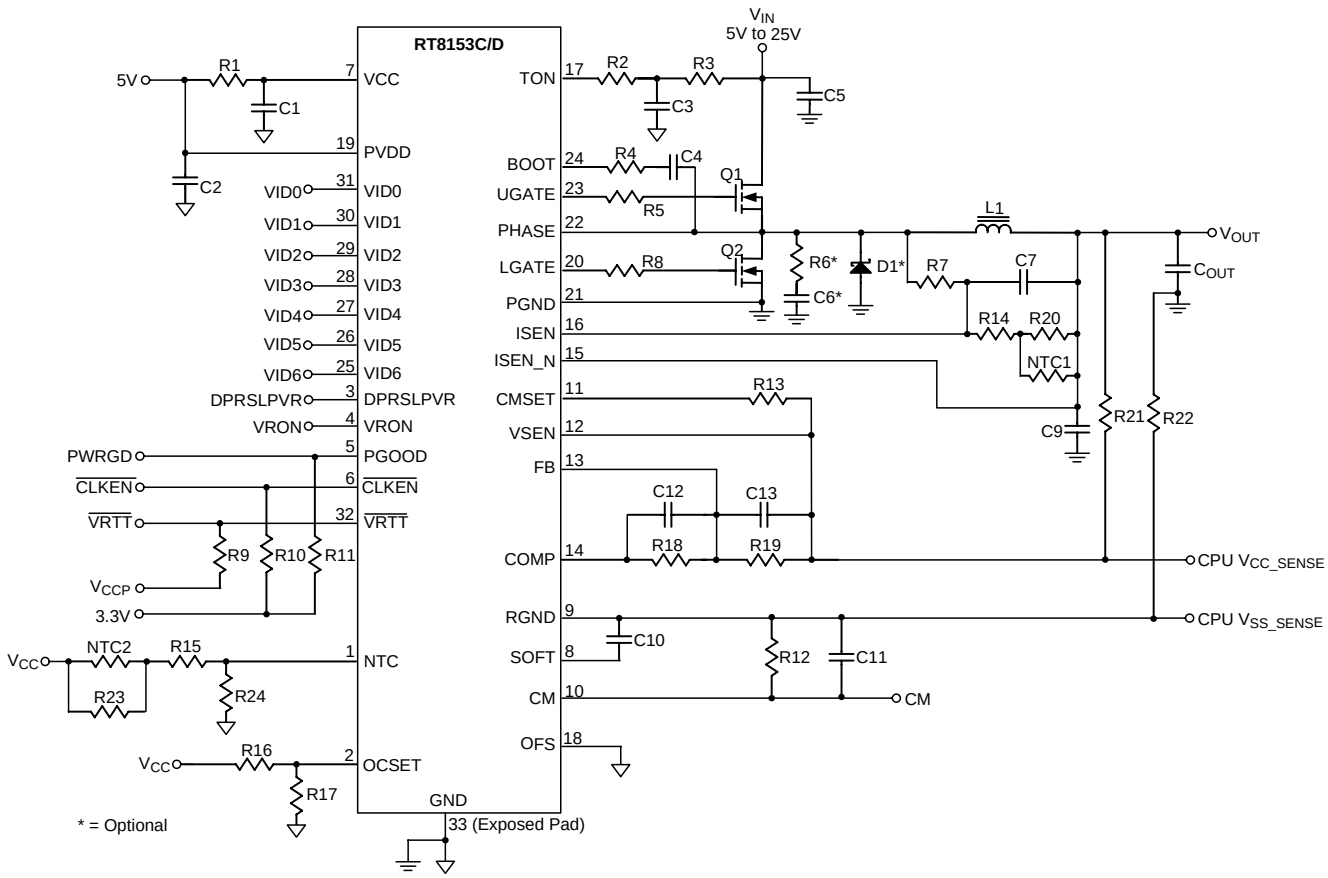


Figure 1. IMVP 6.5 CPU Core Application Circuit

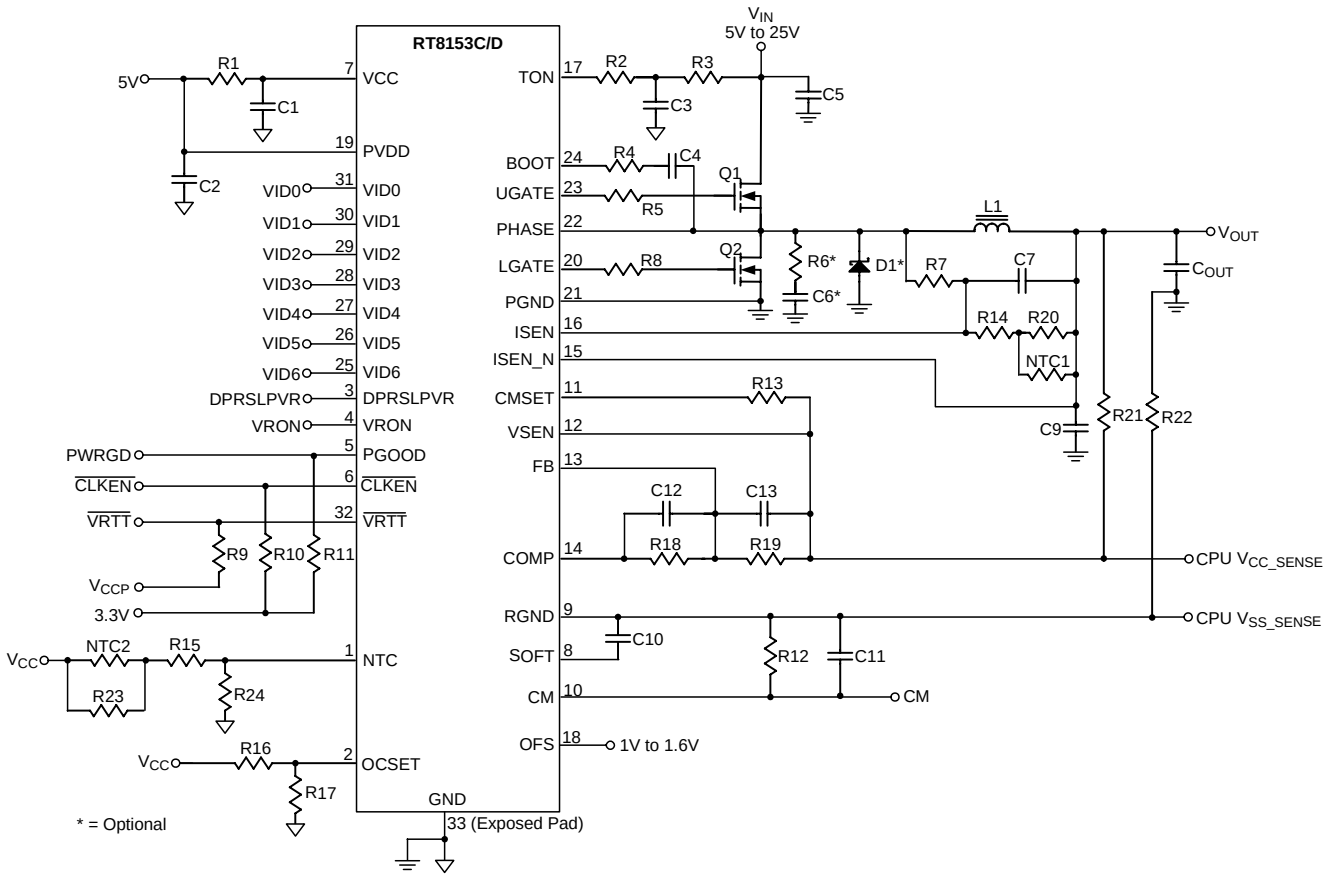


Figure 2. IMVP 6.5 CPU Core with Offset Application Circuit

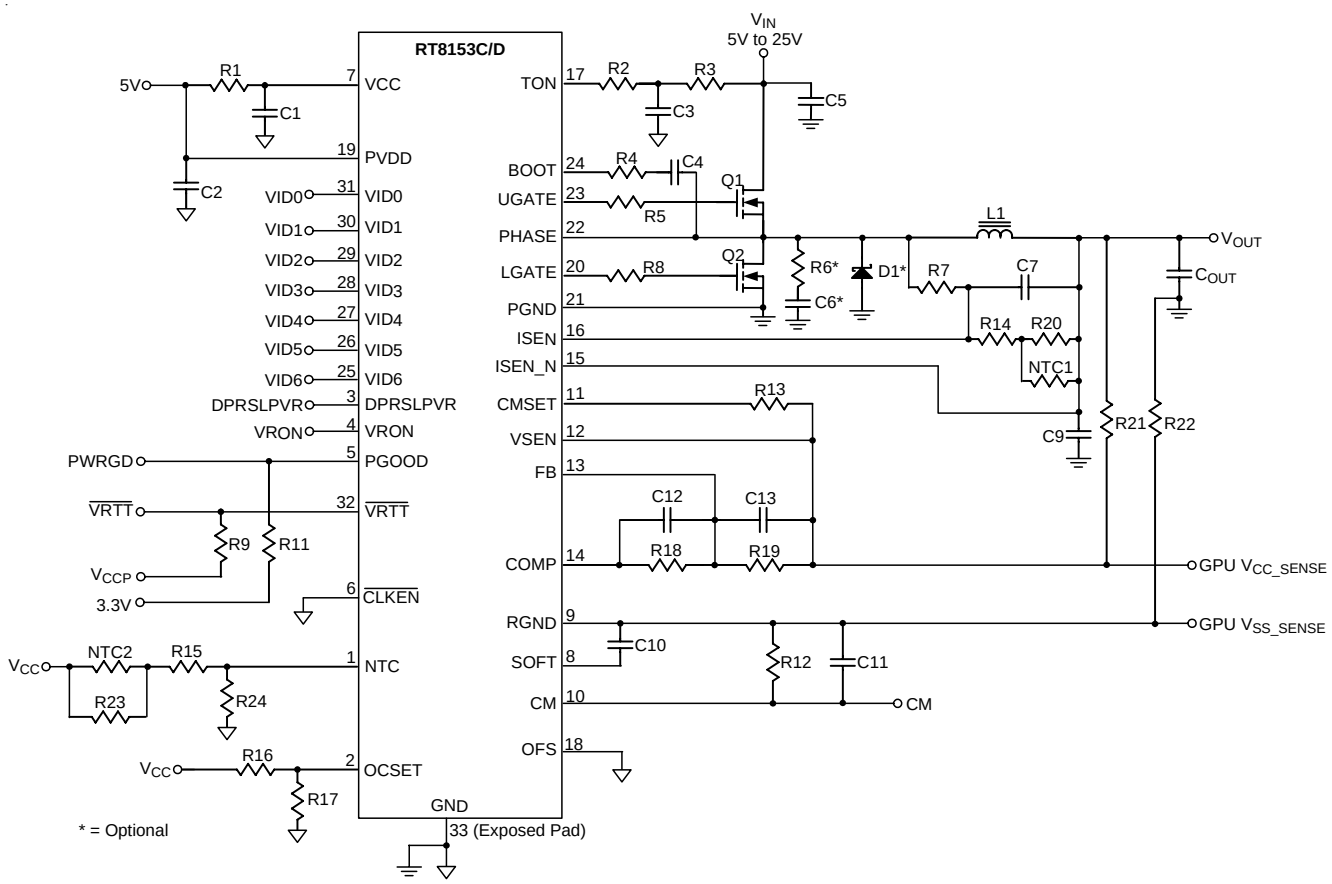


Figure 3. IMVP 6.5 Render Application Circuit

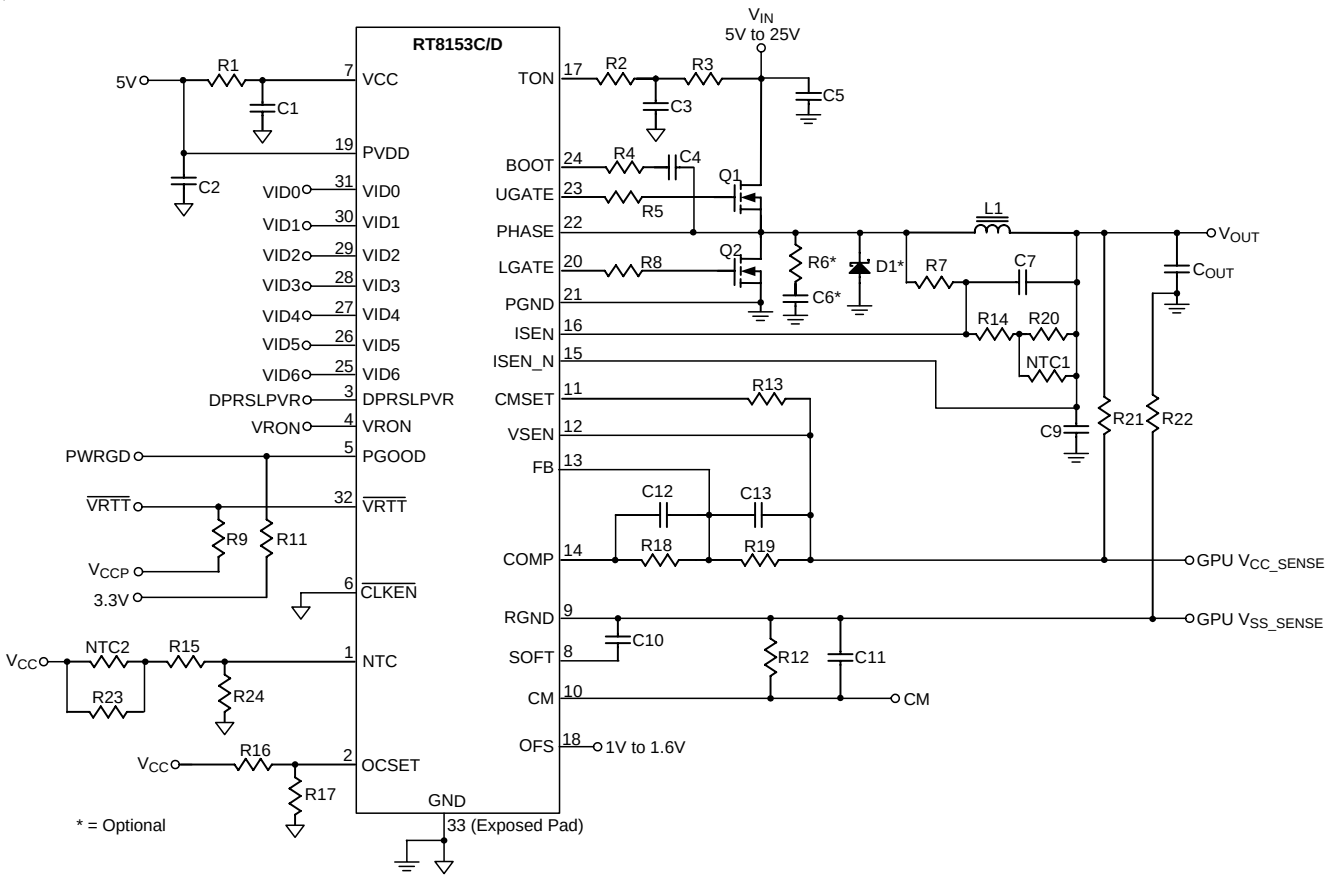


Figure 4. IMVP 6.5 Render with Offset Application Circuit

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	NTC	Thermal Detection Input for $\overline{VRTT}$ Circuit. Connect this pin with a resistor divider from V_{CC} using NTC on the top to set the thermal management threshold level. Furthermore, this pin provides load line enable/disable function.
2	OCSET	Over Current Protection Setting. Connect a resistor voltage divider from V_{CC} to ground, the joint of the resistive voltage divider is connected to the OCSET pin, with a voltage V_{OCSET}, to set the over current threshold I_{LIM}.
3	DPRSLPVR	Deeper Sleep Mode Signal.
4	VRON	Voltage Regulator Enabler.
5	PGOOD	Power Good Indicator.
6	$\overline{CLKEN}$	Inverted Clock Enable. Pull high by a resistor for CPU core application. This open-drain pin is an output indicating the start of the PLL locking of the clock chip. Connect to GND for Render application.
7	VCC	Chip Power.
8	SOFT	Soft-Start. This pin provides soft-start function and slew rate controller. The capacitance of the slew rate control capacitor is restricted to be larger than 10nF. The feedback voltage of the converter follows the ramping voltage on the SOFT pin during soft-start and other voltage transitions according to different mode of operation and VID change.
9	RGND	Return Ground. This pin is the negative node of the differential remote voltage sensing.
10	CM	Current Monitor Output. This pin outputs a voltage proportional to the output current.
11	CMSET	Current Monitor Output Gain Externally Setting. Connect this pin with one resistor to VSEN the while CM pin is connected to ground with another resistor. In such a way, the current monitor output gain can be set by the ratio of these two resistors.
12	VSEN	Positive Voltage Sensing Pin. This pin is the positive node of the differential voltage sensing.
13	FB	Feedback. This is the negative input node of the error amplifier.
14	COMP	Compensation Pin. This pin is the output node of the error amplifier.
15	ISEN_N	Negative Input of the Current Sense.
16	ISEN	Positive Input of the Current Sense.
17	TON	Connect this Pin to V_{IN} with One Resistor.
18	OFS	Output Voltage Offset Setting.
19	PVDD	Driver Power.
20	LGATE	Lower Gate Drive. This pin drives the gate of the low side MOSFETs.
21	PGND	Driver Ground.
22	PHASE	This pin is the return node of the high side MOSFET driver. Connect this pin to the high side MOSFET sources together with the low side MOSFET drains and the inductor.
23	UGATE	Upper Gate Drive. This pin drives the gate of the high side MOSFETs.
24	BOOT	Bootstrap Power Pin. This pin powers the high side MOSFET drivers. Connect this pin to bootstrap capacitor.

To be continued

Pin No.	Pin Name	Pin Function
25 to 31	VID6 to VID0	Voltage ID. DAC voltage identification inputs for IMVP6.5. The logic threshold is 30% of VCC as the maximum value for low state and 70% of the VCC as the minimum value for the high state.
32	$\overline{\text{VRTT}}$	Voltage Regulator Thermal Throttling. This open drain output pin will be pulled low when the preset temperature level is exceeded.
33 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram

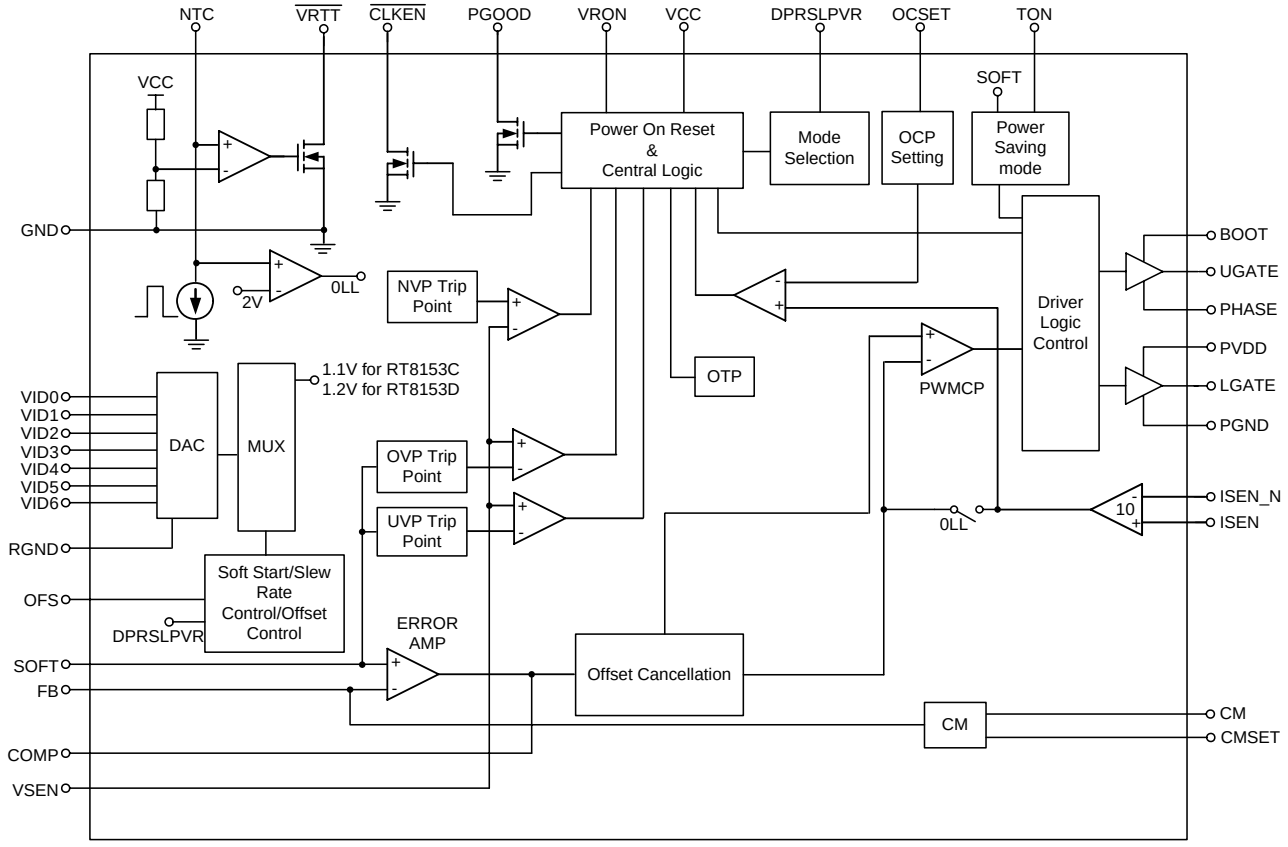


Table 1. IMVP6.5 VID Code Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
0	0	0	0	0	0	0	1.5000V
0	0	0	0	0	0	1	1.4875V
0	0	0	0	0	1	0	1.4750V
0	0	0	0	0	1	1	1.4625V
0	0	0	0	1	0	0	1.4500V
0	0	0	0	1	0	1	1.4375V
0	0	0	0	1	1	0	1.4250V
0	0	0	0	1	1	1	1.4125V
0	0	0	1	0	0	0	1.4000V
0	0	0	1	0	0	1	1.3875V
0	0	0	1	0	1	0	1.3750V
0	0	0	1	0	1	1	1.3625V
0	0	0	1	1	0	0	1.3500V
0	0	0	1	1	0	1	1.3375V
0	0	0	1	1	1	0	1.3250V
0	0	0	1	1	1	1	1.3125V
0	0	1	0	0	0	0	1.3000V
0	0	1	0	0	0	1	1.2875V
0	0	1	0	0	1	0	1.2750V
0	0	1	0	0	1	1	1.2625V
0	0	1	0	1	0	0	1.2500V
0	0	1	0	1	0	1	1.2375V
0	0	1	0	1	1	0	1.2250V
0	0	1	0	1	1	1	1.2125V
0	0	1	1	0	0	0	1.2000V
0	0	1	1	0	0	1	1.1875V
0	0	1	1	0	1	0	1.1750V
0	0	1	1	0	1	1	1.1625V
0	0	1	1	1	0	0	1.1500V
0	0	1	1	1	0	1	1.1375V
0	0	1	1	1	1	0	1.1250V
0	0	1	1	1	1	1	1.1125V
0	1	0	0	0	0	0	1.1000V

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
0	1	0	0	0	0	1	1.0875V
0	1	0	0	0	1	0	1.0750V
0	1	0	0	0	1	1	1.0625V
0	1	0	0	1	0	0	1.0500V
0	1	0	0	1	0	1	1.0375V
0	1	0	0	1	1	0	1.0250V
0	1	0	0	1	1	1	1.0125V
0	1	0	1	0	0	0	1.0000V
0	1	0	1	0	0	1	0.9875V
0	1	0	1	0	1	0	0.9750V
0	1	0	1	0	1	1	0.9625V
0	1	0	1	1	0	0	0.9500V
0	1	0	1	1	0	1	0.9375V
0	1	0	1	1	1	0	0.9250V
0	1	0	1	1	1	1	0.9125V
0	1	1	0	0	0	0	0.9000V
0	1	1	0	0	0	1	0.8875V
0	1	1	0	0	1	0	0.8750V
0	1	1	0	0	1	1	0.8625V
0	1	1	0	1	0	0	0.8500V
0	1	1	0	1	0	1	0.8375V
0	1	1	0	1	1	0	0.8250V
0	1	1	0	1	1	1	0.8125V
0	1	1	1	0	0	0	0.8000V
0	1	1	1	0	0	1	0.7875V
0	1	1	1	0	1	0	0.7750V
0	1	1	1	0	1	1	0.7625V
0	1	1	1	1	0	0	0.7500V
0	1	1	1	1	0	1	0.7375V
0	1	1	1	1	1	0	0.7250V
0	1	1	1	1	1	1	0.7125V
1	0	0	0	0	0	0	0.7000V
1	0	0	0	0	0	1	0.6875V

To be continued

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
1	0	0	0	0	1	0	0.6750V
1	0	0	0	0	1	1	0.6625V
1	0	0	0	1	0	0	0.6500V
1	0	0	0	1	0	1	0.6375V
1	0	0	0	1	1	0	0.6250V
1	0	0	0	1	1	1	0.6125V
1	0	0	1	0	0	0	0.6000V
1	0	0	1	0	0	1	0.5875V
1	0	0	1	0	1	0	0.5750V
1	0	0	1	0	1	1	0.5625V
1	0	0	1	1	0	0	0.5500V
1	0	0	1	1	0	1	0.5375V
1	0	0	1	1	1	0	0.5250V
1	0	0	1	1	1	1	0.5125V
1	0	1	0	0	0	0	0.5000V
1	0	1	0	0	0	1	0.4875V
1	0	1	0	0	1	0	0.4750V
1	0	1	0	0	1	1	0.4625V
1	0	1	0	1	0	0	0.4500V
1	0	1	0	1	0	1	0.4375V
1	0	1	0	1	1	0	0.4250V
1	0	1	0	1	1	1	0.4125V
1	0	1	1	0	0	0	0.4000V
1	0	1	1	0	0	1	0.3875V
1	0	1	1	0	1	0	0.3750V
1	0	1	1	0	1	1	0.3625V
1	0	1	1	1	0	0	0.3500V
1	0	1	1	1	0	1	0.3375V
1	0	1	1	1	1	0	0.3250V
1	0	1	1	1	1	1	0.3125V
1	1	0	0	0	0	0	0.3000V

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output
1	1	0	0	0	0	1	0.2875V
1	1	0	0	0	1	0	0.2750V
1	1	0	0	0	1	1	0.2625V
1	1	0	0	1	0	0	0.2500V
1	1	0	0	1	0	1	0.2375V
1	1	0	0	1	1	0	0.2250V
1	1	0	0	1	1	1	0.2125V
1	1	0	1	0	0	0	0.2000V
1	1	0	1	0	0	1	0.1875V
1	1	0	1	0	1	0	0.1750V
1	1	0	1	0	1	1	0.1625V
1	1	0	1	1	0	0	0.1500V
1	1	0	1	1	0	1	0.1375V
1	1	0	1	1	1	0	0.1250V
1	1	0	1	1	1	1	0.1125V
1	1	1	0	0	0	0	0.1000V
1	1	1	0	0	0	1	0.0875V
1	1	1	0	0	1	0	0.0750V
1	1	1	0	0	1	1	0.0625V
1	1	1	0	1	0	0	0.0500V
1	1	1	0	1	0	1	0.0375V
1	1	1	0	1	1	0	0.0250V
1	1	1	0	1	1	1	0.0125V
1	1	1	1	0	0	0	0.0000V
1	1	1	1	0	0	1	0.0000V
1	1	1	1	0	1	0	0.0000V
1	1	1	1	0	1	1	0.0000V
1	1	1	1	1	0	0	0.0000V
1	1	1	1	1	0	1	0.0000V
1	1	1	1	1	1	0	0.0000V
1	1	1	1	1	1	1	0.0000V

Absolute Maximum Ratings (Note 1)

- V_{CC} to GND ---------- –0.3V to 6.5V
- RGND, PGND to GND ---------- –0.3V to 0.3V
- VIDx to GND ---------- –0.3V to (V_{CC} + 0.3V)
- DPRSLPVR, VRON to GND ---------- –0.3V to (V_{CC} + 0.3V)
- PGOOD, $\overline{\text{CLKEN}}$, $\overline{\text{VRTT}}$ to GND ---------- –0.3V to (V_{CC} + 0.3V)
- VSEN, FB, COMP, SOFT, OCSET, CM, CMSET, NTC to GND ---------- –0.3V to (V_{CC} + 0.3V)
- ISEN, ISEN_N to GND ---------- –0.3V to (V_{CC} + 0.3V)
- PVDD to PGND ---------- –0.3V to 6.5V
- LGATE to PGND
  - DC ---------- –0.3V to (PVDD + 0.3V)
  - <20ns ---------- –2.5V to 7.5V
- PHASE to PGND
  - DC ---------- –0.3V to 30V
  - <20ns ---------- –8V to 38V
- BOOT to PHASE ---------- –0.3V to 6.5V
- UGATE to PHASE
  - DC ---------- –0.3V to (PVDD + 0.3V)
  - <20ns ---------- –5V to 7.5V
- TON to GND ---------- –0.3V to 30V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–32L 5x5 ---------- 2.778W
  - WQFN–32L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 2)
  - WQFN–32L 5x5, θ_{JA} ---------- 36°C/W
  - WQFN–32L 5x5, θ_{JC} ---------- 6°C/W
  - WQFN–32L 4x4, θ_{JA} ---------- 52°C/W
  - WQFN–32L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 4.5V to 5.5V
- Battery Voltage, V_{IN} ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
OFS Function (Only for RT8153C/D)							
OFS Threshold Voltage	Enable Offset		V_{OFS} > 0.92V before VRON rising	0.92	1.2	--	V
	Disable Offset		V_{OFS} connected to GND before VRON rising				
Set OFS voltage		V_{OFS}	No Offset Voltage	--	1.2	--	V
			Offset 400mV	--	1.6	--	
			Offset –200mV	--	1	--	
Impedance		R_{OFS}		1	--	--	MΩ
OLL Function							
NTC		I_{0LL}	Pulse sinking current source NTC resistor at VRON rising edge.	--	80	--	µA
		V_{0LL}	Detect and Latch voltage at NTC pin at VRON rising edge. V_{NTC} < V_{0LL}, enable 0 Load Line Function.	2	--	--	V
Supply Input							
Supply Voltage		V_{CC}		4.5	5	5.5	V
Supply Current		I_{VCC} + I_{PVCC}	V_{RON} = 3.3V, Not Switching	--	--	10	mA
Shutdown Current		I_{CC} + I_{PVCC}	V_{RON} = 0V	--	--	5	µA
Soft-Start/Slew Rate Control (based on 10nF C_{SS})							
Soft-Start / Soft-Shutdown		I_{SS1}	V_{SOFT} = 1.5V	--	20	--	µA
Normal VID change slew current		I_{SS2}	V_{SOFT} = 1.5V	40	50	60	µA
Deeper Sleep Exit/VID Change Slew Current (only at IMVP6.5 Render application)		I_{SS3}	V_{SOFT} = 1.5V	80	100	120	µA
Reference and DAC							
DC Accuracy		V_{FB}	V_{VID} = 0.7500 – 1.5000 (No Load, Active Mode)	–0.5	0	0.5	%VID
			V_{VID} = 0.5000 – 0.7500	–7.5	0	7.5	mV
Boot Voltage		V_{BOOT}	For RT8153C VCORE	1.089	1.1	1.111	V
			For RT8153D VCORE	1.188	1.2	1.212	
Error Amplifier							
Input Offset Voltage		V_{OSEA}		–2	--	2	mV
DC Gain			R_L = 47kΩ	70	80	--	dB
Gain Bandwidth Product		GBW	C_{LOAD} = 5pF	--	10	--	MHz
Slew Rate		SR_{COMP}	C_{LOAD} = 10pF (Gain = –4, R_F = 47kΩ, V_{OUT} = 0.5V – 3V)	--	5	--	V/µs
Output Voltage Range		V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Source Current	I_{OUTEA_COMP}	V_{COMP} = 2V	200	250	--	μA
Maximum Sink Current		V_{COMP} = 2V	20	--	--	mA
Current Sense Amplifier						
Input Offset Voltage	V_{OSCS}		–1	--	1	mV
Impedance at Neg. Input	R_{ISEN_N}		1	--	--	MΩ
Impedance at Pos Input	R_{ISEN}		1	--	--	MΩ
DC Gain		1 Phase Operating	--	10	--	V/V
V_{ISEN} Linearity	V_{ISEN_ACC}	–30mV < I_{SEN_IN} < 50mV	–1		1	%
DEM TON Setting						
TON Pin Output Voltage	V_{TON}	I_{TON} = 80μA, V_{TON} = V_{VID} = 0.75	–5	0	5	%
DEM ON-Time Setting	t_{ON}	I_{RTON} = 80μA	--	350	--	ns
R_{TON} Current Range	I_{RTON}		25	--	280	μA
Protection						
Under Voltage Lock out Threshold	V_{UVLO}	Falling Edge.	4.1	4.3	4.5	V
UVLO Hysteresis			--	200	--	mV
Absolute Over Voltage Protection Threshold	V_{OVABS}	(Respect to 1.7V, ±50mV)	1.65	1.7	1.75	V
Absolute Over Voltage Offset	V_{OVABS_OFS}	(Respect to 2V, ±50mV)	1.95	2	2.05	V
Relative Over Voltage Protection Threshold	V_{OV}	(Respect to V_{DAC}, ±50mV)	250	300	350	mV
Under Voltage Protection Threshold	V_{UV}	Measured at VSEN with respect to Unloaded Output Voltage (UOV) (for 0.8 < UOV < 1.5)	–450	–400	–350	mV
Negative Voltage Protection Threshold	V_{NV}	Measured at VSEN with Respect to GND	–100	--	--	mV
Current Limit Threshold Voltage	V_{ILIMIT}	V_{ISEN} – V_{ISEN_N} = V_{ILIM}, V_{OCSET} = 2.4V, 48 x V_{ILIMT} = V_{OCSET}	45	50	55	mV
Thermal Shut Down Threshold	T_{SD}		--	160	--	°C
Thermal Shut Down Hysteresis	ΔT_{SD}		--	10	--	°C
Logic Inputs						
VRON Threshold	V_{IH}	Respect to 1.05V, 70%	0.735	--	--	V
	V_{IL}	Respect to 1.05V, 30%	--	--	0.315	
Leakage Current of VRON			–1	--	1	μA
DAC (VID0 to VID6) and DPRSLPVR	V_{IH}	Respect to 1.05V, 70%	0.735	--	--	V
	V_{IL}	Respect to 1.05V, 30%	--	--	0.315	
Leakage Current of DAC (VID0 to VID6), $\overline{PSI}$ and DPRSLPVR			–1	--	1	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good						
PGOOD Low Voltage	V_{PGOOD}	I_{PGOOD} = 4mA	--	--	0.4	V
PGOOD Delay	t_{PGD}	$\overline{CLK\_EN}$ Low to PGOOD High	3	--	20	ms
Clock Enable						
$\overline{CLKEN}$ Low Voltage	$V_{\overline{CLKEN}}$	$I_{\overline{CLKEN}}$ = 4mA (only for V_{CORE})	--	--	0.4	V
Thermal Throttling						
Thermal Throttling Threshold	V_{OT}	Measure at NTC Respect to V_{CC}	--	80	--	%VDD
Thermal Throttling Threshold Hysteresis	V_{OT_HY}	At V_{CC} = 5V	--	230	--	mV
$\overline{VRTT}$ Output Voltage	$V_{\overline{VRTT}}$	$I_{\overline{VRTT}}$ = –40mA	--	--	0.4	V
Current Monitor						
Current Monitor Output Voltage in Operating Range		$V_{ISEN} - V_{ISEN\_N}$= 20mV, R_{CM} = 18kΩ, R_{CMSET} = 12kΩ	450	480	510	mV
Current Monitor Maximum Output Voltage			--	--	1.15	V
Gate Driver						
Upper Driver Source	$R_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 5V $V_{BOOT} - V_{LGATE}$ = 1V	--	1	--	Ω
Upper Driver Sink	$R_{UGATEsk}$	V_{UGATE} = 1V		1		Ω
Lower Driver Source	$R_{LGATEsr}$	V_{PVDD} = 5V, $V_{PVDD} - V_{LGATE}$ = 1V	--	1	--	Ω
Lower Driver Sink	$R_{LGATEsk}$	V_{LGATE} = 1V	--	0.5	--	Ω
Upper Driver Source/Sink Current	I_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 5V V_{UGATE} = 2.5V	--	2	--	A
Lower Driver Source Current	$I_{LGATEsr}$	V_{LGATE} = 2.5V	--	2	--	A
Lower Driver Sink Current	$I_{LGATEsk}$	V_{LGATE} = 2.5V	--	4	--	A
Internal Boot Charging Switch On Resistance	R_{BOOT}	PVDD to BOOT	--	30	--	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

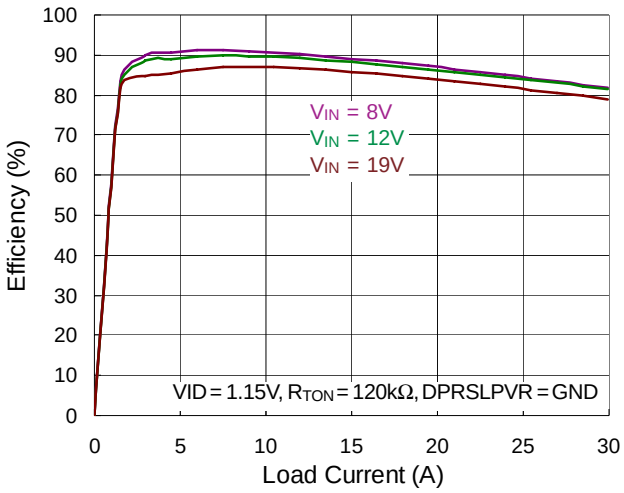
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layers test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

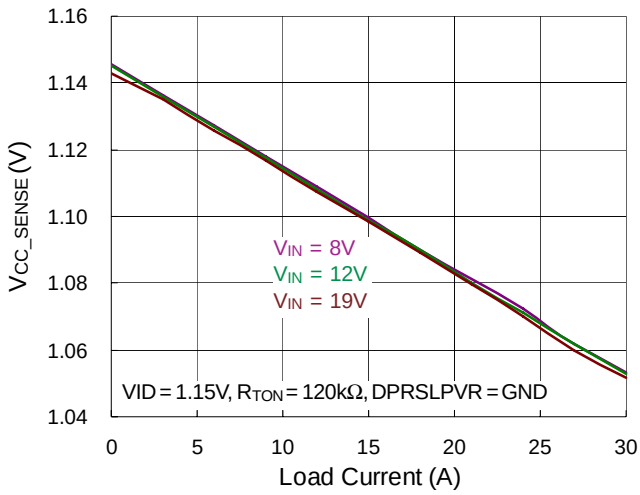
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

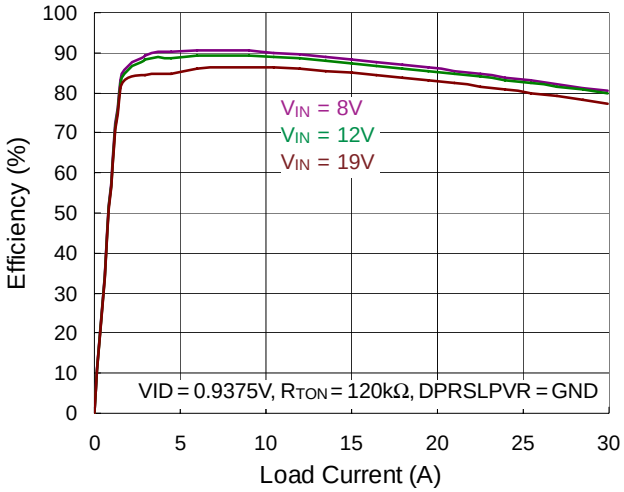
CCM Efficiency vs. Load Current



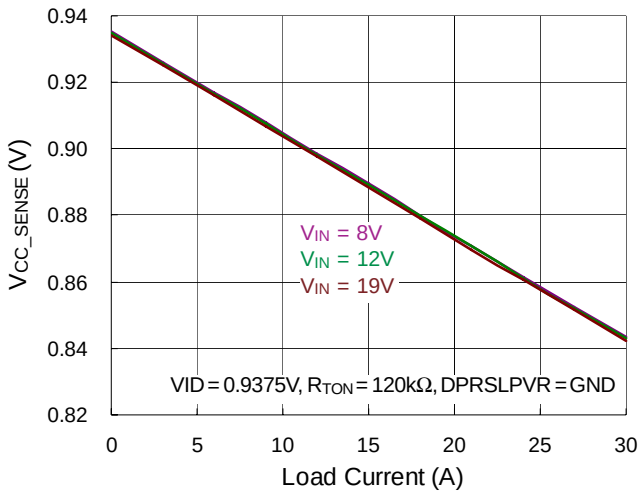
CCM V_{CC_SENSE} vs. Load Current



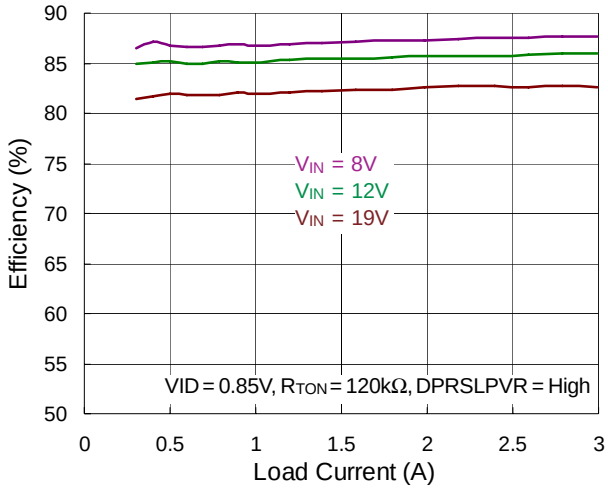
CCM Efficiency vs. Load Current



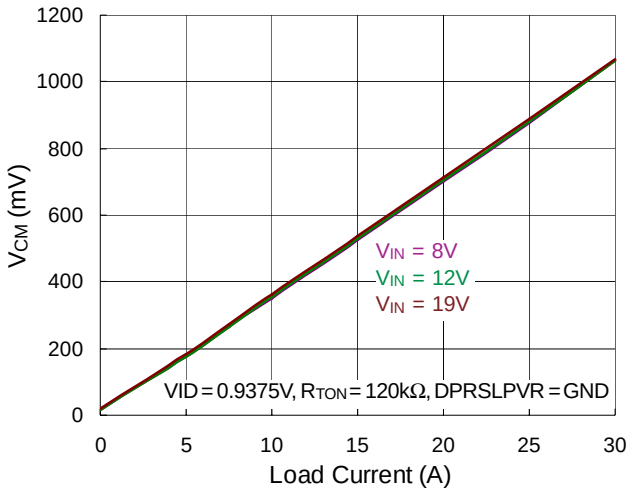
CCM V_{CC_SENSE} vs. Load Current



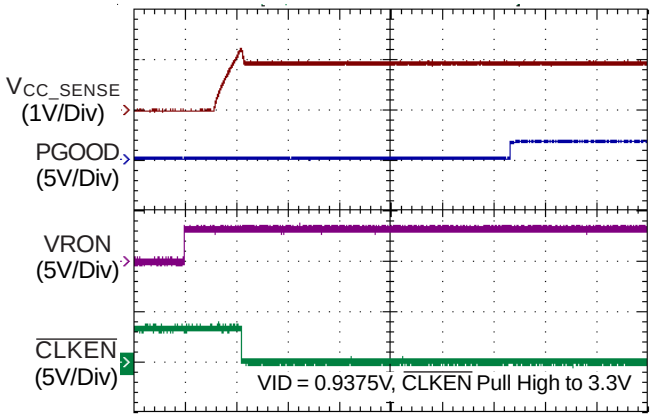
DEM Efficiency vs. Load Current



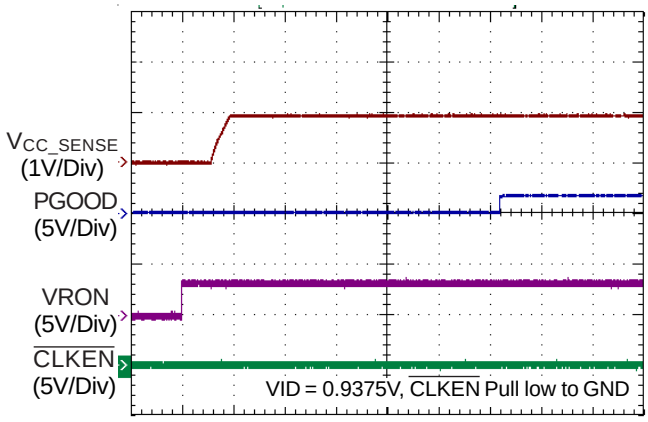
V_{CM} vs. Load Current



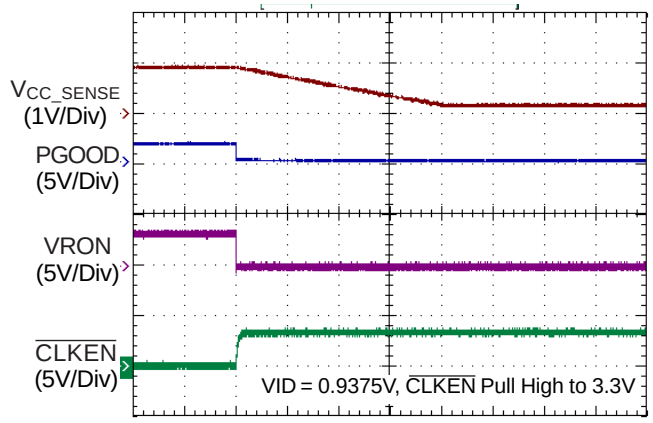
CPU Mode Power On



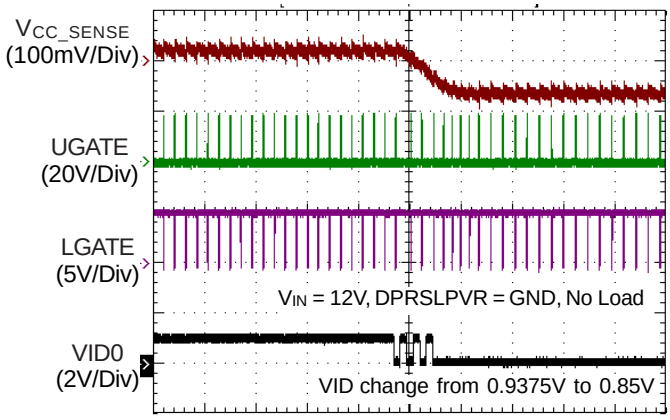
Render Mode Power On



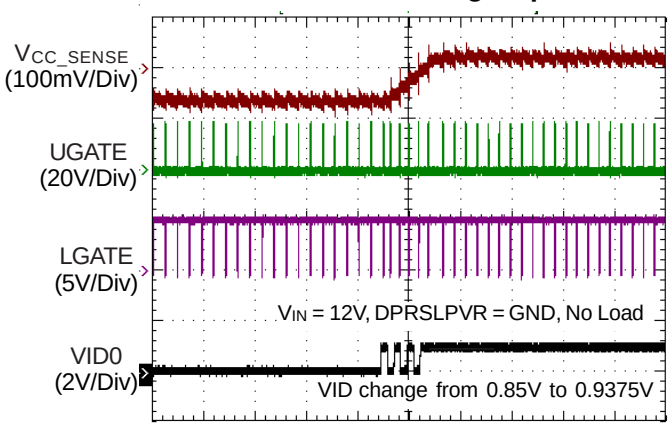
CPU Mode Power Down



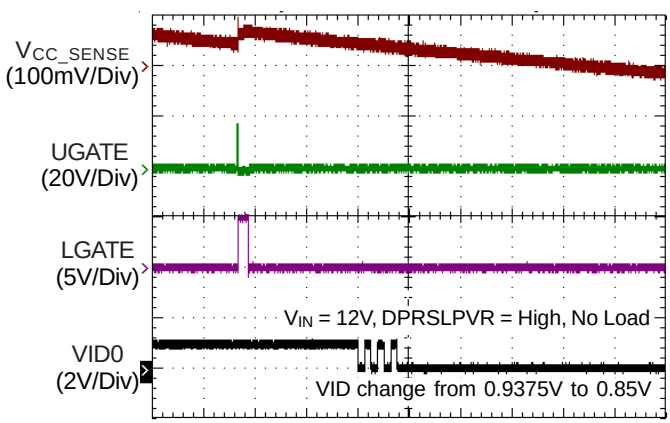
CCM VID Change Down



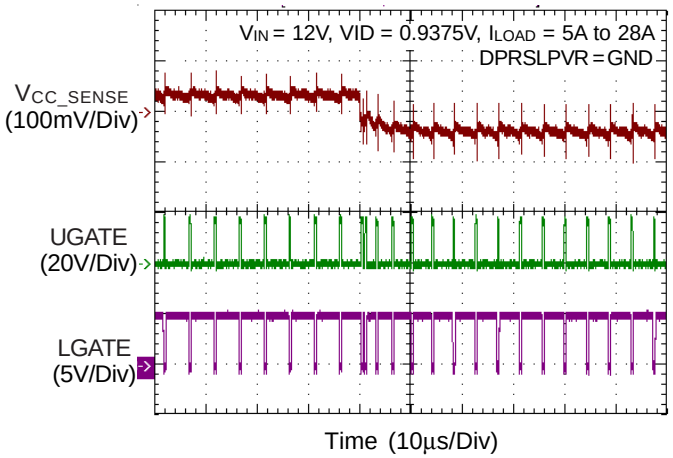
CCM VID Change Up



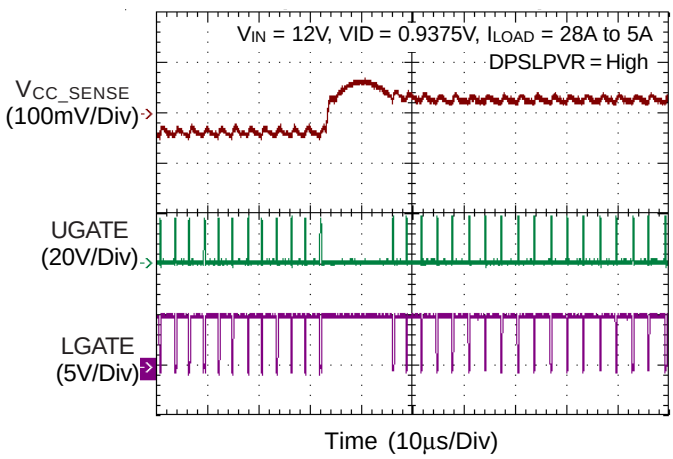
CPU-DEM VID Change Down



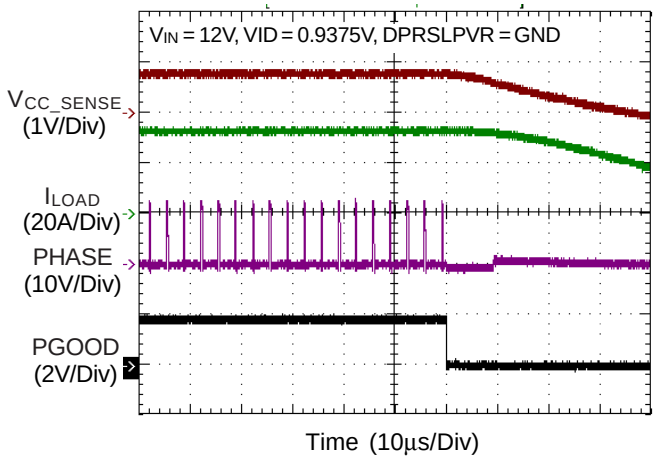
CCM Load Transient Response



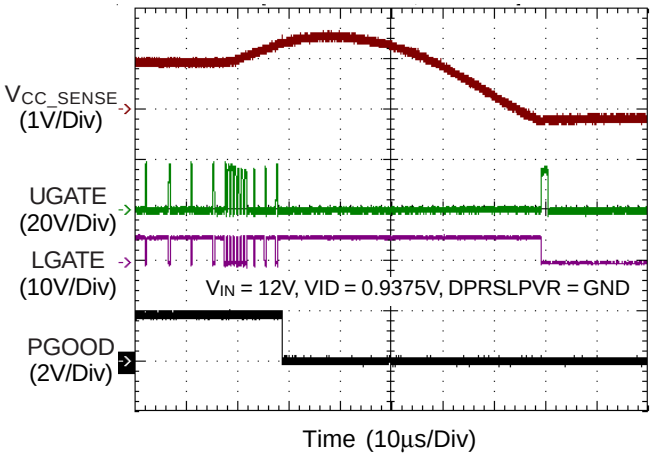
CCM Load Transient Response



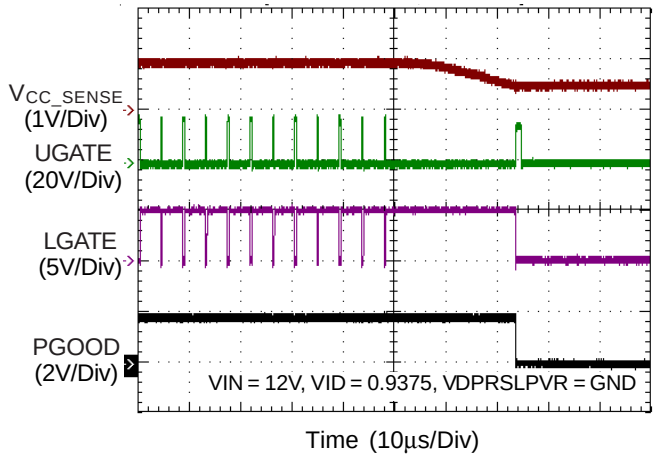
Over Current Protection



Over Voltage Protection



Under Voltage Protection



Application Information

The RT8153C/D is a single-phase PWM controller with embedded gate driver. It is compliant with Intel IMVP6.5 Voltage Regulator Specification to fulfill its mobile CPU and Render voltage regulator power supply requirement. Inductor current are continuously sensed for loop control, droop tuning, and over current protection. The 7-bit VID DAC and low offset differential amplifier allow the controller to maintain high regulating accuracy to meet Intel's IMVP6.5 specification.

Design Tool

To help users to reduce the efforts and errors caused by manual calculations using the design concept below, a user-friendly design tool is now available on request.

This design tool calculates all necessary design parameters by entering user's requirements. Please contact Richtek's representatives for details.

Operation Modes

Table 2 shows the RT8153C/D operation modes. When VRON is enabled (=1), the RT8153C/D will detect $\overline{\text{CLKEN}}$ within 10μs to determine which operation mode is applied. If $\overline{\text{CLKEN}}$ is low, the RT8153C/D will operate in Render core voltage regulator mode. If $\overline{\text{CLKEN}}$ is high, the IC will operate in CPU core voltage regulator mode.

DPRSLPVR determines whether the operation mode of the controller operation is in CCM or DEM. The controller enters DEM (Diode Emulation Mode) when DPRSLPVR = 1 and enters CCM when DPRSLPVR = 0.

Table 2. Control Signal Truth Table for Operation Modes of the RT8153C/D

$\overline{\text{CLKEN}}$	DPRSLPVR	Operation Mode
0 (GND)	0	Render CCM
	1	Render DEM
1 (Pull High)	0	CPU CCM
	1	CPU DEM

Differential Remote Sense Connection

The RT8153C/D includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes, and socket contacts. CPU contains on-die sense pins V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE}. Connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier. Connect VSEN to V_{CC_SENSE} for $\overline{\text{CLKEN}}$, PGOOD, OVP, and UVP detection. The 7 bit VID DAC and the precision voltage reference are referred to RGND for accurate remote sensing.

Current Sense Setting

The RT8153C/D is continuously sensing the inductor current. Therefore, the controller can be less noise sensitive. Low offset amplifiers are used for loop control and over current detection. The internal current sense amplifier gain (A_I) is fixed to be 10. ISEN and ISEN_N denote the positive and negative inputs of the current sense amplifier.

Users can either use a current-sense resistor or the inductor's DCR for current sensing. Using inductor's DCR allows higher efficiency as shown in Figure 5. If

$$\frac{L}{DCR} = R_X \times C_X \quad (1)$$

then the transient performance will be optimum. For example, choose L = 0.36μH with 1mΩ DCR and C_X = 100nF, to yield for R_X :

$$R_X = \frac{0.36\mu H}{1m\Omega \times 100nF} = 3.6k\Omega \quad (2)$$

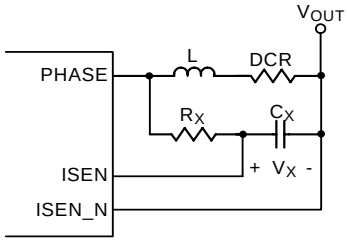


Figure 5. Lossless Inductor Current Sensing

Considering the inductance tolerance, the resistor, R_X, has to be tuned on board by examining the transient voltage. If the output voltage transient has an initial dip below the minimum load line requirement with a slow recovery, R_X is chosen too small. Vice-versa, with a resistance too large, the output voltage transient has only a small initial dip and the recovery become too fast, causing a ring-back.

Since the DCR of inductor is highly temperature dependent, it affects the output accuracy, current monitor and over current protection accuracy at hot conditions. Temperature compensation is recommended for the lossless inductor DCR current sense method. Figure 6 shows a simple but effective way of compensating the temperature variations of the sense resistor using an NTC thermistor at DCR sensing network.

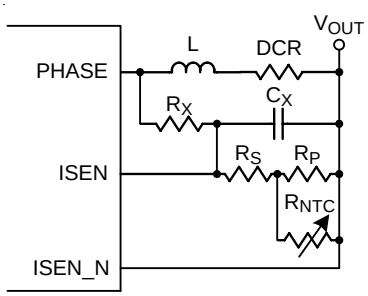


Figure 6. Lossless Inductor Current Sensing with NTC Compensation

Usually, R_P is set to equal R_{NTC}(25°C). R_S is selected to linearize the NTC's temperature characteristic. For a given NTC, design is to get R_S and R_X to compensate the temperature variations of the sense resistor.

Let

$$R_{equ} = R_S + (R_P \,//\, R_{NTC}) \quad (3)$$

Then, according to above circuit,

$$\frac{L}{DCR} = C_X \times \frac{R_{equ}}{R_X + R_{equ}} \quad (4)$$

Next, let

$$m = \frac{L}{DCR \times C_X} \quad (5)$$

Then

$$m \times \left(R_X + R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right) = R_X \times \left(R_S + \frac{R_{NTC} + R_P}{R_{NTC} + R_P} \right) \quad (6)$$

so

$$R_S = \frac{R_{NTC}R_PR_X - (mR_{NTC} + mR_P)R_X - mR_{NTC}R_P}{(-R_{NTC} - R_P)R_X + m(R_{NTC} + R_P)} \quad (7)$$

R_X can be expressed by :

$$R_X = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad (8)$$

where

$a = A_{TH}C_{TL} - A_{TL}C_{TH}$

$b = A_{TH}D_{TL} - B_{TL}C_{TH} - A_{TL}D_{TH}$

$c = B_{TL}D_{TH} - B_{TH}D_{TL}$

where

$A_{TH} = R_{NTC\_TH}R_P - m_{TH}R_{NTC\_TH} - m_{TH}R_P$

$A_{TL} = R_{NTC\_TL}R_P - m_{TL}R_{NTC\_TL} - m_{TL}R_P$

$B_{TH} = R_{NTC\_TH}R_P$

$B_{TL} = R_{NTC\_TL}R_P$

$C_{TH} = -R_{NTC\_TH} - R_P$

$C_{TL} = -R_{NTC\_TL} - R_P$

$D_{TH} = m_{TH}(R_{NTC\_TH} + R_P)$

$D_{TL} = m_{TL}(R_{NTC\_TL} + R_P)$

where X_{TH} denotes the value of this variable at high temperature, and X_{TL} denotes the value of this variable at low temperature.

Using current sense resistor in series with the inductor can have better accuracy, but the efficiency is a trade-off. Considering the equivalent inductance (L_{ESL}) of the current sense resistor, a RC filter is recommended. The RC filter calculation method is similar to the above-mentioned inductor DCR sensing method.

Loop Control

The RT8153C/D adopts Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite-gain current mode with CCRCOT (Constant Current Ripple Constant On Time) topology. The output voltage, V_{OUT}, will decrease with increasing output load current. The control loop consists of PWM modulator with power stage, current sense amplifier and error amplifier as shown in Figure 7.

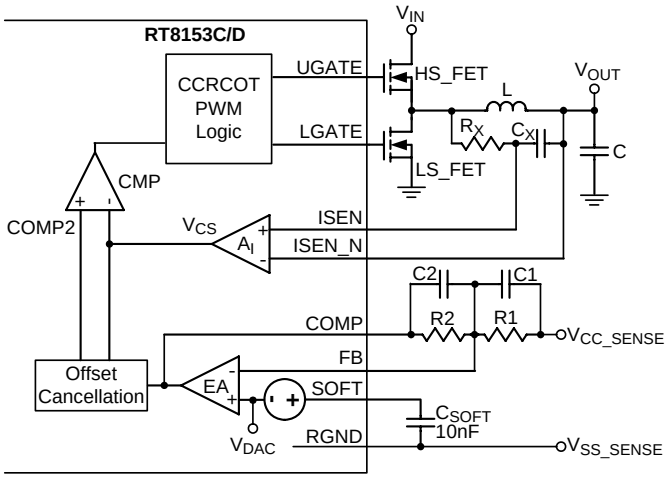


Figure 7. Simplified Schematic for Droop and Remote Sense in CCM

The HS_FET on-time is determined by CCRCOT On-Time generator. When load current increases, V_{CS} increases, the steady-state COMP voltage also increases and makes V_{OUT} decrease, achieving AVP. A near-DC offset cancellation is added to the output of EA to cancel the inherent output offset of finite-gain current mode controller.

In RFM, HS_FET is turned on with constant t_{ON} when V_{CS} is lower than V_{COMP2}. Once HS_FET is turned off, LS_FET is turned on automatically. With Ringing-Free Technique, LS_FET allows only partial negative current when the inductor free-wheeling current reaches negative. The switching frequency will be proportionately reduced, thus the conduction and switching losses will be greatly reduced.

Output Voltage Droop Setting (with Temperature Compensation)

It's very easy to achieve Active Voltage Positioning (AVP) by properly setting the error amplifier gain due to the native droop characteristics. The target is to have

$$V_{OUT} = V_{DAC} - I_{LOAD} \times R_{DROOP} \quad (9)$$

, then solving the switching condition $V_{COMP} = V_{CS}$ in Figure 7 yields the desired error amplifier gain as

$$A_V = \frac{R2}{R1} = \frac{A_I \times R_{SENSE}}{R_{DROOP}} \quad (10)$$

where A_I is the internal current sense amplifier gain. R_{SENSE} is the current sense resistor. If no external sense resistor present, it is the DCR of the inductor. R_{DROOP} is the resistive slope value of the converter output and is the desired static output impedance.

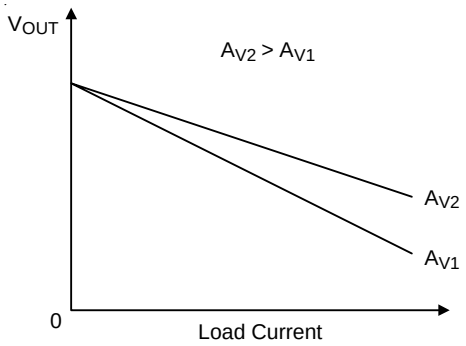


Figure 8. Error Amplifier Gain (A_V) Influence on V_{OUT}

As shown in Figure 9, when DCR sensing network is used for NTC thermistor temperature compensation, the error amplifier gain can be calculated as :

$$A_V = \frac{Z2}{Z1} = \frac{A_I \times R_{SENSE}}{R_{DROOP}} \times K \quad (11)$$

where K is the dividing ratio of DCR sensing as shown below :

$$K = \frac{Z2}{Z1 + Z2} \quad (12)$$

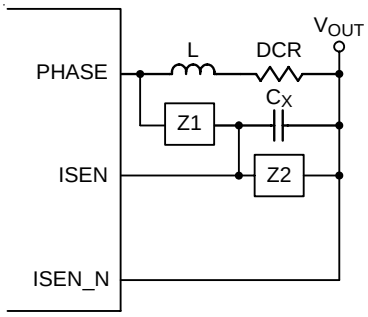


Figure 9. Using an NTC Thermistor at DCR Sensing Network

Loop Compensation

Optimized compensation of the RT8153C/D allows for best possible load step response of the regulator's output. A compensator with one pole and one zero is adequate for a proper compensation. Figure 7 shows the compensation circuit. Prior design procedure shows how to determine

the resistive feedback components of error amplifier gain. The C1 and C2 must be calculated for the compensation. The target is to achieve constant resistive output impedance over the widest possible frequency range.

The pole frequency of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2 \times \pi \times C \times R_C} \quad (13)$$

where C is the capacitance of output capacitor and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{C \times R_C}{R2} \quad (14)$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching-related noise, such that,

$$C1 = \frac{1}{(R1b + R1a // R_{NTC,\ 25}) \times \pi \times f_{SW}} \quad (15)$$

TON Setting

High frequency operation optimizes the application for the smaller component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low frequency operation offers the best overall efficiency at the expense of component size and board space. Figure 10 shows the On-Time setting circuit. Connect a resistor (R_{TON}) between VIN and TON to set the on-time of UGATE:

$$t_{ON} = \frac{14.5 \times 10^{-12} \times R_{TON} \times 2}{(V_{IN} - V_{DAC})} \quad (16)$$

where t_{ON} is UGATE turn on period, V_{IN} is input voltage of converter, V_{DAC} is DAC voltage.

On-time translates only roughly to switching frequencies. The on-times guaranteed in the Electrical Characteristics are influenced by switching delays in external HS-FET. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in CCM (DPRSLPVR = 0) and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, PHASE goes high earlier than normal, extending the on-time by a period equal to the HS-FET rising dead time.

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{S(MAX)} = \frac{1}{t_{ON} - t_{HS\text{-}Delay}} \times \frac{V_{DAC(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS\text{-}FET} + DCR_L - R_{DROOP}\right]}{V_{IN(MAX)} + I_{LOAD(MAX)} \times \left[R_{ON\_LS\text{-}FET} - R_{ON\_HS\text{-}FET}\right]} \quad (17)$$

where

- fs_{MAX} is the maximum switching frequency
- $t_{HS\text{-}Delay}$ is the turn on delay of HS-FET
- $V_{DAC(MAX)}$ is the maximum VDAC of application
- V_{INMAX} is the maximum application Input voltage
- $I_{LOAD(MAX)}$ is the maximum load of application
- $R_{ON\_LS\text{-}FET}$ is the Low side FET $R_{DS(ON)}$
- $R_{ON\_HS\text{-}FET}$ is the High side FET $R_{DS(ON)}$
- DCR_L is the inductor DCR
- R_{DROOP} is the load line setting

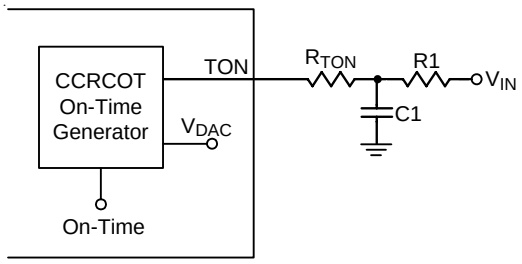


Figure 10. On-Time setting with RC Filter

Soft-Start and Mode Transition Slew Rates

The RT8153C/D uses 3 slew rates for various modes of operation. The three slew rates are internally determined by commanding one of three bi-directional current sources (I_{SS}) into the SOFT pin. The 7 bit VID DAC and the precision voltage reference are referred to RGND for accurate remote sensing. Hence, connect a capacitor (C_{SOFT}) from SOFT pin to RGND for controlling the slew rate as shown in Figure 7. The capacitance of capacitor is restricted to be larger than 10nF. The voltage (V_{SOFT}) on the SOFT pin is the reference voltage of the error amplifier and is, therefore, the commanded system voltage.

The first current is typically 20μA used to charge or discharge the C_{SOFT} during soft-start, and soft-shutdown.

The second current is typically 50μA used during other voltage transitions, including VID change and transitions between operation modes. The third current is typically 100μA used during Render DEM with VID change up transitions.

The IMVP–6.5 specification specifies the critical timing associated with regulating the output voltage. The symbol, SLEWRATE, as given in the IMVP–6.5 specification will determine the choice of the SOFT capacitor, $C_{SOFT,}$ by the following equation :

$$C_{SOFT} = \frac{I_{SS}}{SLEWRATE} \quad (18)$$

Power Up Sequence

When the controller's VCC voltage rises above the UVLO threshold (typ. 4.3V), the power up sequence begins when VRON goes high. If $\overline{CLKEN}$ = 1 (Pull High), the RT8153C/D will enter CPU mode power-up sequence. If $\overline{CLKEN}$ = 0 (Connect to GND), the controller will enter Render mode power up sequence.

After the RT8153C/D enters CPU mode, VSEN starts ramping up to V_{BOOT} within 1ms. The slew rate during power-up is 20μA/C_{SOFT}. The RT8153C/D pulls $\overline{CLKEN}$ low after VSEN gets across V_{BOOT} – 0.1V for 73μs. Right after $\overline{CLKEN}$ goes low, VSEN starts ramping to first V_{DAC} value. After $\overline{CLKEN}$ goes low for approximately 4.7ms, PGOOD is asserted HIGH. DPRSLPVR is valid right after PGOOD is asserted. UVP is masked as long as VSEN is less than V_{BOOT} – 0.1V.

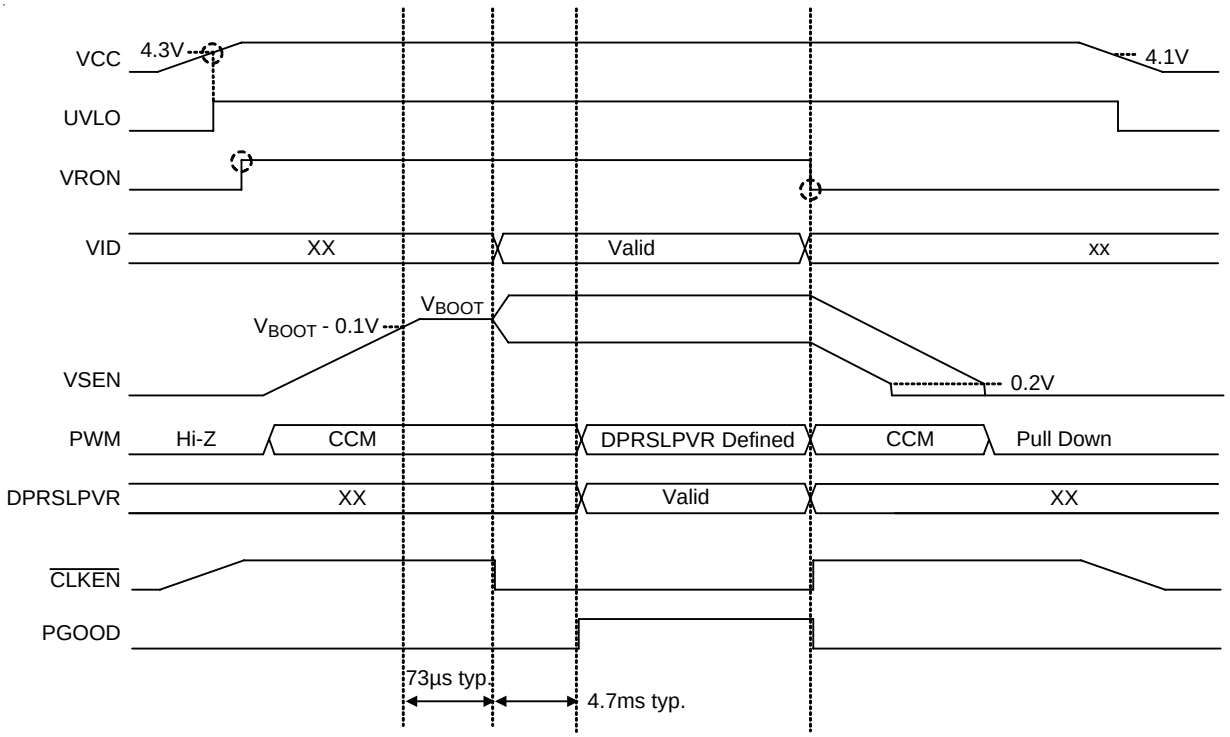


Figure 11. CPU Mode Timing Diagram for Power Up and Power Down

After the RT8153C/D enters Render mode, VSEN starts ramping up to VDAC within 1ms. The slew rate during power-up is 20μA/C_{SOFT}. PGOOD is asserted HIGH after VSEN exceeds VDAC – 100mV for 4.77ms (typ.). DPRSLPVR is valid right after PGOOD is asserted. UVP is masked as long as VSEN is less than VDAC – 100mV.

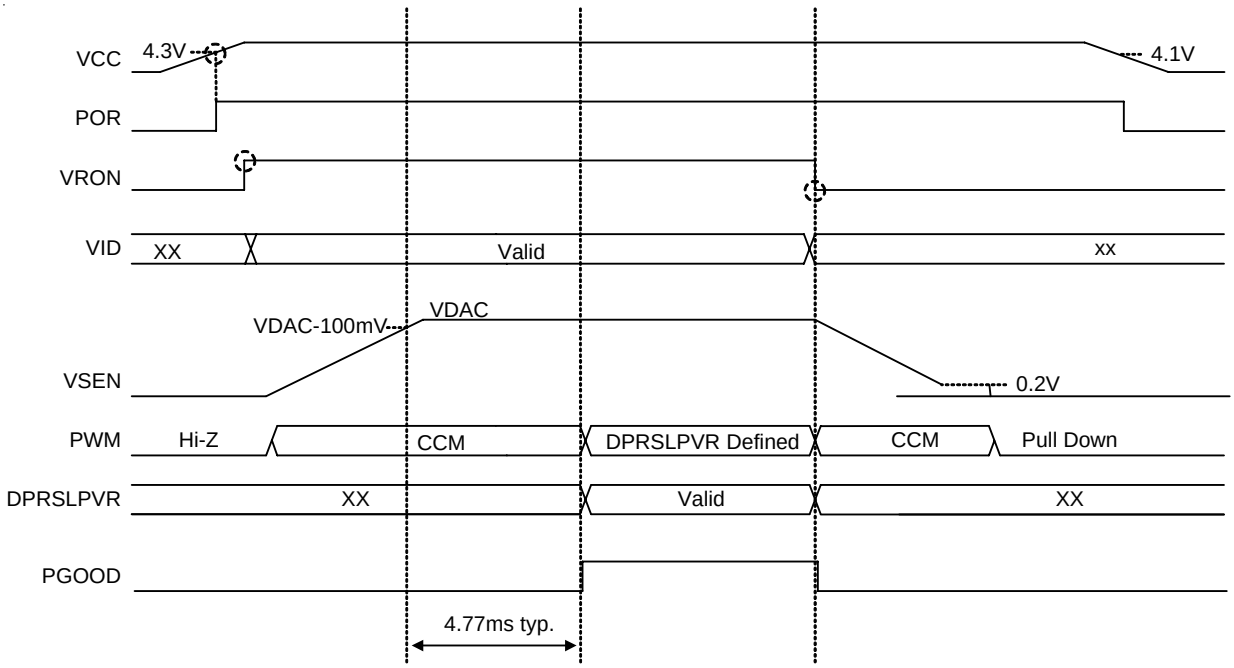


Figure 12. Render Mode Timing Diagram for Power Up and Power Down

Power Down

When VRON goes low, the RT8153C/D enters low power shutdown mode. PGOOD is pulled low immediately and the V_{SOFT} ramps down with slew rate of 20μA/C_{SOFT}. VSEN also ramps down following V_{SOFT}. After V_{VSEN} is lower than 200mV, the RT8153C/D turns off high side FETs and low side FETs. An internal discharge resistor at VSEN will be enabled and the analog part will be turned off.

Deeper Sleep Mode Transitions

After DPRSLPVR goes high, the RT8153C/D enters deeper sleep mode operation. If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target V_{SOFT} still ramps as before, and UVP, OCP and OVP are masked for 73μs.

Over Current Protection Setting

The RT8153C/D compares a programmable current limit set point to the voltage from the current sense amplifier output for over current protection (OCP). The voltage applied to OCSET pin defines the desired current limit threshold I_{LIM} :

$$V_{OCSET} = 48 \times I_{LIM} \times R_{SENSE} \quad (19)$$

Connect a resistive voltage divider from VCC to GND, with the joint of the voltage divider connected to OCSET pin as shown in Figure 13. For a given R_{OC2}, then

$$R_{OC1} = R_{OC2} \times \left(\frac{V_{CC}}{V_{OCSET}} - 1 \right) \quad (20)$$

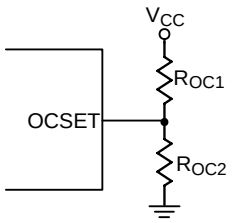


Figure 13. OCP Setting Without Temperature Compensation

The RT8153C/D provides current limit function and over current protection. The current limit function is triggered when inductor current exceeds the current limit threshold, I_{LIM}, defined by V_{OCSET}. When current limit function is tripped, high side MOSFET will be forced off until the over current condition is cleared.

If the current limit function is triggered for 15 switching cycles, OCP will be tripped. Once OCP is tripped, both high side and low side MOSFET will be turned off, and the internal discharge resistor at the VSEN pin will be enabled to discharge output capacitors. OCP is a latched protection, it can only be reset by cycling VRON or VCC.

Over Voltage Protection (OVP)

The OVP circuit is triggered under two conditions (without offset mode):

- Condition 1 : When V_{VSEN} exceeds 1.7V.
- Condition 2 : When V_{VSEN} exceeds V_{DAC} by 300mV (typ.).

When offset mode, the relative over voltage protection is disable and the over circuit is triggered until V_{VSEN} exceeds 2V.

If either condition is valid, the RT8153C/D latches the LGATE = 1 and UGATE = 0 as crowbar to the output voltage of VR. Turning on all LS_FETs can lead to very large reverse inductor current and potentially result in negative output voltage of VR. To prevent the CPU from damage by negative voltage. The RT8153C/D turns off all LS_FETs when V_{VSEN} falls below –100mV.

Under Voltage Protection (UVP)

If V_{VSEN} is lower than V_{DAC} by 400mV (typ.) a UVP fault will be tripped. Once UVP is tripped, both high side and low side MOSFET will be turned off and the internal discharge resistor at VSEN pin will be enabled. UVP is a latched protection; it can only be reset by cycling VRON or VCC.

Negative Voltage Protection (NVP)

During the state when V_{VSEN} is lower than –100mV, the controller will force LGATE = 0 and UGATE = 0 to prevent negative voltage. Once V_{VSEN} recovers to be higher than 0V, NVP will be suspended and LGATE = 1 will be enabled again.

Over Temperature Protection (OTP)

Over Temperature Protection prevents the VR from damage. OTP is considered to be the final protection stage against overheating of the VR. The thermal throttling $\overline{VRTT}$ is set to be asserted prior to OTP to manage the VR power. When this measure becomes insufficient to keep the die temperature of the controller below the OTP threshold, OTP will be asserted and latched. The die temperature of the controller is monitored internally by a temperature sensor. As a result of OTP triggering, a soft shutdown will be launched and V_{VSEN} will be monitored. When V_{VSEN} is less than 200mV, the driver remains in high impedance state and the discharging resistor at VSEN pin will be enabled. A reset can be executed by cycling VCC or VRON.

Thermal Throttling Control

Intel IMVP-6.5 technology supports thermal throttling of the processor to prevent catastrophic thermal damage. The RT8153C/D includes a thermal monitoring circuit to detect an exceeded user-defined temperature on a VR point. The thermal monitoring circuit senses the voltage change across NTC pin. Figure 14 shows the principle of setting the temperature threshold. Connect an external resistive voltage divider between Vcc and GND. This divider uses a Negative Temperature Coefficient (NTC) thermistor and a resistor. The joint of the voltage divider is connected to the NTC pin in order to generate a voltage that is inversely proportional to temperature. The RT8153C/D pulls $\overline{VRTT}$ low if the voltage on the NTC pin is greater than 0.8 x V_{CC}. The internal $\overline{VRTT}$ comparator has a hysteresis of 200mV (typ.) to prevent high frequency $\overline{VRTT}$ oscillation when the temperature is near the setting point. The minimum assertion/de-assertion time for $\overline{VRTT}$ toggling is 1.6ms (typ.).

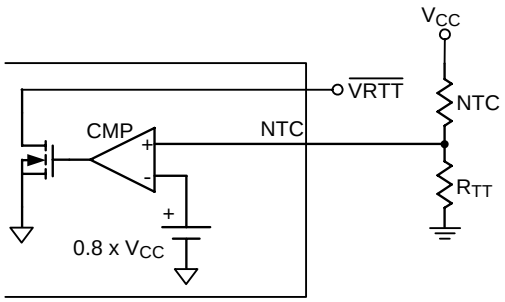


Figure 14. Thermal Throttling Setting Principle

Furthermore, this pin also provides load line enable/disable function in which the zero load line regulation can be implemented through NTC pin. The NTC pin will sink a 80µA current pulse inward the IC at VRON rising edge and the IC will detect the voltage of NTC pin at the same time to determine whether the zero load line function is enabled or not. Figure 15 is the recommended setting network of zero load line. The 100kΩ NTC resistor is recommended in this setting network for zero load line application and the resistance of R1 is set to be the same value as the resistor at 25°C. In addition, the resistance of both R2 and R3 can be obtained by solving the equations 21 and 22.

for 120°C

$$V_{NTC} = \frac{R3}{(R1//R_{NTCHT}) + R2 + R3} \times VCC = 4V \quad (21)$$

for – 20°C

$$V_{NTC} = \frac{R3}{(R1//R_{NTCLT}) + R2 + R3} \times VCC = 1.5V \quad (22)$$

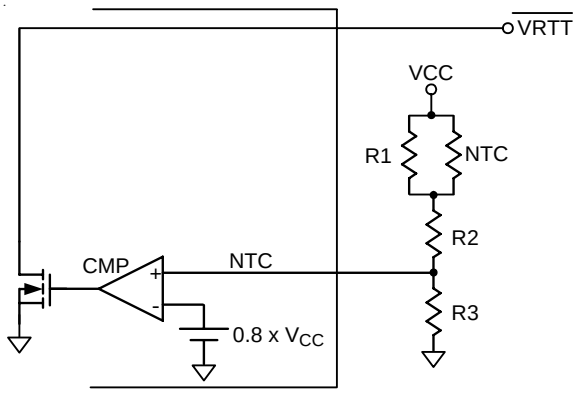


Figure15. For Zero Load Line Network

Current Monitor

Figure 16 shows the current monitor setting principle. Current monitor needs to meet IMVP6.5 specification. The RT8153C/D is based on the relation between R_{DROOP} and load current to provide an easy setting and high accuracy current monitor indicator.

The current monitor indication voltage, V_{CM}, is calculated as :

$$V_{CM} = \frac{16 \times I_{LOAD} \times DCR \times R_{CM}}{R_{CMSET}} \quad (23)$$

where I_{LOAD} is the output load current, DCR is the load line setting of applications, and R_{CM} and R_{CMSET} are the current monitor current setting resistors.

To find R_{CM} and R_{CMSET}, follow below equation :

$$\frac{R_{CM}}{R_{CMSET}} = \frac{V_{CM}}{16 \times I_{(MAX)} \times DCR} \quad (24)$$

V_{CM} must be kept equal to 1V and $I_{(MAX)}$ needs to follow the setting current of the IMVP6.5 definition with various CPU. V_{CM} is clamped not higher than 1.15V.

For an example of current monitor setting, the following design parameters are given :

$I_{(MAX)}$ = 30A, DCR = 1mΩ,

V_{CM} = 1V, R_{CMSET} = 10kΩ

⇒ R_{CM} = 20.8kΩ

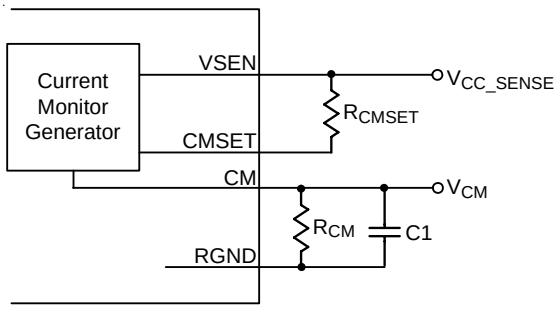


Figure 16. Current Monitor Setting Principle

When DCR sensing network is used for NTC thermistor temperature compensation, the current monitor indication voltage, V_{CM}, can be calculated as below :

$$V_{CM} = \frac{16 \times I_{LOAD} \times DCR \times R_{CM} \times K}{R_{CMSET}} \quad (25)$$

To find R_{CM} and R_{CMSET} follow below equation :

$$\frac{V_{CM}}{R_{CMSET}} = \frac{V_{CM(MAX)}}{16 \times I_{(MAX)} \times DCR \times R_{CM} \times K} \quad (26)$$

where, K is dividing ration of DCR sensing.

No Load Offset

The RT8153C/D feature no-load offset function which provides the possibility of wide range positive/negative offset. The no-load offset function can be implemented through OFS pin. To enable no-load offset function, the voltage of the OFS pin should be higher than 0.9V at the VRON raising edge. It is recommended to set the OFS pin at 1.2V before VRON rising edge. The no-load offset range can be from 400mV to –200mV while OFS pin voltage varying from 1.6V to 1V. The output offset voltage magnitude is equaled to the voltage difference between OFS pin and the 1.2V. For example, the OFS pin should be set to 1.4V if the target offset voltage is 200mV and OFS pin should be set to 1.1V to have –100mV output offset voltage. The accuracy of this offset voltage is ±10mV at no-offset point which OFS pin is 12V and the linearity of no-load offset function is higher than 95% in the 400mV

to –200mV range. Furthermore, the offset function has clamp mechanism to prevent the output voltage run-away. The lower limit of the offset function is –300mV which means the output offset voltage magnitude will keep exactly –300mV even if the OFS pin voltage is lower than 0.9V. In another hand, the upper limit of the offset function is about 600mV which means the output offset voltage magnitude will keep about 600mV even if the OFS pin voltage is higher than 1.8V.

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{I_{Ripple-MAX}} \times t_{ON} \quad (27)$$

where t_{ON} is the UGATE turn on period.

Higher inductance yields in less ripple current and hence in higher efficiency. The flaw is the slower transient response of the power stage to load transients. This might increase the need for more output capacitors driving the cost up. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to be saturated at the peak inductor current.

Output Capacitor Selection

Output capacitors are used to obtain high bandwidth for the output voltage beyond the bandwidth of the converter itself. Usually, the CPU manufacturer recommends a capacitor configuration. Two different kinds of output capacitors can be found including, bulk capacitors closely located to the inductors and ceramic output capacitors in close proximity to the load. Latter ones are for mid-frequency decoupling with especially small ESR and ESL values while the bulk capacitors have to provide enough stored energy to overcome the low frequency bandwidth gap between the regulator and the CPU.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8153C/D, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-32L 4x4 packages, the thermal resistance, θ_{JA}, is 52°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WQFN-32L 5x5 packages, the thermal resistance, θ_{JA}, is 36°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (36°C/W) = 2.778W for WQFN-32L 5x5 package

$P_{D(MAX)}$ = (125°C – 25°C) / (52°C/W) = 1.923W for WQFN-32L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8153C/D packages, the derating curves in Figure 17 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

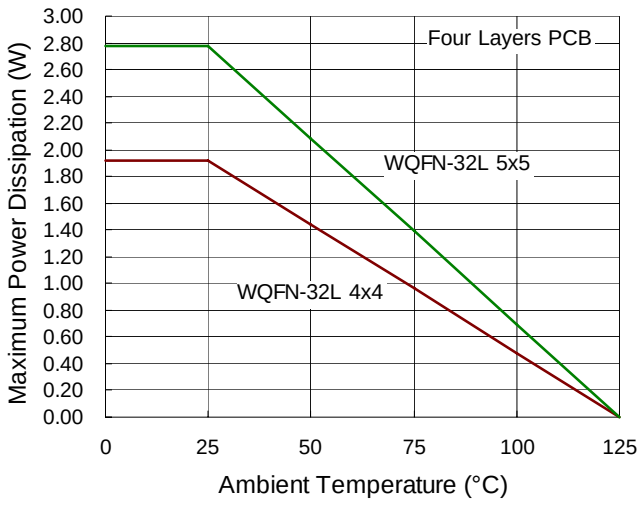


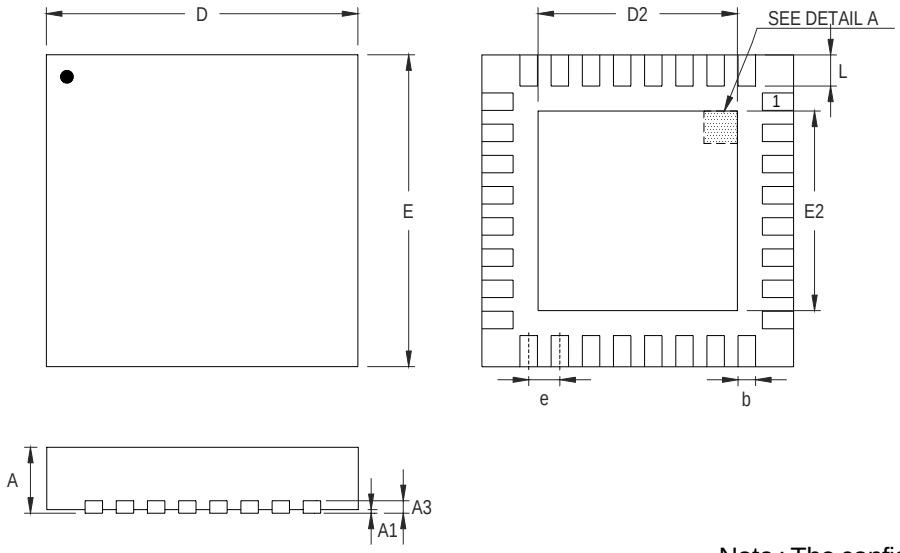
Figure 17. Derating Curve for RT8153C/D Package

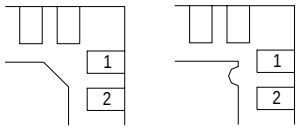
Layout Considerations

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for optimum PC board layout :

- Keep the high current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- The slew rate control capacitor should be connected from SOFT to RGND.
- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharging path.
- Place the current sense component close to the controller. ISEN and ISEN_N connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee the current sense accuracy. The PCB trace from the sense nodes to controller should be parallel to each other.
- Route high-speed switching nodes away from sensitive analog areas (SOFT, COMP, FB, VSEN, ISEN, ISEN_N, CM, etc...)

Outline Dimension





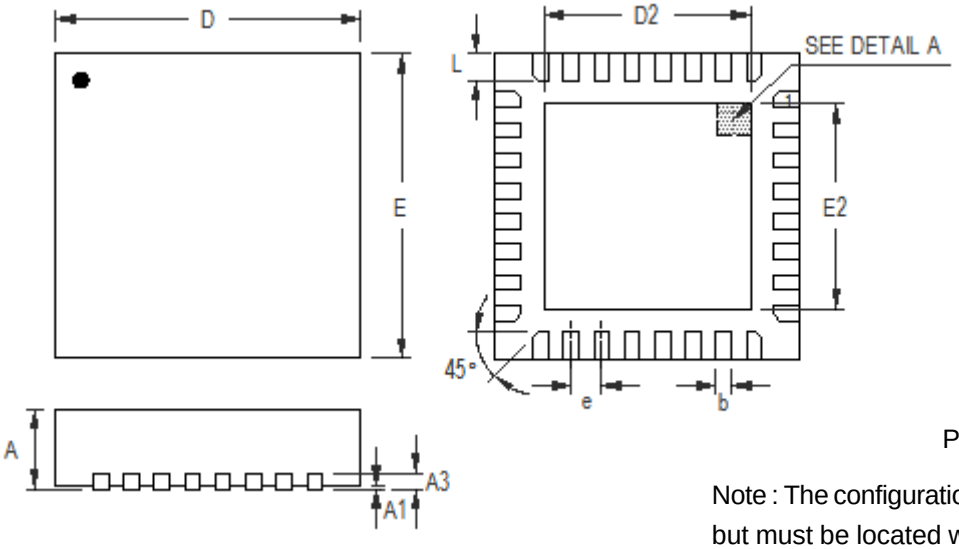
DETAIL A

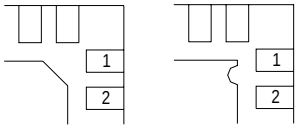
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

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