Dual-Output PWM Controller for AMD SVI Mobile CPU Power Supply

General Description

The RT8870A is a dual-output PWM controller for AMD SVI mobile CPU power supply. The RT8870A provides a two-phase PWM controller to power the CPU Core (VDD) and a single-phase PWM controller to power the Northbridge portion of the CPU (VDDNB). This part has three integrated MOSFET drivers and is fully compliant with AMD Voltage Regulator Specification to meet AMD's mobile CPU power supply requirements.

The RT8870A features CCRCOT (Constant Current Ripple Constant On-Time) control with G-NAVP™ (Green-Native AVP), which is a Richtek proprietary topology. The CCRCOT control provides superior output voltage ripple performance over the entire input/output range. G-NAVP™ makes this device an easy setting controller to meet the droop requirement for all AMD mobile CPUs. The droop is easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient response can achieve optimized AVP performance. The droop function is selectable for both VDD and VDDNB outputs. The RT8870A uses Serial VID Interface (SVI) for individual controller output voltage and operation mode programming. A built-in high-accuracy DAC converts the serial VID code for output voltage ranging from 0.5V to 1.55V with up to 0.8% system accuracy. This device supports VID on-the-fly and operation mode transition on-the-fly functions that are fully compliant with the AMD specification. Both VDD and VDDNB controllers provide diode emulation mode to improve efficiency at light load condition.

The RT8870A supports inductor DCR and sense resistor current sensing. It also provides power good indication and complete fault protection functions, including over voltage, out-of-spec, negative voltage, over current and under voltage lockout thermal shutdown.

The RT8870A is available in a WQFN-40L 5x5 small footprint package.

Features

- **Dual-Output PWM Controller for AMD CPU Core and NB Power**
- **G-NAVP™ (Green-Native AVP)**
- **Constant Current Ripple Constant-On-Time (CCRCOT) Control**
- **Fast Line/Load Transient Response**
- **Integrated MOSFET Drivers**
- **0.8% DAC Accuracy**
- **Serial VID Interface (SVI)**
  - **Two-Wire Clock and Data Bus**
  - **High Speed I^2C**
  - **7-bit DAC : 0.5V to 1.55V with 12.5mV Step**
- **Support Power Saving Mode (PSI_L)**
  - **Phase Shedding and Diode Emulation in VDD Output**
  - **Diode Emulation in VDDNB Output**
- **Support VFIX Mode**
- **Selectable Droop Function**
- **Differential Remote Voltage Sensing**
- **Accurate Current Balance**
- **Digital Soft-Start/ Soft-Shutdown for All Outputs**
- **OVP, Out-Of-Spec, NVP, OCP, OTP and UVLO**
- **40-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- AMD SVI Mobile CPU
- Laptop Computer

Ordering Information

RT8870A□□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Operating Temperature Range
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

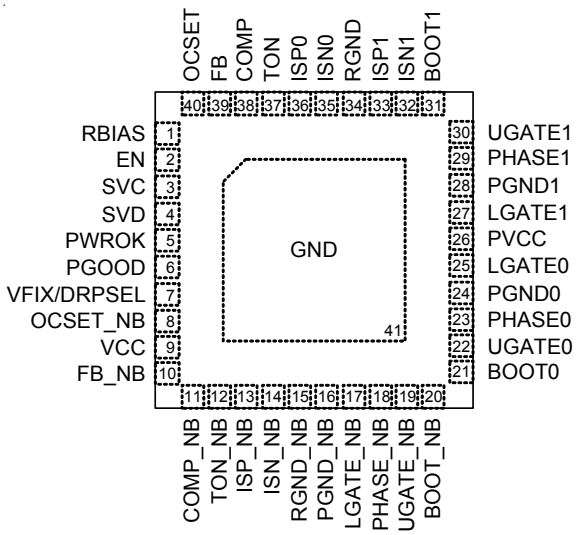
Marking Information

RT8870AGQW : Product Number

YMDNN : Date Code

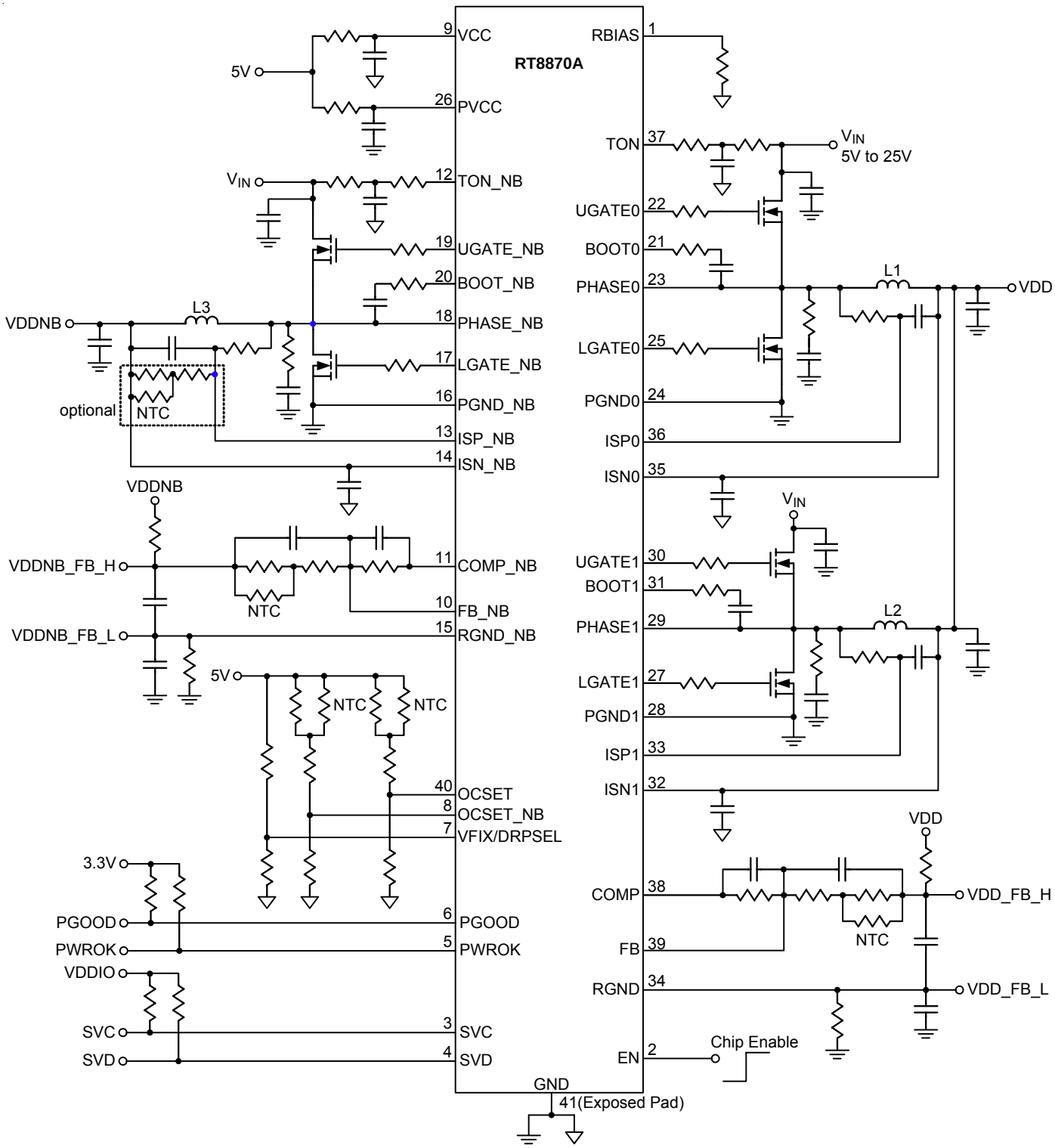
Pin Configurations

(TOP VIEW)



WQFN-40L 5x5

Typical Application Circuit



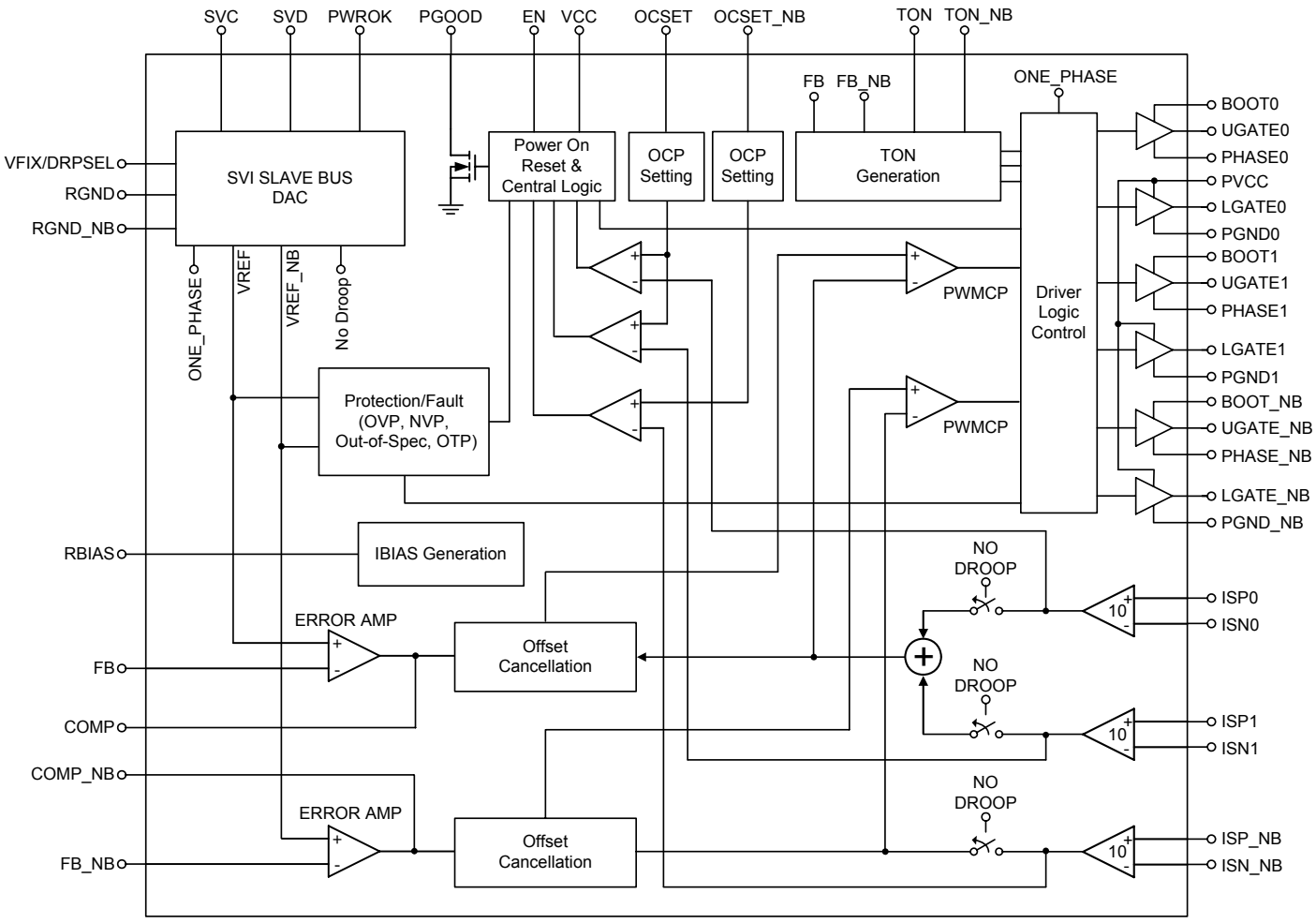
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	RBIAS	Internal Current Bias Setting Pin. Connect a 100kΩ resistor from this pin to GND to generate bias current for controller internal circuit. Place this 100kΩ resistor as close to the RBIAS pin as possible.
2	EN	Controller EN Pin. A logic high signal enables the controller.
3	SVC	Serial VID Clock Input from Processor. This pin has an open-drain output.
4	SVD	Serial VID Data Input from Processor. This pin has an open-drain output.
5	PWROK	System Power Good Input Pin. If PWROK is low, the SVI interface is disabled and the DAC decodes SVC and SVD inputs to determine the boot VID. If PWROK is high, the SVI interface is running and the DAC decodes the received serial VID codes to determine the output voltage.
6	PGOOD	Power Good Indication Pin. This pin has an open-drain output and is typically tied to 3.3V through a 2kΩ resistor.
7	VFIX/DRPSEL	VFIX Mode, Droop Disable and Protection Selection Pin. Controller detects this pin voltage at the EN signal rising edge to determine the droop function, VFIX mode, and protection level setting. Use a resistive voltage-divider to set the pin voltage. If this pin is tied to 5V, controller operates in VFIX mode without droop. If this pin is tied to 3V, controller operates in droop disabled mode with normal protection threshold. If this pin is tied to 2V, controller operates in droop disabled mode with relaxed protection threshold. If this pin is tied to 1V, controller operates in droop enabled mode with relaxed protection threshold. If this pin is tied to GND, controller operates in droop enabled mode with normal protection threshold.
8	OCSET_NB	VDDNB Over Current Protection Threshold Setting Pin. Use a resistive voltage divider to ground and connect the joint of the voltage divider to this pin to set the voltage, V_{OCSET_NB}. V_{OCSET_NB} sets the over current threshold, I_{LIMIT_NB}, for VDDNB output.
9	VCC	Controller Power Supply Pin. Connect this pin to 5V with 0.1μF or greater ceramic capacitor for decoupling.
10	FB_NB	Output Voltage Feedback of VDDNB Controller. This pin is the negative input of the error amplifier for the VDDNB controller.
11	COMP_NB	Error Amplifier Output Pin of Northbridge VDD_NB Controller.
12	TON_NB	VDDNB Controller On-Time Setting Pin. Connect this pin to the converter input voltage, V_{IN}, through a resistor, R_{TONNB}, to set the on-time of UGATE_NB and also the output voltage ripple of VDDNB.
13	ISP_NB	Positive Input of Current Sense Amplifier for VDDNB Controller.
14	ISN_NB	Negative Input of Current Sense Amplifier for VDDNB Controller.
15	RGND_NB	Return Ground of VDDNB. This pin is the negative input of output voltage differential remote sense for VDDNB.
16	PGND_NB	Return Ground of Low Side MOSFET Gate Driver for VDDNB Controller.
17	LGATE_NB	Low Side MOSFET Gate Driver Output for VDDNB Controller. Connect this pin to the gate of the low side MOSFET for VDDNB.
18	PHASE_NB	Switching Node of VDDNB VR. Connect this pin to the VDDNB switching node. This pin is also the floating drive return of the high side MOSFET gate driver. The PHASE_NB voltage is sensed for zero current detection when low side MOSFET is on.
19	UGATE_NB	High Side MOSFET Gate Driver Output for VDDNB Controller. Connect this pin to the gate of the high side MOSFET for VDDNB.

To be continued

Pin No.	Pin Name	Pin Function
20	BOOT_NB	Power Supply of High Side MOSFET Gate Driver for VDDNB Controller. Connect this pin to the PHASE_NB pin with 0.1μF or greater ceramic capacitor for floating drive.
21	BOOT0	Power Supply for Phase 0 High Side MOSFET Gate Driver of VDD Controller. Connect this pin to the PHASE0 pin with 0.1μF or greater ceramic capacitor for floating drive.
22	UGATE0	Phase 0 High Side MOSFET Gate Driver Output of VDD controller. Connect this pin to the gate of phase 0 high side MOSFET for VDD.
23	PHASE0	Phase 0 Switching Node of VDD Controller. Connect this pin to the phase 0 switching node. This pin is also the floating drive return of the phase 0 high side MOSFET gate driver. The PHASE0 voltage is sensed for zero current detection when phase 0 low side MOSFET is on.
24	PGND0	Return Ground of Phase 0 Low Side MOSFET Gate Driver for VDD Controller.
25	LGATE0	Phase 0 Low Side MOSFET Gate Driver Output for VDD Controller. Connect this pin to the gate of phase 0 low side MOSFET for VDD.
26	PVCC	MOSFET Gate Driver Power Supply Input Pin. Connect this pin to 5V. Place a 1μF or greater decoupling capacitor close to this pin and locate it on the same PCB side as the controller.
27	LGATE1	Phase 1 Low Side MOSFET Gate Driver Output for VDD Controller. Connect this pin to the gate of phase 1 low side MOSFET for VDD.
28	PGND1	Return Ground of Phase 1 Low Side MOSFET Gate Driver for VDD Controller.
29	PHASE1	Phase 1 Switching Node of VDD Controller. Connect this pin to the phase 1 switching node. This pin is also the floating drive return of the phase 1 high side MOSFET gate driver.
30	UGATE1	Phase 1 Low Side MOSFET Gate Driver Output for VDD Controller. Connect this pin to the gate of phase 1 low side MOSFET for VDD.
31	BOOT1	Power Supply for Phase 1 High Side MOSFET Gate Driver of VDD Controller. Connect this pin to the PHASE1 pin with 0.1μF or greater ceramic capacitor for floating drive.
32	ISN1	Phase 1 Negative Input of Current Sense Amplifier for VDD Controller.
33	ISP1	Phase 1 Positive Input of Current Sense Amplifier for VDD Controller.
34	RGND	Return Ground of VDD Output. This pin is the negative input of output voltage differential remote sense for VDD.
35	ISN0	Phase 0 Negative Input of Current Sense Amplifier for VDD Controller.
36	ISP0	Phase 0 Positive Input of Current Sense Amplifier for VDD Controller.
37	TON	VDD Controller On-Time Setting Pin. Connect this pin to the converter input voltage, V_{IN}, through a resistor, R_{TON}, to set the on-time of UGATE0 and UGATE1 and also the output voltage ripple of VDD.
38	COMP	Error Amplifier Output Pin of Northbridge VDD Controller.
39	FB	Output Voltage Feedback of VDD Controller. This pin is the negative input of error amplifier for VDD controller.
40	OCSET	VDD Over Current Protection Threshold Setting Pin. Use a resistive voltage divider to ground and connect the joint of the voltage divider to this pin to set the voltage, V_{OCSET}. V_{OCSET} sets the over current threshold, I_{LIMIT}, for VDD total output current.
41 (Exposed Pad)	GND	Return Ground of Controller. The exposed pad must be soldered to a large PCB and connected to PGND for maximum thermal dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- RGND, PGND to GND ---------- –0.3V to 0.3V
- PWROK, EN, SVC, SVD, VFIX/DRPSEL, PGOOD, FB, COMP, FB_NB, COMP_NB, OCSET, OCSET_NB, ISPx, ISNx, ISP_NB, ISN_NB, TON, TON_NB and RBIAS to GND ---------- –0.3V to (V_{CC} + 0.3V)
- PVCC to PGND ---------- –0.3V to 6.5V
- BOOT to PHASE ---------- –0.3V to 6.5V
- PHASE to GND
  - DC ---------- –0.3V to 28V
  - <20ns ---------- –8V to 32V
- UGATE to PHASE
  - DC ---------- –0.3V to (BOOT – PHASE)
  - <20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to (PVCC – 0.3V)
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-40L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  - WQFN-40L 5x5, θ_{JA} ---------- 36°C/W
  - WQFN-40L 5x5, θ_{JC} ---------- 6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM ---------- 2kV
  - MM ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{CC} ---------- 4.5V to 5.5V
- Input Voltage, V_{IN} ---------- 6V to 24V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = V_{PVCC} = 5V, V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	$I_{VCC+PVCC}$	V_{EN} = 3.3V, Not Switching	--	--	10	mA
Shutdown Current	$I_{VCC+PVCC}$	V_{EN} = 0V	--	--	1	μA
Soft-Start/Soft-Shutdown Slew Rate Control						
Soft-Start / Soft-Shutdown Voltage Transition	SR_{SS}		1.25	1.875	2.5	mV/μs

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VID On-The-Fly Transition	SR_{DVID}		5	7.5	10	mV/μs
Reference and DAC						
DC Accuracy	V_{FB}	VID = 0.7500V to 1.5500V (No Load, Active Mode)	–0.8	0	0.8	%VID
		VID = 0.5000V to 0.7375V (No Load, Active Mode)	–7.5	0	7.5	mV
System Accuracy		VID = 0.7500V to 1.5500V No Load, Closed Loop, Active Mode	–1.5	0	1.5	%
		VID = 0.5000V to 0.7375V No Load, Closed Loop, Active Mode	–11.5	0	11.5	mV
Error Amplifier						
Input Offset Voltage	V_{OSEA}		–2	--	2	mV
DC Gain		R_{LOAD} = 47kΩ (Note 5)	70	80	--	dB
Gain-Bandwidth Product	G_{BW}	C_{LOAD} = 5pF (Note 5)	--	10	--	MHz
Slew Rate	S_R	C_{LOAD} = 10pF, gain = –4, R_{LOAD} = 47kΩ, V_{COMP} = 0.5V to 3V	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_{LOAD} = 47kΩ	0.5	--	3.6	V
MAX Source Current	$I_{OUTEAsr}$	V_{COMP} = 2V	--	250	--	μA
MAX Sink Current	$I_{OUTEAsk}$		--	20	--	mA
Current Sense Amplifier						
Input Offset Voltage	V_{OSCS}		–1	--	1	mV
Impedance at Negative Input	R_{ISN}		1	--	--	MΩ
Impedance at Positive Input	R_{ISP}		1	--	--	MΩ
DC Gain	A_I		--	10	--	V/V
Input Range	V_{ISN_IN}		–30	--	50	mV
TON Setting						
TON Pin Output Voltage	V_{TON}	R_{TON} = 80kΩ, V_{TON} = VID = 0.75V	–5	0	5	%
DEM On-Time Setting	t_{ON}	I_{RTON} = 80μA	--	350	--	ns
RTON Current Range	I_{TON}		25	--	280	μA
NB Minimum Off-Time	$t_{OFF-MIN\_NB}$		--	400	--	ns
Core Minimum Off-Time	$t_{OFF-MIN\_CORE}$		--	270	--	ns
Protection						
POR (Power-On Reset) Threshold	V_{PORH}	VCC Rising	--	4.35	4. 5	V
	V_{PORL}	VCC Falling	--	4.1	--	V
Absolute Over Voltage Protection Threshold	V_{ABSOVP}	(With Respect to 1.8V, ±50mV)	1.775	1.8	1.825	V
Out-of-Spec Relative Over Voltage Protection Threshold	V_{ROVP}	(With Respect to VID, ±47mV)	203	250	297	mV
Out-of-Spec Relative Under Voltage Threshold	V_{RUVP}	(With Respect to VID, ±55mV)	–245	–300	–355	mV

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Negative Voltage Protection Threshold		V_{NVP}		–100	-70	--	mV
Negative Voltage Protection Hysteresis		ΔV_{NVP}		--	50	--	mV
Current Limit Threshold Voltage (per phase)		V_{ILIMIT}	$V_{ILIMIT} = V_{ISPx} - V_{ISNx}$, V_{OCSET} = 2.1V	31.5	35	38.5	mV
Thermal Shut-Down Threshold		T_{SD}		--	160	--	°C
Thermal Shut-Down Hysteresis		ΔT_{SD}		--	10	--	°C
Logic Inputs							
EN Input Threshold Voltage	Logic-High	V_{IH}	With Respect to 3.3V	2	--	--	V
	Logic-Low	V_{IL}	With Respect to 3.3V	--	--	0.8	V
EN Leakage Current				–1	--	1	μA
PWROK Input Threshold Voltage		V_{IH_PWROK}		2	--	--	--
		V_{IL_PWROK}		--	--	0.8	--
Power Good							
PGOOD Low Voltage		V_{PG_L}	I_{PGOOD} = 4mA	--	--	0.5	V
PGOOD Soft-Start Delay		t_{PGD}	Delay Time After $V_{ISN0} = V_{BOOT}$ –100mV	--	700	--	μs
SVI Interface							
SVC, SVD Input Threshold Voltage	Logic-High	V_{IH_SVC}, V_{IH_SVD}		1	--	--	V
	Logic-Low	V_{IL_SVC}, V_{IL_SVD}		--	--	0.6	V
Schmitt Trigger Input Hysteresis		V_{HYS}		0.19	--	0.23	V
SVD Low-Level Output Voltage		V_{SVD}	Sink Current = 3mA	--	--	0.285	--
SVC, SVD Leakage			V_{EN} = 0V	--	--	±100	μA
			V_{EN} = 3.3V	--	0	--	μA
MOSFET Gate Driver							
Upper Driver Source		R_{USOURC}	$V_{BOOT} - V_{PHASE}$ = 5V, $V_{BOOT} - V_{UGATE}$ = 1V	--	1	--	Ω
Upper Driver Sink		R_{USINK}	V_{UGATE} = 1V	--	1	--	Ω
Lower Driver Source		R_{LSOURC}	V_{PVCC} = 5V, $V_{PVCC} - V_{LGATE}$ = 1V	--	1	--	Ω
Lower Driver Sink		R_{LSINK}	V_{LGATE} = 1V	--	0.5	--	Ω
Upper Driver Source Current		I_{USOURC}	$V_{BOOT} - V_{PHASE}$ = 5V, V_{UGATE} = 2.5V	--	2	--	A
Upper Driver Sink Current		I_{USINK}	$V_{BOOT} - V_{PHASE}$ = 5V, V_{UGATE} = 2.5V	--	2	--	A
Lower Driver Source Current		I_{LSOURC}	V_{LGATE} = 2.5V	--	2	--	A
Lower Driver Sink Current		I_{LSINK}	V_{LGATE} = 2.5V	--	4	--	A
Internal Boost Charging Switch On-Resistance		R_{BOOT}	PVCC to BOOT	--	30	--	Ω

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RBIAS						
RBIAS Voltage	V_{RBIAS}	R_{RBIAS} = 100kΩ	1.975	2	2.025	V
VFIX/DRPSEL						
VFIX Mode			4.5	--	--	V
No Droop Setting Normal Protection Setting			52	--	--	% of V_{CC}
No Droop Setting Relaxed Protection Setting		ROVP Disabled, V_{RUVP} = −400mV, V_{ABSOVP} = 1.8V	32	--	48	% of V_{CC}
With Droop Setting Relaxed Protection Setting		ROVP Disabled, V_{RUVP} = −400mV, V_{ABSOVP} = 1.8V	12	--	28	% of V_{CC}
With Droop Setting Normal Protection Setting			0	--	8	% of V_{CC}

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

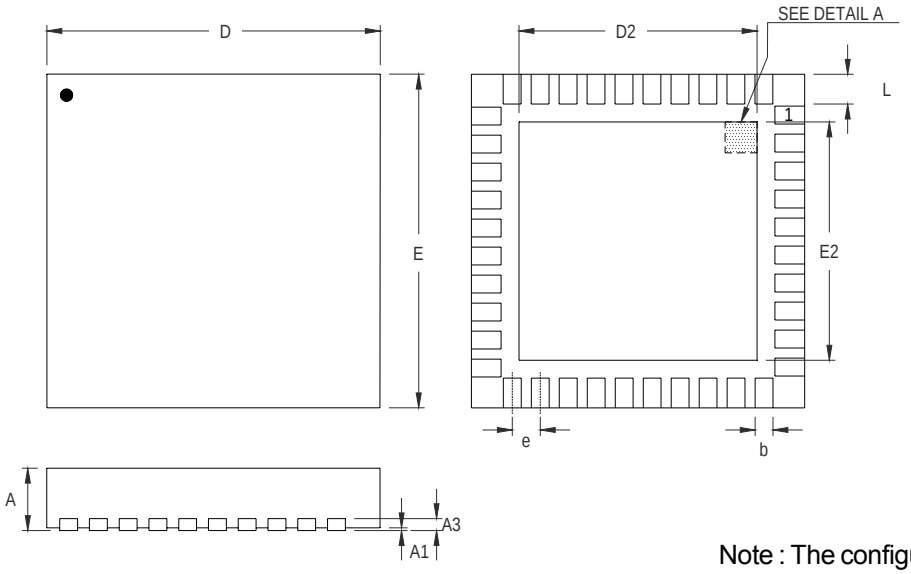
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

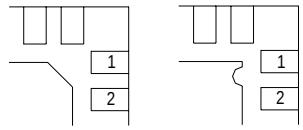
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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Datasheet Revision History

Version	Data	Page No.	Item	Description
P00	2010/7/26			First Edition