SINGLE PHASE, D-CAP+™ SYNCHRONOUS BUCK CONTROLLER WITH INTEGRATED DRIVERS FOR GENERAL IC V_{CORE}™ APPLICATIONS

Check for Samples: TPS51513

FEATURES

- **Minimum External Parts Count**
- **Includes Accurate Output Current Monitor with Programmable Clamp Voltage**
- **3-Bit DAC Selects 1 of 8 Output Voltages**
- **Custom VID Definition Available**
- **Supports *VID-on-the-Fly* Voltage Changes**
- **±8-mV V_{CORE} Accuracy Over Line/Load/Temp.**
- **Optimized Efficiency at Light and Heavy Loads**
- **Patented Output Overshoot Reduction (OSR™) Reduces Output Capacitance**
- **Accurate, Adjustable Voltage Positioning Including *No-Droop* Option**
- **Selectable 250/300/350/500 kHz Frequency**
- **Accurate, 8-level Selectable Current Limit**
- **3-V to 28-V Conversion Voltage Range**
- **Fast FET Driver w/Integrated Boost Diode**
- **5 mm × 5 mm, 32-Pin QFN PowerPAD™ Package**

APPLICATIONS

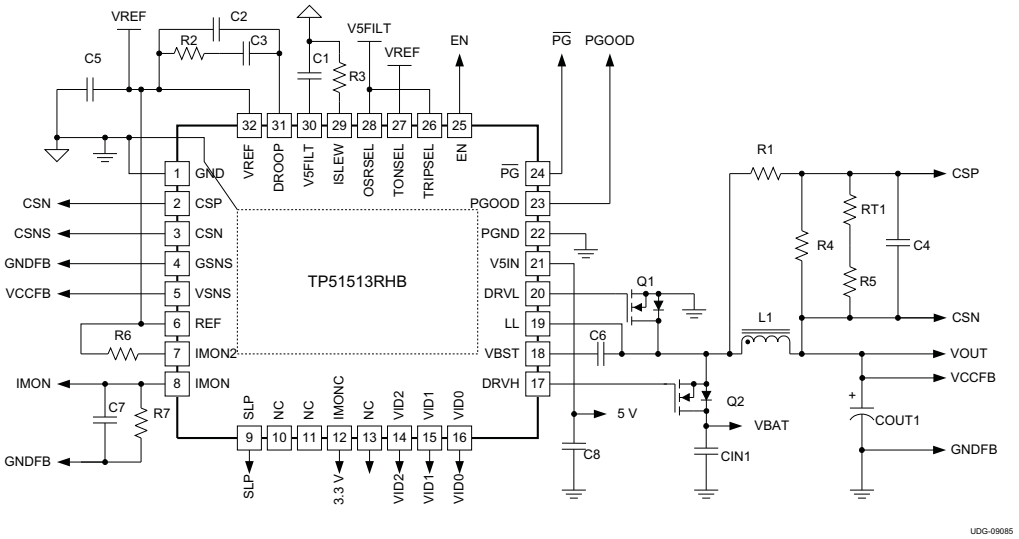
- **General IC V_{CORE} Applications**

DESCRIPTION

The TPS51513 is a single-phase synchronous buck controller with integrated gate drivers. Advanced control features such as the D-CAP+™ architecture and OSR™ overshoot reduction provide fast transient response, low output capacitance and high efficiency. The TPS51513 supports a wide range of IC V_{CORE} applications with an integrated 3-bit DAC. It also provides a full complement of signal I/O including a sleep mode control (SLP), two power good signals (PGOOD and $\overline{PG}$), and an analog current monitor (IMON). Logic inputs are compatible with either 1-V or 3.3-V logic levels. V_{CORE} slew rates are controlled with one resistor. In addition, the TPS51513 includes high-current FET gate drivers with an integrated P/N junction diode to drive N-channel FETs with low switching loss. The TPS51513 is available in the 5 mm × 5 mm, 32-pin QFN package and operates between –10°C and 100°C.

ORDERING INFORMATION

T_A	PLASTIC QFN (RHB)
–10°C to 100°C	TPS51513RHB (32-pin)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE / UNIT
Input voltage range(2)	VBST	–0.3 V to 36 V
	VBST to LL	–0.3 V to 6 V
	CSP, CSN, EN, IMON2, ISLEW, OSRSEL, REF, SLP, TONSEL, TRIPSEL, V5IN, V5FILT, VID0, VID1, VID2, VSNS	–0.3 V to 6 V
Output voltage range(2)	LL	–5.0 V to 30 V
	DRVH	–5.0 V to 36 V
	DRVH to LL	–0.3 V to 6 V
	DROOP, DRVL, IMON, IMON2 IMONC, $\overline{PG}$, PGOOD, VREF	–0.3 V to 6 V
	GSNS, PGND	–0.3 V to 0.3 V
Operating junction temperature, T_J		–40°C to +150°C
Storage temperature, T_{stg}:		–55°C to +150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATING TABLE (2 OZ. TRACE AND COPPER PAD WITH SOLDER)

PACKAGE	T_A< 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
32 pin RHB	2.94 W	29.4 mW / °C	1.17 W

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltages	Conversion voltage (no pin assigned)	3.0		28	V
	V5IN, V5FILT	4.5		5.5	
Voltage range, conversion pins	VBST	–0.1		34	V
	DRVH	–0.8		34	
	LL	–0.8		28	
Voltage range, 5-V pins	DRVL, OSRSEL, TONSEL, TRIPSEL	–0.1		5.5	V
Voltage range, 3.3-V pins	EN, IMON, IMONC, $\overline{PG}$, PGOOD, SLP, VID0, VID1, VID2	–0.1		3.6	V
Voltage range, low-voltage pins	CSN, CSP, DROOP, IMON2, ISLEW, REF, VREF, VSNS	–0.1		2.0	V
Ground pins	GSNS, PGND	–0.1		0.1	V
Operating free-air temperature, T_A		–10		100	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V5IN = V5FILT = 5.0V, GSNS = PGND = GND, VSNS = V_{CORE} (Unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: CURRENTS, UVLO AND POWER-ON RESET						
I_{V5}	V5IN + V5FILT supply current	VDAC < VSNS < VDAC + 100 mV, EN = 'HI'		2	4	mA
I_{V5STBY}	V5IN + V5FILT standby current	EN = 'LO'			10	μA
V_{UVLOH}	V5FILT UVLO 'OK' threshold	V5FILT = V5IN, VSNS < 200 mV, Ramp up; EN='HI'; Switching begins.	4.25	4.4	4.5	V
V_{UVLOL}	V5FILT UVLO fault threshold	V5FILT = V5IN, Ramp down; EN = 'HI', VSNS = 100 mV, Restart if 5 V dips below V_{POR} then rises > V_{UVLOH}, or EN is toggled with 5 V > V_{UVLOH}	4.0	4.2	4.3	V
V_{POR}	V5FILT fault latch reset threshold	V5FILT=V5IN, Ramp Down, EN='HI'. Can restart if 5 V goes up to V_{UVLOH} and no other faults present.	1.6	1.9	2.3	V
REFERENCES: DAC, VREF, VBOOT AND DRVL DISCHARGE						
V_{VIDSTP}	VID step size	Change VID0 HI to LO to HI		12.5		mV
V_{DAC1}	VSNS voltage range 1	0.75 V ≤ VSNS ≤ 1.25 V	–0.5%		0.5%	
V_{DAC2}	VSNS no voltage range 2	0.50V ≤ VSNS ≤ 0.75 V	–8		8	mV
V_{DAC3}	VSNS voltage range 3	0.30V ≤ VSNS ≤ 0.50 V	–12		12	mV
V_{DAC4}	VSNS voltage range 4	1.25V ≤ VSNS ≤ 1.50 V	–1%		1%	
V_{VREF}	VREF output voltage	4.5V ≤ V5FILT ≤ 5.5 V, IREF = 0 A	1.665	1.700	1.735	V
$V_{VREFSRC}$	VREF output source	IREF = 0 to 250 μA	–9	–3		mV
$V_{VREFSNK}$	VREF output sink	IREF = –250 μA to 0 μA		10	39	mV
$V_{DLDQDRVL}$	Discharge threshold	VSNS < 200 mV, DRVL goes high for 1 ms	200	250	325	mV
VOLTAGE SENSE: VSNS AND GSNS						
I_{VSNS}	VSNS input bias current	Not in Fault, Disable or UVLO		9	40	μA
I_{VSNSDQ}	VSNS input bias current, discharge	Fault, Disable or UVLO, VSNS = 100 mV	90	125	175	μA
I_{GSNS}	GSNS input bias current		–40	–8		μA
V_{DELGND}	GSNS differential			±300		mV
$A_{GAINGND}$	GSNS/GND gain		0.993	1	1.009	V/V
$V_{VSNSCOM}$	VSNS common mode dnput		–0.3		2	V

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V5IN = V5FILT = 5.0V, GSNS = PGND = GND, VSNS = V_{CORE} (Unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE: OVERCURRENT, ZERO CROSSING AND VOLTAGE POSITIONING						
I_{CS}	CS input bias current	CSP and CSN	–1.0		1.0	µA
V_{ZXOFF}	Zero crossing comp. internal offset	CSP–CSN	–1.5		0.7	mV
$G_{M-DROOP}$	Droop amplifier transconductance	VSNS = 1 V	485	500	519	µS
$V_{DCLAMPN}$	Droop amplifier clamp voltage	$V_{REF} – V_{DROOP}$		46		mV
$V_{DCLAMPP}$	Droop amplifier clamp voltage	$V_{DROOP} – V_{REF}$		600		mV
A_{CSINT}	Internal current sense gain	Gain from CSP - CSN to modulator	5.92	6	6.06	V/V
V_{OCPP}	OCP voltage set (Valley current limit)	TRIPSEL = GND; R_{SLEW} tied to GND	10.1	11.4	12.8	mV
		TRIPSEL = REF; R_{SLEW} tied to GND	12.9	14.0	15.4	
		TRIPSEL = 3.3 V; R_{SLEW} tied to GND	16.1	17.4	18.8	
		TRIPSEL = V5FILT; R_{SLEW} tied to GND	20.4	21.7	23.2	
		TRIPSEL = GND; R_{SLEW} tied to VREF	25.1	26.7	28.5	
		TRIPSEL = REF; R_{SLEW} tied to VREF	31.4	33.3	35.3	
		TRIPSEL = 3.3 V; R_{SLEW} tied to VREF	39.2	41.5	43.8	
		TRIPSEL = V5FILT; R_{SLEW} tied to VREF	50.4	53.1	55.7	
V_{OCPN}	Negative OCP voltage set (valley current limit)	TRIPSEL = GND; R_{SLEW} tied to GND	14.0	15.6	17.4	mV
		TRIPSEL = REF; R_{SLEW} tied to GND	17.2	19.0	20.4	
		TRIPSEL = 3.3 V; R_{SLEW} tied to GND	21.3	23.1	24.6	
		TRIPSEL = V5FILT; R_{SLEW} tied to GND	28.1	29.7	31.1	
		TRIPSEL = GND; R_{SLEW} tied to VREF	34.5	36.3	38.0	
		TRIPSEL = REF; R_{SLEW} tied to VREF	42.9	44.6	46.1	
		TRIPSEL = 3.3 V; R_{SLEW} tied to VREF	54.3	56.2	57.9	
		TRIPSEL = V5FILT; R_{SLEW} tied to VREF	67.6	69.4	71.2	
DRIVERS: HIGH-SIDE, LOW-SIDE, CROSS CONDUCTION PREVENTION AND BOOST RECTIFIER						
R_{DRVH}	DRVH on-resistance	VBST – LL = 5 V, 'HI' State VBST – VDRVH = 0.1 V		0.9	2.5	Ω
		VBST – LL = 5 V, 'LO' State VDRVH – VLL = 0.1 V		0.7	2.5	
I_{DRVH}	DRVH sink/source current(1)	DRVH forced to 2.5 V, VBST – LL forced to 5 V		2.2		A
t_{DRVH}	DRVH transition time	DRVH 10% to 90% or 90% to 10%, C_{DRVH} = 3 nF		15	25	ns
R_{DRVL}	DRVL on-resistance	'HI' State, V5IN – VDRVL = 0.1 V		0.7	2	Ω
		'LO' State, VDRVL – PGND = 0.1 V		0.45	1	
I_{DRVL}	DRVL Sink/Source current(1)	DRVL forced to 2.5 V, Source		2.7		A
		DRVL forced to 2.5 V, Sink		8		A
t_{DRVL}	DRVL transition time	DRVL 90% to 10%, CDRVL = 3 nF		12	25	ns
		DRVL 10% to 90%, CDRVL = 3 nF		12	25	
$t_{NONOVLP}$	Driver non-overlap time	LL falls to 1 V to DRVL rises to 1 V	15	19	25	ns
		DRVL falls to 1 V to DRVH rises to 1 V	22	27	35	
V_{FBST}	BST rectifier forward voltage	V5IN – VBST, IF=5 mA, T_A = 25°C	0.6	0.7	0.8	V
I_{BSTLK}	BST rectifier leakage current	V_{VBST} = 34 V, V_{LL}=28 V		0.1	1	µA

(1) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V5IN = V5FILT = 5.0V, GSNS = PGND = GND, VSNS = V_{CORE} (Unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OVERSHOOT REDUCTION (OSR) THRESHOLD SETTING						
V_{OSR}	OSR voltage set	V_{OSRSEL} = GND	85		133	mV
		V_{OSRSEL} = REF	119		170	
		V_{OSRSEL} = 3.3 V	163		220	
		V_{OSRSEL} = V5FILT; OSR is OFF		N/A		
V_{OSRHYS}	OSR voltage hysteresis(2)	All settings		20		mV
TIMERS: SLEW RATE, ISLEW, ON-TIME AND I/O TIMING						
$I_{SLEW\ 1}$	R_{SLEW} to GND current	R_{SLEW} = 125 kΩ from ISLEW to GND	9.9	10	10.15	µA
$I_{SLEW\ 2}$	R_{SLEW} to VREF current	R_{SLEW} = 45 kΩ from VREF to ISLEW	9.5	10	10.8	µA
$t_{STARTUP}$	VSNS startup time	I_{SLEW} = |10 µA|, No Faults, Time from EN to V_{SNS} = V_{VID} = 1.0	0.6		1.15	ms
$SL_{STRTSTP}$	VSNS slew soft-start / soft-stop	I_{SLEW} = |10 µA|, EN goes 'HI' (Soft-start) Non-OVP Fault = 'Soft-stop'	1.3	1.6	1.9	mV/µs
SL_{SLPE}	VSNS slew SLP exit	I_{SLEW} = |10 µA|, SLP goes low/high. Measure slew on SLP transition.	10	12.5	15	mV/µs
t_{PGDPO}	PGOOD power-on delay time	Time from $\overline{PG}$ going low to PGOOD going HI	3	6	9	ms
$t_{PGDDGLT}$	PGOOD deglitch time	Time from VSNS out of +200 mV/–300 mV VDAC boundary to PGOOD low.	50	100	160	µs
t_{ON}	On-time control	V_{TON} = GND, V_{LL}=12 V, VSNS=1 V	265	319	385	ns
		V_{TON} = REF, V_{LL}=12 V, VSNS=1 V	215	259	295	
		V_{TON} = 3.3 V, V_{LL}=12 V, VSNS=1 V	180	215	250	
		V_{TON} = 5 V, V_{LL}=12 V, VSNS=1 V	140	160	185	
t_{MIN}	Controller minimum off-time	Fixed value	80	105	125	ns
$t_{VIDDBNC}$	VID debounce time(2)		100			ns
t_{VCCVID}	VID change to VSNS change (2)				600	ns
$t_{VRONPGD}$	EN low to PGOOD low				100	ns
t_{PGDVCC}	PGOOD low to VSNS change(2)				100	ns
PROTECTION: OVP, PGOOD, FAULTS OFF AND INTERNAL THERMAL SHUTDOWN						
V_{VOVPH}	Internal high OVP threshold voltage	VSNS > V_{OVPH} for 500 ns, DRVL turns ON	1.50	1.55	1.60	V
V_{PGDH}	PGOOD high threshold	Measured at the VSNS pin wrt/VID code. device latches OFF, begins soft-stop.	183	215	247	mV
V_{PGDL}	PGOOD low threshold	Measured at the VSNS pin wrt/VID code. device latches off, begins soft-stop.	–358	–315	–275	mV
TH_{INT}	Internal controller thermal shutdown(2)	Not final tested. Latch off controller, attempt soft-stop.		160		°C
TH_{HYS}	Thermal shutdown hysteresis(2)	Not final tested. Controller will start again after temperature has dropped.		10		°C

(2) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V5IN = V5FILT = 5.0V, GSNS = PGND = GND, VSNS = V_{CORE} (Unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT MONITOR						
V_{PWRLK}	No output current	$V_{CSP} – V_{CSN}$ = 0 mV; R_{IMON} = 69.8 kΩ; R_{IMON2} = 23.7 kΩ, V_{IMONC} = 3.3 V		40		mV
V_{PWRLO}	Low-level power output	$V_{CSP} – V_{CSN}$ = 5 mV; R_{IMON} = 69.8 kΩ; R_{IMON2} = 23.7 kΩ, V_{IMONC} = 3.3 V	590	700	826	mV
V_{PWRMID}	Mid-level power output	$V_{CSP} – V_{CSN}$ = 10 mV; R_{IMON} = 69.8 kΩ; R_{IMON2} = 23.7 kΩ, V_{IMONC} = 3.3 V	1.29	1.40	1.51	V
V_{PWRHI}	High-level power output	$V_{CSP} – V_{CSN}$ = 22 mV; R_{IMON} = 69.8 kΩ; R_{IMON2} = 23.7 kΩ, V_{IMONC} = 3.3 V	2.92	3.04	3.18	V
K_{IMON}	Gain factor			2		μA/mV
$I_{IMONSRC}$	IMON source	$V_{CSP} – V_{CSN}$ = 30 mV	50			μA
V_{IMONCL}	IMON clamp	$V_{CSP} – V_{CSN}$ = 40 mV; R_{IMON} = Open; $V=V_{IMONC}$	V–33	V	V+33	mV
$V_{IMONC-HR}$	IMON clamp headroom	($V_{V5FILT} – V_{IMONC}$); Required for Specified Operation of the IMON Clamp	1.4			V
$V_{IMONC-Z}$	IMON clamp input impedance	Resistance to GND		100		kΩ
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{CLKPGL}	$\overline{PG}$, PGOOD pul-down voltage	Pull down voltage with 3-mA sink current		0.1	0.4	V
$I_{CLKPGLK}$	$\overline{PG}$, PGOOD leakage current	Hi-Z Leakage Current, Apply 5-V in off state	–2	0.2	2	μA
V_{1VH}	I/O 1V logic high	EN, SLP, VID0, VID1, VID2	0.8			V
V_{1VL}	I/O 1V logic low	EN, SLP, VID0, VID1, VID2			0.3	V
I_{1VLK}	I/O 1V leakage – Off	EN = 0V; SLP = VID0 = VID1 = VID2 = 1 V	–1	0	1	μA
I_{1VLKON}	I/O 1V leakage – On	EN = SLP = VID0 = VID1 = VID2 = 1 V	5	10	15	μA
I_{1VLKLO}	I/O 1V leakage – Lo	EN = 1 V; SLP = VID0 = VID1 = VID2 = 0V	–3		1	μA
I_{ENHI}	EN current – On	EN = 1 V			10	μA
I_{ENLO}	EN current – OFF	EN = 0 V	–3		1	μA
I_{SELECT}	Select line current	$V_{TRIPSEL}$ = V_{OSRSEL} = V_{TONSEL} = 5 V	–2	1.5	5	μA

TPS51513
(Top View)

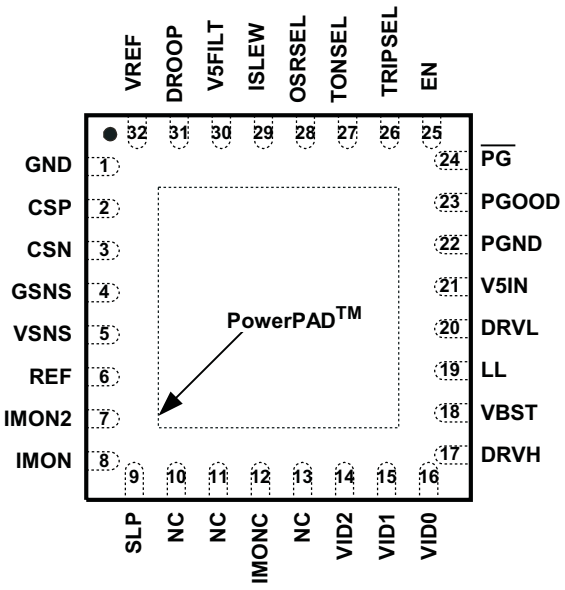


Table 1. Pin Functions

PIN #	NAME	I/O	DESCRIPTION
3	CSN	I	Negative current sense input. Connect to the negative node of current sense resistor or inductor DCR sense RC network.
2	CSP	I	Positive current sense input. Connect to the positive node of current sense resistor or inductor DCR sense RC network.
31	DROOP	O	Output of g_M error amplifier. A resistor to VREF sets the droop gain. A capacitor to VREF helps shape the transient response. Please see *Applications Information* section for configurations with no droop.
17	DRVH	O	Top N-channel FET gate drive outputs.
20	DRVL	O	Synchronous N-channel FET gate drive outputs.
25	EN	I	Chip enable signal. 1-V I/O level; 100-ns de-bounce. Regulator enters controlled soft-stop when brought low.
1	GND	—	Analog / signal ground. Tie to quiet ground plane.
4	GSNS	I	Voltage sense return tied directly to GND of the microprocessor. Tie to GND with a 10-Ω resistor for feedback when μP is not present.
8	IMON	O	Current monitor output. The current out of the IMON output is proportional to the voltage between the CS inputs.
7	IMON2	O	Connection point for IMON mirror matching resistor.
12	IMONC	I	Clamp reference input for the IMON signal; 3.6-V maximum. Bypass to GND with a ceramic capacitor of 0.1 μF or greater.
29	ISLEW	I	Precision current set-point for slew rate control. Tie the ISLEW resistor to GND to select the low range of OCP values; VREF for the higher range.
19	LL	I/O	Top N-channel FET gate drive return. Also, input for adaptive gate drive timing.
10	NC	—	No connection; leave floating.
11			
13			
28	OSRSEL	I	Overshoot reduction (OSR) setting. One of three OSR settings is selected with OSRSEL = GND/VREF/3.3 V. OSRSEL = 5 V disables OSR.
24	$\overline{PG}$	O	Negative active power good output. Transitions low of approximately 50 μs after V_{CORE} reaches the VID-defined level. Open-drain. Leave open if unused.
22	PGND	—	Power return for the synchronous N-channel FET gate driver outputs.
23	PGOOD	O	Power Good output. 6-ms nominal delay from $\overline{PG}$. Open-drain.

Table 1. Pin Functions (continued)

PIN #	NAME	I/O	DESCRIPTION
6	REF	I	Termination for test circuitry. Connect to VREF.
9	SLP	I	Sleep mode control. 1-V I/O level. 100-ns de-bounce.
27	TONSEL	I	On-time selection pin. One of four operating frequencies is selected with TONSEL = GND/VREF/3.3V/5V.
26	TRIPSEL	I	Overcurrent protection (OCP) setting. One of eight valley-current limits is selected with the combination of the ISLEW resistor voltage (GND or VREF) and TRIPSEL = GND/VREF/3.3V/5V.
30	V5FILT	I	5-V power input for control circuitry. Has internal 3-Ω resistor to V5IN. Bypass to GND with a ceramic capacitor of 0.1 μF or greater.
21	V5IN	I	5-V driver power input. Bypass to PGND with a ceramic capacitor of 2.2μF or greater.
18	VBST	I	Top N-channel FET bootstrap voltage inputs.
14	VID0	I	VID programming bits (MSB to LSB). 1-V I/O level. 100 ns de-bounce.
15	VID1	I	
16	VID2	I	
32	VREF	O	1.7-V, 250-μA voltage reference. Bypass to GND with a 0.22-μF capacitor.
5	VSNS	I	Voltage sense line tied directly to VCORE of μP. Tie to V_{CORE} with a 10-Ω resistor to close feedback when μP is not present.
PAD	—	—	Thermal pad; connect to system GND plane with multiple vias.

FUNCTIONAL BLOCK DIAGRAM

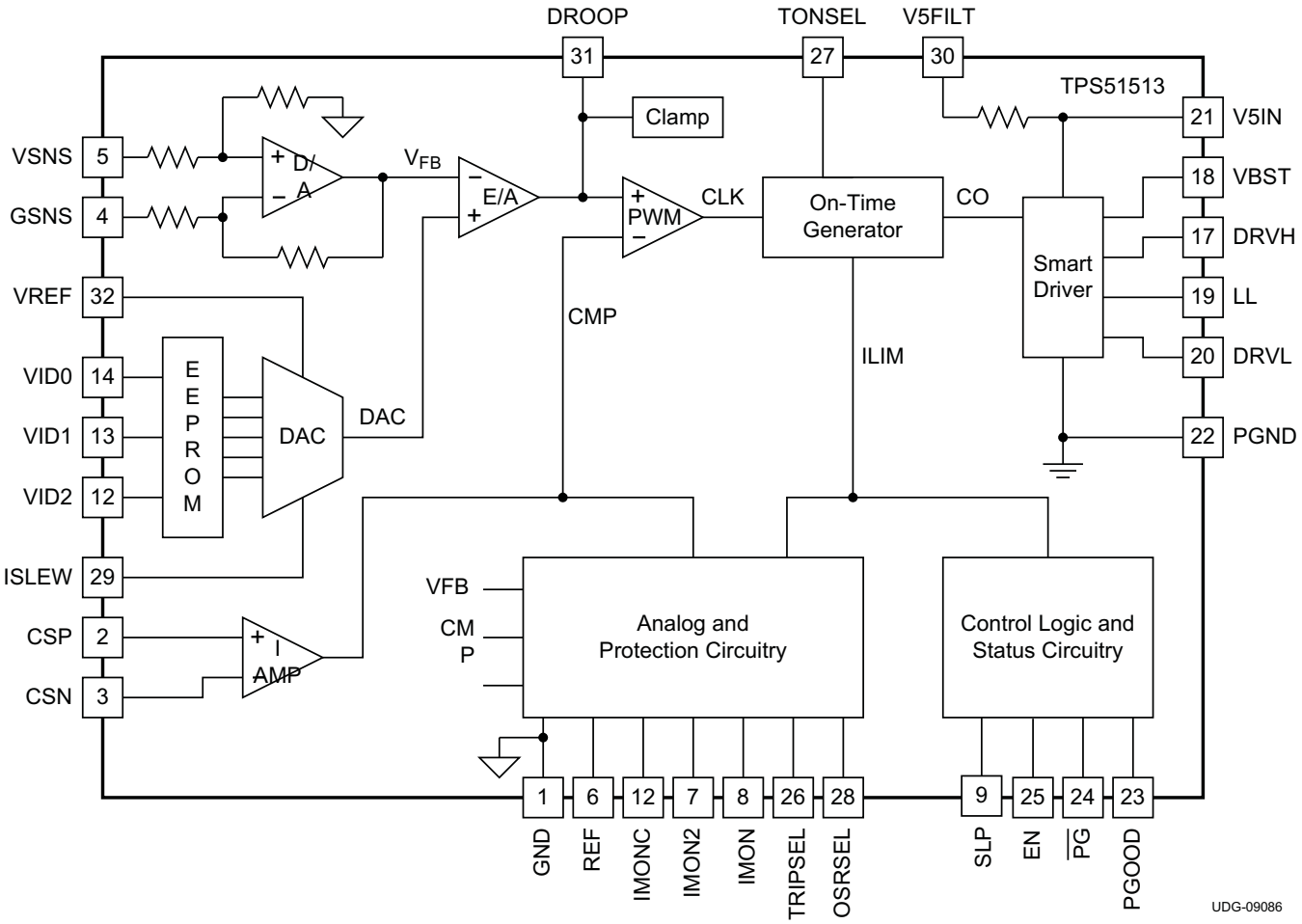


Figure 1. TPS51513 Functional Block Diagram

APPLICATION DIAGRAMS

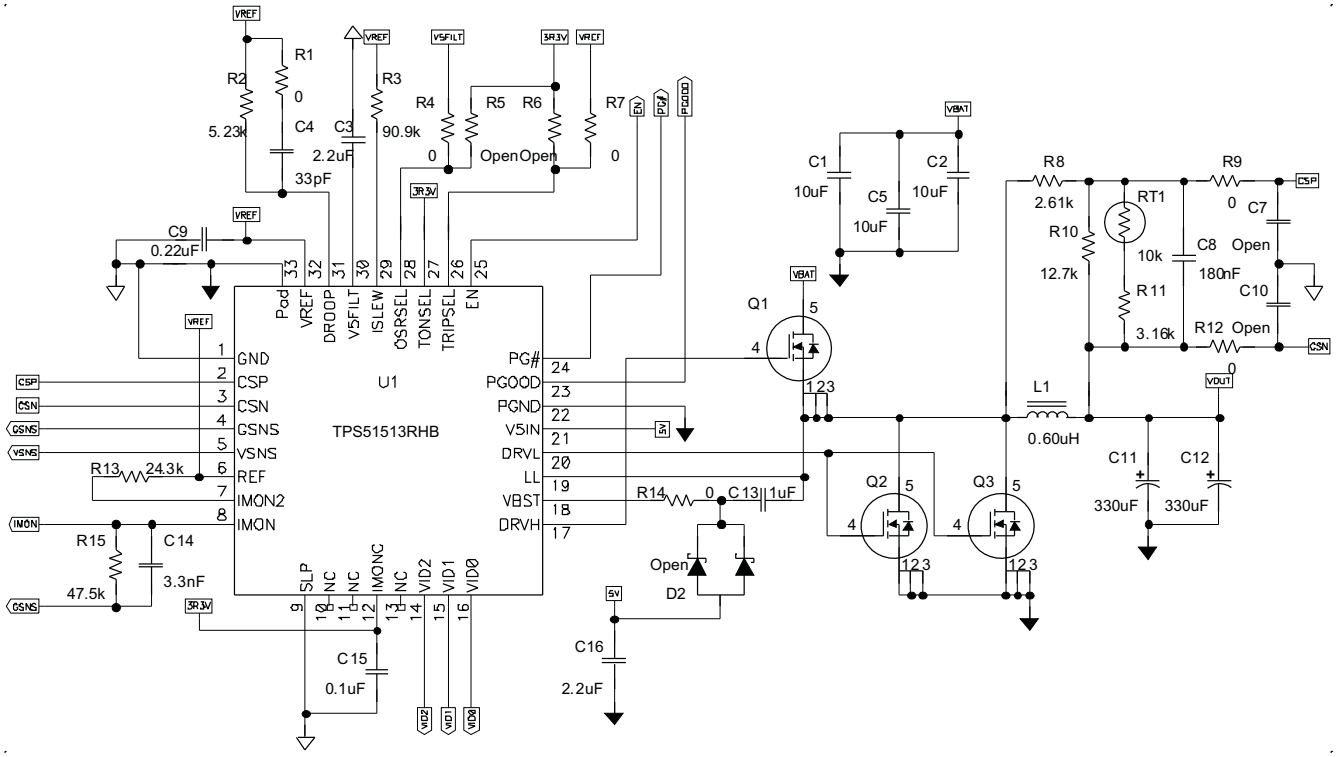


Figure 2. Inductor DCR Current Sense Typical Application Circuit with Droop

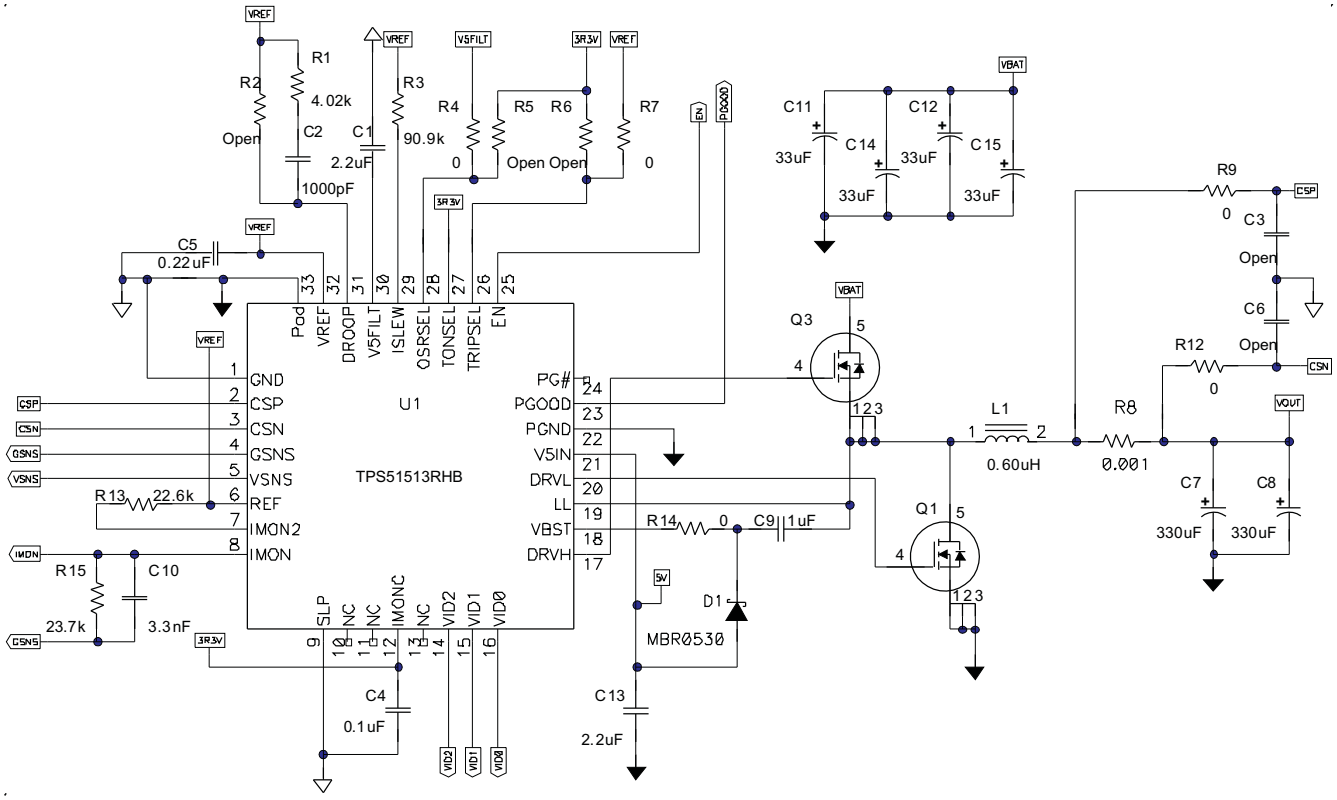


Figure 3. Resistor Current Sense Typical Application Without Droop

DETAILED DESCRIPTION

Application Circuit List of Materials

Recommended parts for key external components for the circuits in Figure 2 and Figure 3 are in Table 2. These parts have passed applications tests.

Table 2. Key External Component Recommendations

COMPONENT	MANUFACTURER	PART NUMBER
High-side FET(s)	TI	CSD16409Q3
	Infineon	BSC080N03MSG
Low-side FET(s)	TI	CSD16401Q5
	Infineon	BSC030N03MSG
Inductors	Panasonic	ETQP4L series
	Tokin	MPCG1040L series
	Toko	FDUE10140D series
	Vishay	IHLP5050 series
Bulk output capacitors	Panasonic	EEFSX0D331XE
	Kemet	T528Z series
	NEC Proadlizer	PFAF250E127MNS
Ceramic output capacitors	Panasonic	ECJ2FB0J106K
	Murata	GRM21BR60J106KE19L
Sense resistor (resistor sensing only)	Panasonic	ERJM1WTJ1M0U
NTC thermistors	Panasonic	ERTJ1VG103JA
	TDK	NTCG163JF103HT

Functional Overview

The TPS51513 is a DCAP+™ mode adaptive on-time converter. The output voltage is set using a DAC that outputs a reference in accordance with either the 3-bit VID code defined in Table 3. *VID-on-the-fly* transitions are supported with the slew rate controlled by a single resistor on the ISLEW pin. Powerful integrated FET drivers support output currents in excess of 25 A. The converter automatically runs in discontinuous mode to optimize light-load efficiency and battery life. The four switching frequency selections (given in Table 3) enable optimization of the power chain for the cost, size and efficiency requirements of the design.

Table 3. Frequency Selection Table

TONSEL	FREQUENCY (f_{SEL}) (kHz)
GND	250
VREF	300
3.3 V	350
5 V	500

In adaptive on-time converters, the controller changes the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS51513, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the DAC voltage and the feedback voltage.

This approach has two advantages:

1. The amplifier DC gain sets an accurate linear load-line; this is required for CPU core applications.
2. The error voltage input to the PWM comparator is filtered to improve the noise performance.

PWM Operation

Referring to Figure 1 and Figure 4, in steady state, continuous conduction mode, the converter operates as follows:

Starting with the condition that the top FET is off and the bottom FET is on, the current feedback (V_{CMP}) is higher than the error amplifier output (V_{DROOP}). V_{CMP} falls until it hits V_{DROOP}, which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.

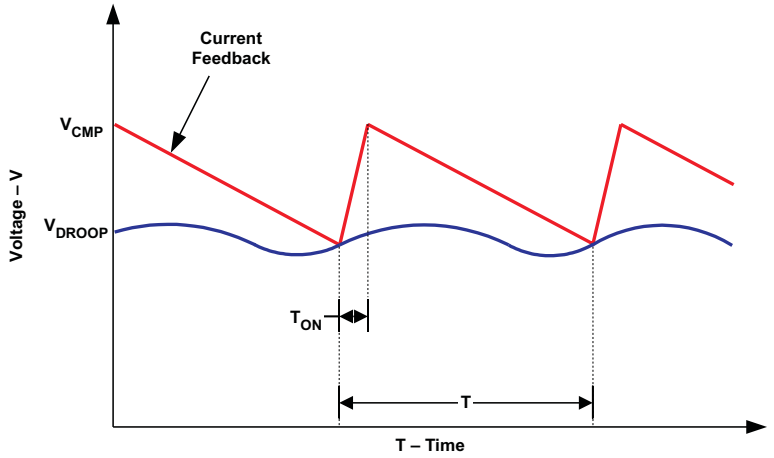


Figure 4. D-CAP+ Mode Basic Waveforms

The current feedback is an amplified and filtered version of the voltage between the CSP and CSN inputs. The TPS51513 provides fully differential current and voltage feedback to increase the system accuracy and reduce the dependence of circuit performance on layout.

PWM Frequency and Adaptive On-Time Control

The on-time is determined by Equation 1.

$$t_{ON} = \left(\frac{V_{OUT}}{V_{IN}} \right) \times \left(\frac{1}{f_{SEL}} \right) + 30\,ns \quad (1)$$

where

- f_{SEL} is the frequency selected by the connection of the TONSEL pin, given in Table 3

The on-time pulse is sent to the top FET; the inductor current and the current feedback rises to its maximum value. Each ON pulse is latched to prevent double pulsing.

Droop or No-Droop Compensation

The TPS51513 can be designed to either provide a linear load line (also known as *droop*) or operate with a flat load-line (*no-droop*). This is achieved by the component topology at the DROOP pin.

Droop is obtained by putting a resistor from DROOP to VREF (R_{DROOP}) to limit the gain of the error amplifier. The equation for droop is shown in Equation 2.

$$V_{DROOP} = \frac{R_{CS} \times A_{CSINT} \times I_{OUT}}{R_{DROOP} \times G_{M(droop)}}$$

where

- R_{CS} is the effective current sense resistance, whether a sense resistor or inductor DCR is used
- A_{CSINT} is the gain of the current sense amplifier
- I_{OUT} is the output current,
- GM_{DROOP} is the G_M of the droop amplifier. (2)

The load-line is defined by the change in output voltage vs. the change in current.

$$R_{L-L} = -\frac{V_{DROOP}}{I_{OUT}} \quad (3)$$

The TPS51513 also has the ability to provide an output without a load line. In this case, referring to Figure 2, R2 is left open, and R1 and C2 are populated to break the DC path between DROOP and REF and providing very high DC loop gain. Means to select R1 and C2 are given in the *Design Procedure* section.

Overshoot Reduction (OSR™) Feature

The problem of overshoot in low duty-cycle synchronous buck converters is well known, and results from the output inductor having a small voltage (V_{CORE}) with which to respond to a transient load release.

In Figure 5, with ideal components and the common values of 12-V input and 1-V output, the inductor voltage (V_L) with the upper FET on is 11 V (12V – 1V). With the lower FET on, the inductor voltage is only 1 V.

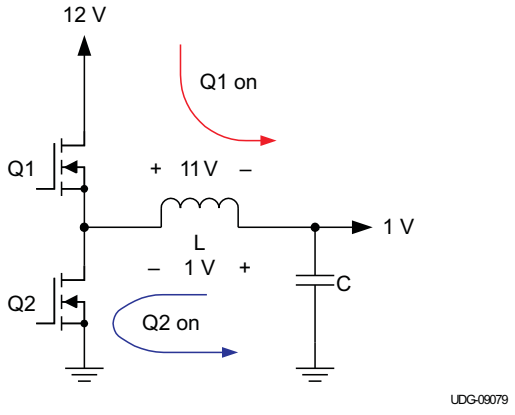


Figure 5. Representative Schematic of a Synchronous Converter

Because $\frac{\Delta I}{\Delta t} = \frac{V_L}{L}$, the converter can respond much more quickly to a load step than it can to a load release.

The idea of OSR is to turn off the lower FET during a transient load release to force the inductor current through the body diode of the lower FET, thus increasing the voltage across the inductor to V_{CORE} + V_{DIODE}. This discharges the inductor more quickly and reduces the peak voltage of the transient overshoot. As a result, less output capacitance is required to achieve a given output tolerance specification.

Figure 6 shows the converter operation during transient release. The energy in the inductor is transferred to the capacitance on the V_{CORE} node above and the output voltage (channel 4) overshoots the desired level (lower cursor). In this case, the magnitude of the overshoot is 34 mV. Note that the DRVL waveform (channel 2) is high during the overshoot.

The performance of the same circuit, but with OSR enabled is shown in Figure 7. In this case, the low-side FET is shut off when overshoot is detected and the energy in the inductor is partially dissipated by the body diodes. The overshoot is reduced to 18 mV. Also note that the DRVL signal is OFF only long enough to reduce the overshoot.

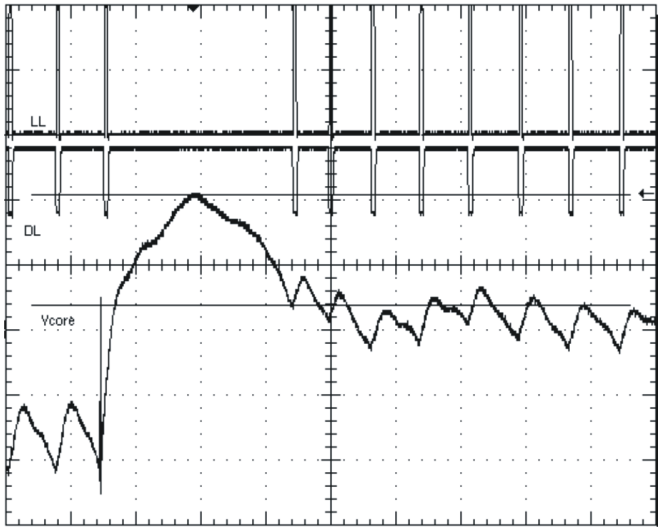


Figure 6. Circuit Performance Without Overshoot Reduction

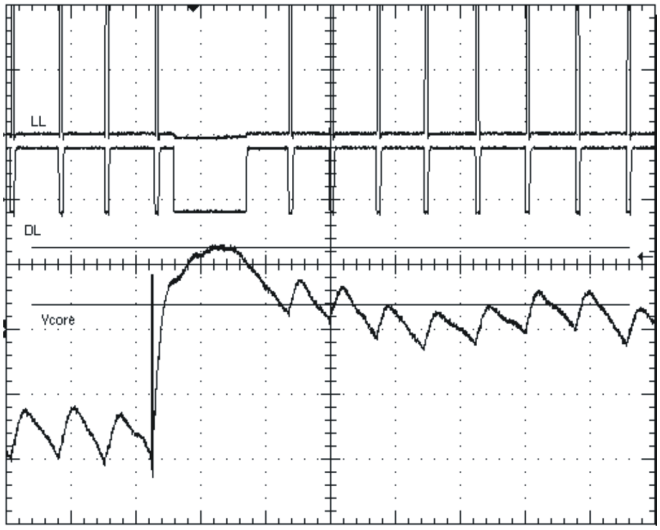


Figure 7. Transient Release Performance is Greatly Improved by the OSR Circuit

Implementation

OSR is implemented using a comparator between the DROOP and CMP nodes in Figure 1. To implement OSR, simply terminate the OSRSEL pin to the desired voltage to set the threshold voltage for the comparator. The settings are:

1. GND = minimum trigger voltage (Maximum overshoot reduction)
2. VREF = medium trigger voltage
3. +3.3V = maximum trigger voltage (Minimum overshoot reduction)
4. 5V = OSR off

Use the highest setting that provides the desired level of overshoot reduction to eliminate the possibility of false OSR operation.

Light Load Power Saving Features

The TPS51513 has several power saving features to provide excellent efficiency over a very large load range. The TPS51513 has an automatic pulse skipping *skip* mode. Regardless of the state of the logic inputs, the converter senses negative inductor current flow and prevents it by shutting off DRVL. This saves power by eliminating re-circulating current. Also, when the bottom FET shuts off, the converter enters discontinuous mode, and the switching frequency decreases, thus reducing switching losses as well.

The SLP signal is used to enter a *sleep* (SLP) mode. The SLP pin determines the method of entering sleep mode. If SLP is HI, the converter is allowed to run in skip mode. In this mode, for loads with low leakage current, the output voltage slew rate is determined by the output capacitance and the leakage current. If SLP is LO, the device enters PWM mode, and the voltage is actively pulled down by the rate set by R_{SLEW}. The equations are given below. Because changing V_{CORE} quickly results in large currents charging/discharging the output capacitors, and this can cause audible noise in inductors and ceramic capacitors, entering a sleep mode with SLP=HI is recommended.

FET Drivers

The TPS51513 incorporates strong, high-performance gate drives with adaptive cross-conduction protection. The driver uses the state of the DRVL, DRVH, and LL pins to ensure that the top or bottom FET is off before turning the other on. Fast logic and high-drive currents quickly charge and discharge FET gates to minimize dead-time to increase efficiency. The top gate driver also includes an internal P-N junction *boost* diode, decreasing the size and cost of the external circuitry. For maximum efficiency, this diode can be bypassed externally by connecting a Schottky diode from V5IN (anode) to VBST (cathode).

Voltage Slewing

The TPS51513 changes the voltage of the internal DAC in a controlled manner to perform SLP entry, SLP exit, and VID change functions. The slew rate is independent of switching frequency or load. It is set by a resistor from the ISLEW pin to either GND or VREF (R_{SLEW}). R_{SLEW} sets one rate for SLP exit and VID changes (SR in the equation below; SR is in units of mV/µs.) A proportional rate is used for soft-start and soft-stop functions. The ISLEW pin is held at $VSLEW_{REF}$, which is 1.25 V, nominal.

$$R_{SLEW} = \frac{K_{SLEW} \times V_{SLEW}}{SR} \tag{4}$$

In Equation 4), K_{SLEW} = 1.25x10^9. V_{SLEW} is equal to $VSLEW_{REF}$ (1.25V) when R_{SLEW} is tied to GND. To access the upper range of OCL limit values, connect R_{SLEW} to VREF. In this case, V_{SLEW} is 0.45V (VREF – $VSLEW_{REF}$) and R_{SLEW} must be changed accordingly.

The soft-start and soft-stop slew rates are 1/8 of SR. On start-up, the TPS51513 V_{CORE} output ramps to the level defined by the VID code (V_{VID}). Because of this, the VID code needs to be valid and stable at the time EN is raised. The calculation for soft-start and soft-stop time is shown in Equation 5.

$$t_{SS} = \frac{V_{VID} \times 8}{SR} \tag{5}$$

After approximately 50µs, $\overline{PG}$ is set LO. Once $\overline{PG}$ transitions LO, the VID code can change at any time.

Soft Stop Control with Low Impedance Output Termination

The voltage slewing capability is also used to slowly slew the voltage down for a soft-stop without undershoot. The soft-stop rate equals the soft-start rate. As long as V5IN is available and EN toggles low, the TPS51513 slews from the current VID to approximately 0.3 V. At this point, the DRVL signal is held LO and an internal transistor of approximately 1-kΩ is connected from VSNS to GND turns on to keep V_{CORE} from rising up as a result of stray leakage currents.

Protection Features

The TPS51513 has a full suite of features to protect the converter power chain as well as the system electronics.

Input Undervoltage Protection (UVLO):

The TPS51513 continuously monitors the voltage on the V5FILT pin to be sure the value is high enough to bias the device properly and provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.4 V and has a nominal 200 mV of hysteresis. This function is not latched. Removing and restoring the 5-V power supply to the device can be used to reset it. Be sure the voltage at the device discharges below 1.6 V before rising again to reset the device.. The power input (V_{BAT}) does not have a UVLO function, so the circuit operates with power inputs down to approximately 2 × V_{CORE}.

Power Good Signals

The TPS51513 has two open-drain power good pins. PGOOD and $\overline{PG}$ have the following nominal thresholds:

- High: V_{DAC} +200mV (also acts as a proportional OVP signal)
- Low : V_{DAC} –300mV

The differences are:

- $\overline{PG}$ transitions active shortly after V_{CORE} reaches V_{DAC} on power-up; PGOOD has a 6ms nominal delay after $\overline{PG}$.

- $\overline{PG}$ is negative active; PGOOD is positive active.

Both signals go inactive as soon as the EN pin is pulled low or an undervoltage condition on V5IN is detected. Both signals are masked during DAC transitions to prevent false triggering during voltage slewing.

Output Overvoltage Protection (OVP):

An OVP condition is detected when V_{CORE} reaches the high PG threshold. When this threshold is reached, the converter sets PGOOD and $\overline{PG}$ signals inactive, performs the soft-stop sequence, and latches OFF. The converter remains in this state until the device is reset by cycling either V5IN or EN.

However, because of the dynamic nature of actively power managed systems, the +200 mV OVP threshold is *blanked* during voltage transitions. In order to protect the processor 100% of the time, there is a second OVP level fixed at 1.55-V nominal which is always active. When a fixed OVP condition is detected, PGOOD and $\overline{PG}$ are set inactive and DRVL is driven HI. The converter remains in this state until either V5IN or EN are cycled.

Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described below. If V_{CORE} drops below the low PGOOD threshold for 80µs, then the converter enters soft-stop mode and latches OFF at the completion of soft stop.

Current Protection

Two types of current protection are provided in the TPS51513:

- Overcurrent Protection (OCP)
- Negative OCP

Overcurrent Protection

The TPS51513 uses a “valley” current limiting circuit. As a result, the OCP set point is the OCP DC limit minus half of the ripple current. Current limiting occurs on a pulse-by-pulse basis. If the sensed current value is above the OCP setting, the converter holds off the next ON pulse until the current ramp drops below the OCP limit. Eight OCP settings are provided in two ranges. The ranges are selected by the termination of the R_{SLEW} resistor as in Figure 8.

The OCP range is selected by the connection of the R_{SLEW} resistor. Connect R_{SLEW} to VREF to select the high OCP range as shown in Figure 8. Connect R_{SLEW} to GND to select the low OCP range as shown in Figure 9

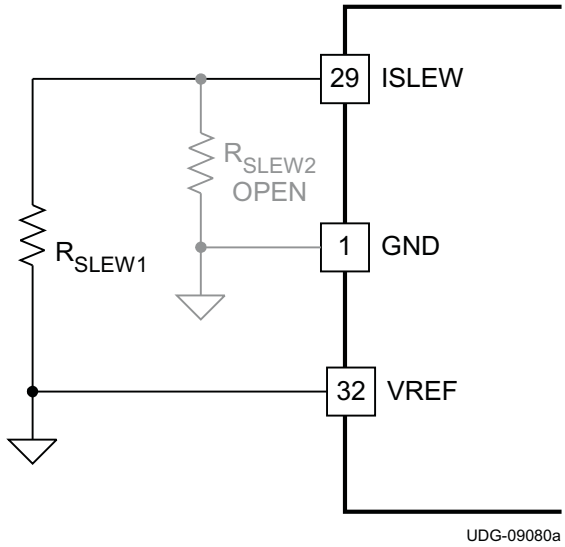


Figure 8. Connection to Select High Range Overcurrent Protection

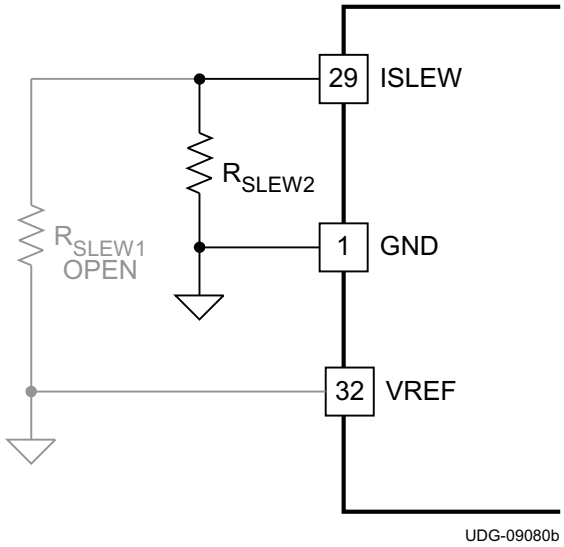


Figure 9. Connection to Select Low Range Overcurrent Protection

The OCP values refer to the voltage between the current sense inputs. Refer to the parameter table to choose the appropriate TRIPSEL value. The value of R_{SLEW} changes depending on the termination. See the *Voltage Slewing* section for details.

In OCP, the voltage droops until the UVP limit is reached. After the UPC limit is reached (approximately 80 μs later) the converter sets PGOOD and PG signals inactive, performs the soft-stop sequence, and then latches OFF. The converter remains in this state until the device is reset.

Negative Overcurrent Protection

The negative OCP circuit acts when the converter is sinking current. The converter continues to act in a "valley" mode, so to have a similar negative DC limit, the absolute value of the negative OCP set point is typically 50% higher than the positive one.

Thermal Shutdown

The TPS51513 has an internal temperature sensor. When the temperature reaches a nominal 160°C, the device shuts down until the temperature cools approximately 10°C. Then, the converter latches off until either EN or V5IN is cycled.

Current Monitor

The TPS51513 includes a current monitor function. The current monitor puts out an analog voltage proportional to the output power on the IMON pin. The equation is shown in Equation 6.

$$V_{IMON} = K_{IMON} \times R_{IMON} \times V_{CS} \quad (6)$$

where

- K_{IMON} is given in the parameter table
- V_{CS} is the differential voltage at the inputs to the current sense amplifiers

In order to increase the accuracy of the current monitor over temperature the IMON2 pin is provided to match the temperature coefficients of two critical resistors in the circuit. Connect a resistor from IMON2 to VREF.

After determining the full-scale voltage on the IMON output (V_{IMON}) and selecting R_{IMON}, the value of R_{IMON2} resistor can be calculated as shown in Equation 7.

$$R_{IMON2} = \frac{8 \times V_{CS} \times A_{CSINT} \times R_{IMON}}{V_{IMON}} \quad (7)$$

where

- A_{CSINT} is the gain of the internal current sense amplifier (given in the parameter table)
- 8 is the internal current mirror ratio

The IMON output requires a ceramic capacitor ≥3.3 nF connected to GSNS (or GND) for stable operation.

IMON Clamp Function

The IMON function also includes a clamp to prevent overvoltage of the device reading the IMON voltage. The clamp voltage is set by the voltage applied at the IMONC pin (pin 12). IMONC is intended to be connected to the same supply voltage as the downstream A/D converter, but other implementations are possible. To meet the specified tolerances, a minimum *headroom* voltage for the IMON clamp must be observed. The V5FILT voltage needs to be higher than the IMONC voltage by a minimum amount specified in the parameter table. Bypass IMONC with a ceramic capacitor ≥0.1μF connected to GND.

VID Table

The TPS51513 belongs to a family of power management devices that can be programmed to any eight VID values. These values are from 0.3 V to 1.5 V in 12.5 mV steps. The specific VID selections for the TPS51513 are given in Table 4. Other VID selections are possible, and are provided under a different device number. Contact your TI field support team for details.

Table 4. VID Selections for the TPS51513

VID			V_{DAC} (V)
0	0	0	1.05
0	0	1	1.00
0	1	0	0.95
0	1	1	0.90
1	0	0	0.85
1	0	1	0.80
1	1	0	0.75
1	1	1	0.70

APPLICATION INFORMATION

Design Procedure

The TPS51513 has a simple design procedure for a high-performance controller.

Initial Parameters:

Step One: Determine the load requirements. For the purposes of this exercise, the following requirements are used:

The processor requirements provide the following key parameters:

1. V_{MAX} = 1.050 V
2. R_{L-L} = –3 mΩ
3. I_{MAX} = 22 A; I_{OCP_MIN} = 25 A
4. $I_{DYN-MAX}$ = 10 A
5. Sleep slew rate = 5 mV/μs (minimum)

Step Two: Determine system parameters. The input voltage range and operating frequency are of primary interest. For example:

1. V_{IN-MAX} = 15 V
2. V_{IN-MIN} = 8 V
3. f = 300 kHz

For an operating frequency of 350 kHz, tie TONSEL to 3.3 V.

Step Three: Determine current sensing method. The TPS51513 supports both resistor sensing and inductor DCR sensing. Inductor DCR sensing is chosen.

For resistor sensing, substitute the resistor value (1 mΩ recommended for a approximately 25-A application) for R_{CS} in the subsequent equations and skip Step Five.

Step Four: Determine inductor value and choose inductor. Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 20% to 40% of the maximum current per phase. In this case, we use 20%:

I_{P-P} = 25 A × 0.2 = 5 A

At f = 350 kHz, with 15-V input and 1.05-V output:

$$I_{P-P} = 25\,A \times 0.2 = 5\,A$$

where

- $V = V_{IN-MAX} - V_{MAX}$
- $dT = V_{MAX}\ (F \times V_{IN-MAX})$. (8)

$$L = \frac{V \times dT}{I_{P-P}}$$

where

- L = 0.6 μH (9)

An inductor value of 0.6 μH is chosen. The inductor must not saturate during peak loading conditions. The factor of 1.2 is to allow for current sensing and current limiting tolerances.

$$I_{SAT} = \left(I_{INST} + \frac{I_{P-P}}{2} \right) \times 1.2 \times = 41.5\,A \quad (10)$$

The chosen inductor should have the following characteristics:

1. As flat an inductance vs. current curve as possible. Inductor DCR sensing is based on the idea L/DCR is approximately a constant through the current range of interest.
2. Either high saturation or *soft saturation*
3. Low DCR for high efficiency, but at least 0.7 mΩ for proper signal levels.
4. DCR tolerance as low as possible for load-line accuracy.

For this application, the Vishay IHLP5050CZ-06 0.6-μH, 1.85-mΩ inductor is chosen.

Step Five: Design the thermal compensation network. In most designs, NTC thermistors are used to compensate thermal variations in the resistance of the inductor winding. This winding is generally copper, and so has a resistance coefficient of 3900 PPM/°C. NTC thermistors, on the other hand, have very non-linear characteristics and need two or three resistors to linearize them over the range of interest. The typical DCR circuit is shown in Figure 10.

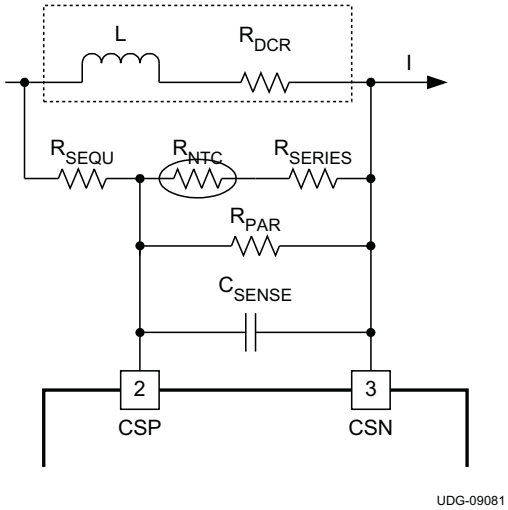


Figure 10. Typical DCR Sensing Circuit

In this circuit, good performance is obtained when:

$$\frac{L}{R_{DCR}} = C_{SENSE} \times R_{EQ} \quad (11)$$

where

- all of the parameters are defined in Figure 10
- R_{EQ} is the series/parallel combination of the other four discrete resistors

C_{SENSE} should be a capacitor type which is stable overtemperature. Use X7R or better dielectric (C0G preferred).

Because calculating these values by hand is difficult, TI offers a spreadsheet using the Excel *Solver* function.. Contact your local TI representative to get a copy of the spreadsheet.

In the reference design, the following values are input to the spreadsheet:

- L
- R_{DCR}
- Load line
- Thermistor R25 and “b” value

The spreadsheet then calculates R_{SEQU}, R_{SERIES}, R_{PAR}, and C_{SENSE}. The R_{CS_Eff} versus temperature curve is shown in Figure 11.

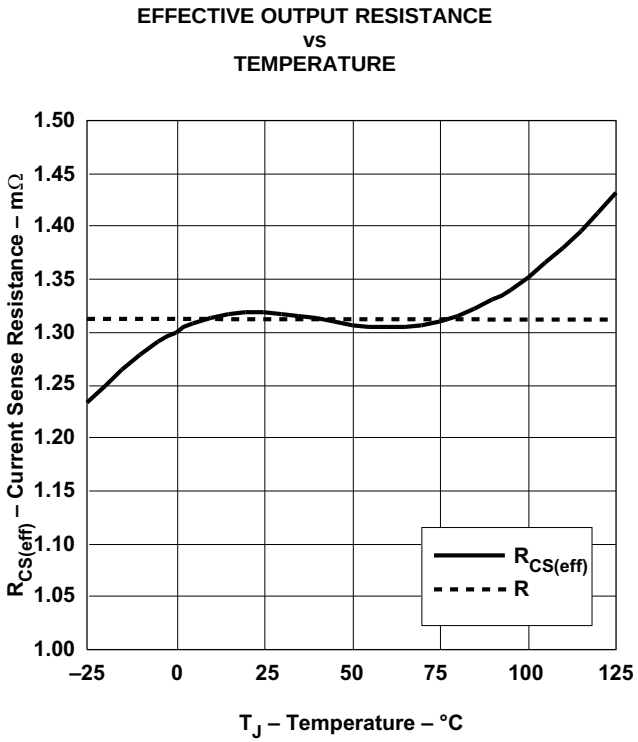


Figure 11.

In this case, the nearest standard values are:

- R_{SEQU} = 2.61 kΩ;
- R_{SERIES} = 3.16 kΩ;
- R_{PAR} = 12.7 kΩ
- C_{SENSE} =180 nF

Note the effective divider ratio for the inductor DCR. The effective current sense resistance (R_{CS_Eff}) is:

$$R_{CS(eff)} = R_{DCR} \times \frac{R_{P\_N}}{R_{SEQU} + R_{P\_N}} \tag{12}$$

R_{P_N} is the series/parallel combination of R_{NTC}, R_{SERIES} and R_{PAR}.

$$R_{P\_N} = \frac{R_{PAR} \times (R_{NTC} + R_{SERIES})}{R_{PAR} + R_{NTC} + R_{SERIES}} \tag{13}$$

R_{CS_Eff} is 1.31mΩ. Choose the value of TRIPSEL so the minimum TRIPSEL voltage is just above the voltage across the current sense pins at the valley point of the current waveform. Maximize the value of R_{CS_Eff} for improved circuit performance.

$$V_{TRIPSEL(min)} \geq R_{CS(eff)} \times \left(I_{MAX} - \left(\frac{I_{RIPPLE}}{2} \right) \right) \tag{14}$$

In this case, the TRIPSEL minimum value needs to be greater than 29.8 mV; the next highest value in the parameter table is 31.4 mV. This value corresponds to connecting TRIPSEL to VREF and R_{SLEW} to VREF.

Step Six: Determine the output capacitor configuration. In general, for a system with a load-line, the ESR of the output capacitors should be equal to or less than the load-line value. The magnitude and slew rate of the dynamic load also drives the capacitor choice, as does the inductor selection. For highly dynamic systems, a successful design has a combination of bulk and ceramic capacitance totaling approximately 1000μF.

Step Seven: Set the load line. The load line is set by the droop resistor knowing R_{L-L} and R_{CS_Eff}.

$$R_{DROOP} = \frac{R_{CS(eff)} \times A_{CS}}{G_M \times R_{L-L}} \quad (15)$$

R_{DROOP} = 5.23 kΩ.

Step Eight: Select the DROOP capacitor.

The DROOP capacitor is used to provide high-frequency filtering of the voltage loop. Use values under 100 pF. A higher value provides less jitter for steady-state operation, but slows down the transient response.

Step Nine: Calculate R_{SLEW}. R_{SLEW} sets both slew rates:

1. Sleep exit slew rate.
2. Soft-start and soft-stop exit rate is 1/8 of the sleep exit rate

Set the sleep rate to 6 mV/μs to allow 20% for tolerances. From Equation 3):

$$R_{SLEW} = \frac{K_{SLEW} \times V_{SLEW}}{SR} \quad (16)$$

In this case, R_{SLEW} is terminated to GND. K_{SLEW} = 1.25x10^9 and V_{SLEW} = 0.45 V. For a slew rate (SR) of 6 mV/μs nominal, 5 mV/μS minimum, R_{SLEW} = 90.9 kΩ.

Step Ten: Calculate IMON resistors.

From Equation 6,

$$R_{IMON} = \frac{V_{IMON}}{K_{IMON} \times V_{CS}} \quad (17)$$

And,

$$V_{CS} = R_{CS(eff)} \times I_{MAX}$$

where

- V_{CS} = 29.8 mV
- K_{IMON} = 2μA/mV (18)

The IMONC pin is connected to 3.3 V; to allow for tolerances, a full scale value of 3.1 V (V_{IMON}) is desired. Then, R_{IMON} = 47.5 kΩ.

In order to increase the accuracy of the current monitor overtemperature the IMON2 pin is provided to match the temperature coefficients of two critical resistors in the circuit. Connect a resistor from IMON2 to VREF.

After determining the full-scale voltage on the IMON output (V_{IMON}) and selecting R_{IMON}, the value of R_{IMON2} resistor is from Equation 7:

$$R_{IMON2} = \frac{8 \times V_{CS} \times A_{CSINT} \times R_{IMON}}{V_{IMON}}$$

where

- A_{CSINT} = 6
- R_{IMON2} = 24.3kΩ (19)

Step Eleven: Select decoupling and peripheral components.

For TPS51513 peripheral capacitors please use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always OK.

- V5IN decoupling ≥ 2.2μF, ≥ 10V
- V5FILT decoupling ≥ 1μF, ≥ 10V
- VREF decoupling 0.22 μF to 1μF, ≥ 4V
- Bootstrap capacitors ≥ 0.22μF, ≥ 10V
- Bootstrap diode (optional) 30V Schottky diode, BAT-54 or better

For power chain and other component selection, see Table 2.

Control Loop Design

The TPS51513 control architecture (current-mode, constant on-time) has been analyzed by the Center for Power Electronics Systems (CPES) at Virginia Polytechnic and State University. The following equations are from their presentation: *Equivalent Circuit Representation of Current-Mode Control* from November 21, 2008.

One of the benefits of this technology is the lack of the *sample and hold* effect that limits the bandwidth of fixed frequency current mode controllers and causes sub-harmonic oscillations.

The loop gain is the gain of the DROOP amplifier multiplied by the control-to-output gain:

Control-to-Output

The control-to-output gain is given by the expression:

$$\frac{v_O}{v_C} = K_C \times \frac{1}{1+\left(\frac{\omega}{(Q_1 \times \omega_1)}\right)+\left(\frac{\omega^2}{\omega_1^2}\right)} \times \frac{\omega \times R_{ESR} \times C_{OUT} + 1}{\left(\left(\frac{\omega}{\omega_a}\right)+1\right)} \tag{20}$$

where

$$K_C = \frac{\left(\frac{R_L}{R_i}\right)}{1+\left(\frac{(t_{ON} \times R_L)}{(2 \times L_S)}\right)} \tag{21}$$

$$\omega_1 = \frac{\Pi}{t_{ON}} \tag{22}$$

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} \tag{23}$$

$$\omega_a = \frac{1+\left(\frac{t_{ON} \times R_L}{2 \times L_S}\right)}{R_L \times C_{OUT} 1+\left(\frac{t_{ON} \times R_{ESR}}{2 \times L_S}\right)} \tag{24}$$

For this converter,

$$R_1 = R_{CS(eff)} \times A_{CS} \tag{25}$$

The frequency response of the control-to-output gain can be graphed using the following parameters:

- V_{IN} = 12 V
- V_{OUT} = 1.05 V

- I_{OUT} = 5 A
- F_S = 350 kHz
- L_S = 0.56 µH
- C_{OUT} = 660 µF
- R_{ESR} = 3 mΩ

The theoretical waveform is plotted in Figure 12. For comparison purposes, the measured data is in Figure 13. Note the excellent correlation between the theoretical and actual data. In both cases, the 0-dB bandwidth is approximately 25 kHz, and the phase margin is >90 degrees! As a result, creating the desired loop response is a matter of adding a DC gain component (if a load-line is allowed) or adding an appropriate pole-zero or pole-zero-pole compensation

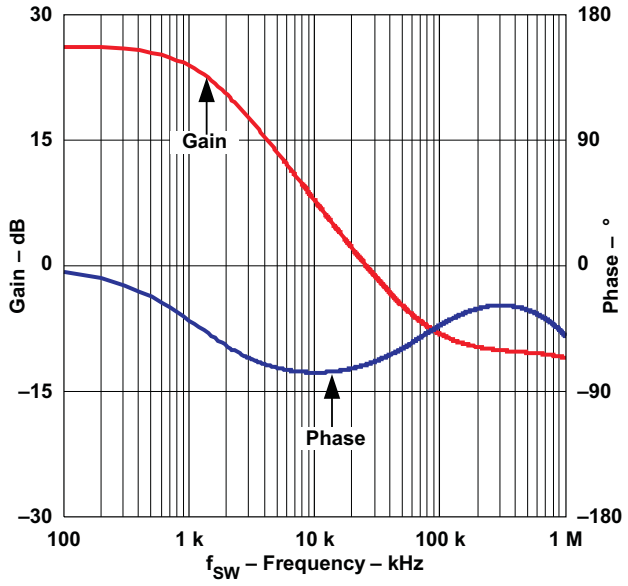


Figure 12. Theoretical Control to Output Transfer Function

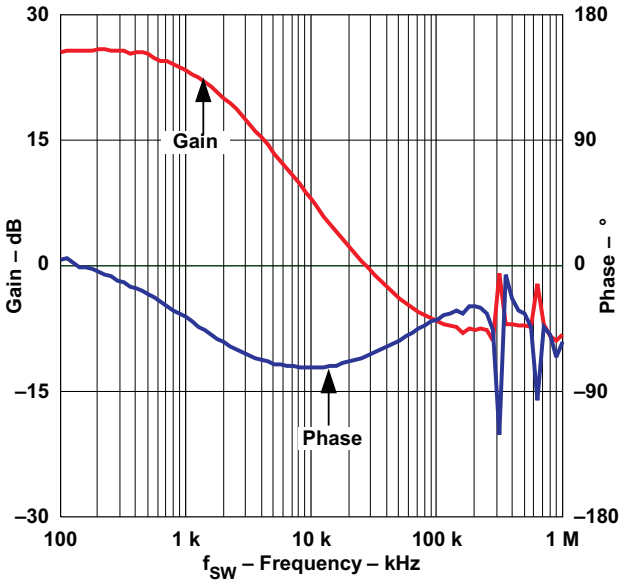


Figure 13. Measured Control to Output Transfer Function

Limit the overall open-loop bandwidth below ½ of f_S to avoid violating the Nyquist Criterion. Also, for the best performance of the modulator, the characteristic of the compensation should be resistive at the switching frequency. With this in mind, a zero frequency in the range of 10% to 20% of f_S is recommended.

Because the droop amplifier is a trans-conductance amplifier, for a series R_C-C_C, the pole is at 0 Hz, mid-band gain is $g_M \times R_C$, and the zero frequency is $R_C \times C_C$. For R_C = 4.02 kΩ and C_C = 1000 pF, the mid-band gain is 2.01 and the zero frequency is approximately 40 kHz. The droop amplifier gain is graphed in Figure 14 and the overall loop gain in Figure 15.

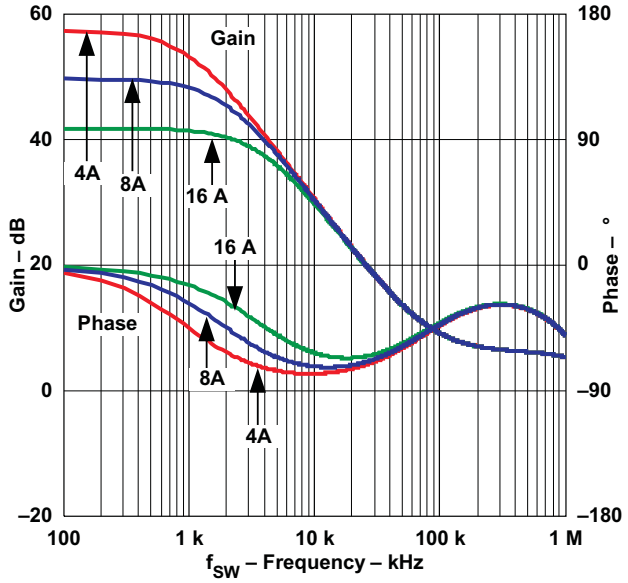


Figure 14. Droop Amplifier Gain for Zero Load-line Compensation

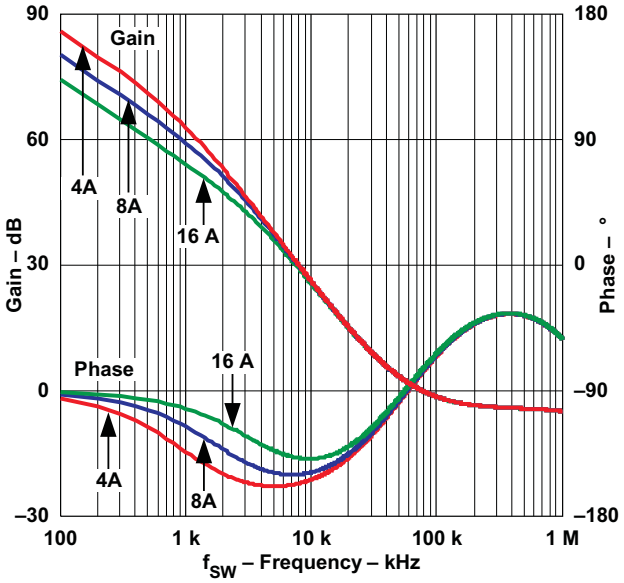


Figure 15. Overall Loop Gain with Zero Load-line Compensation Shown for 4A, 8A, and 16A Load Current

In this design, the bandwidth is 80 kHz and the phase margin is >90 degrees. The gain margin is low, however, this analysis omits the affect of ceramic capacitance on the output. Ceramic capacitors reduce the loop gain at high frequencies. Contact your TI representative to obtain a copy of the Mathcad® spreadsheet used to generate the above curves.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

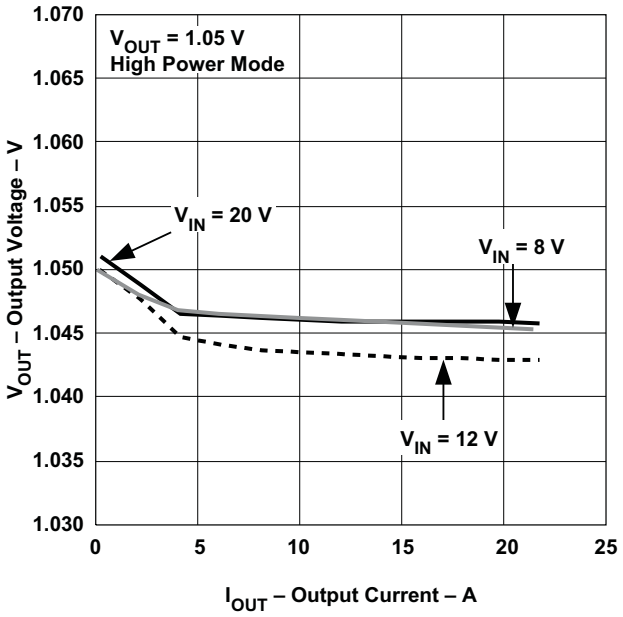


Figure 16.

OUTPUT VOLTAGE vs OUTPUT CURRENT

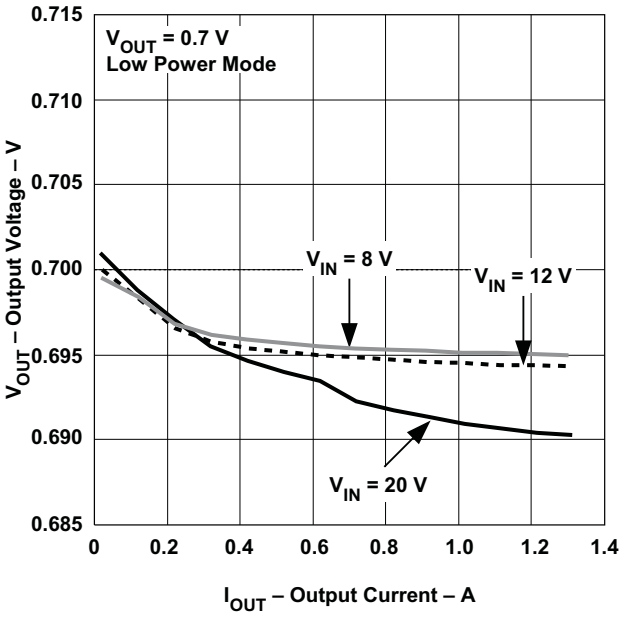


Figure 17.

EFFICIENCY vs OUTPUT CURRENT

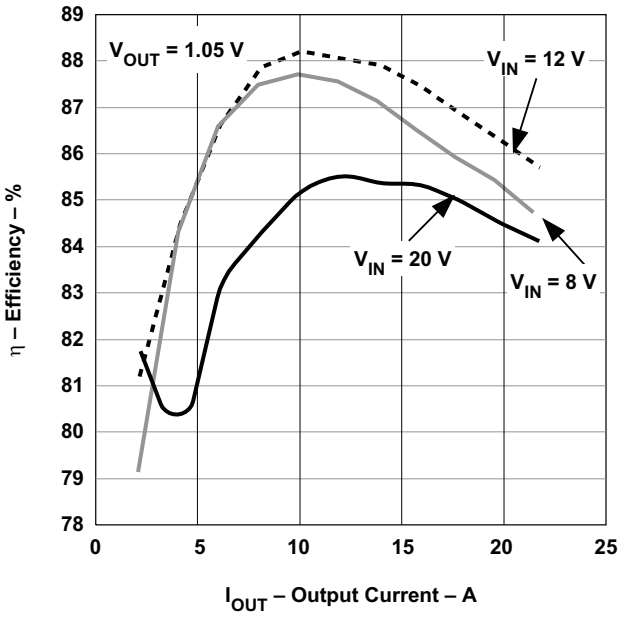


Figure 18.

EFFICIENCY vs OUTPUT CURRENT

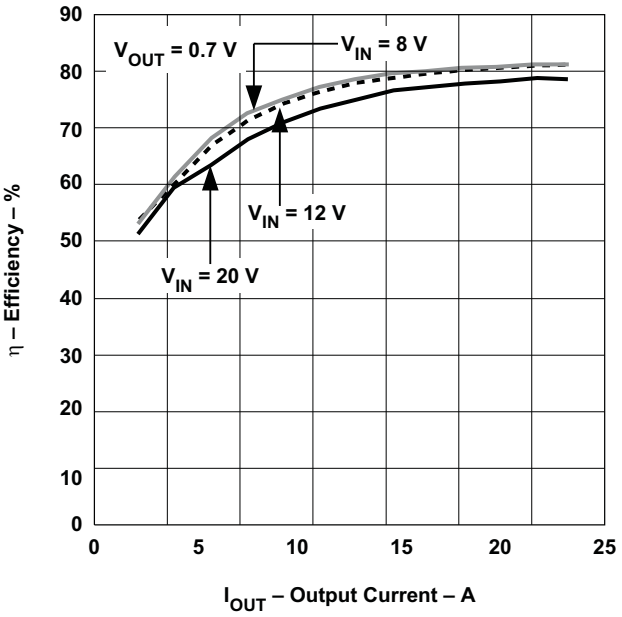


Figure 19.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY vs OUTPUT VOLTAGE

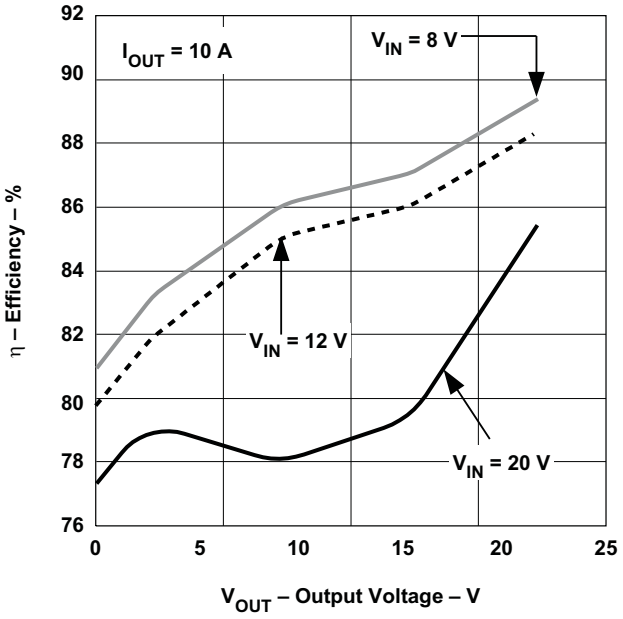


Figure 20.

EFICIENCY vs INPUT VOLTAGE

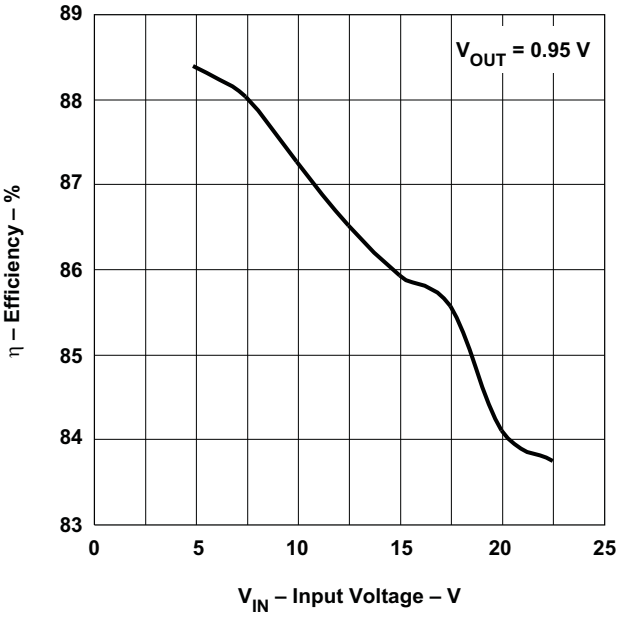


Figure 21.

SWITCHING FREQUENCY vs OUTPUT CURRENT

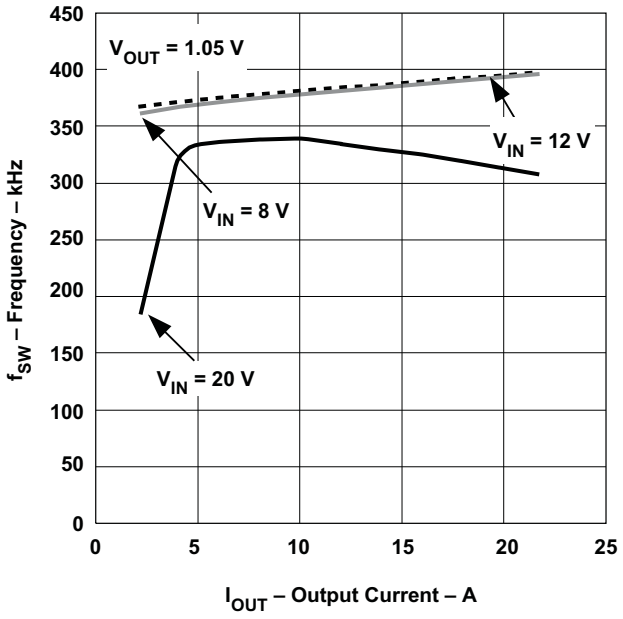


Figure 22.

SWITCHING FREQUENCY vs INPUT VOLTAGE

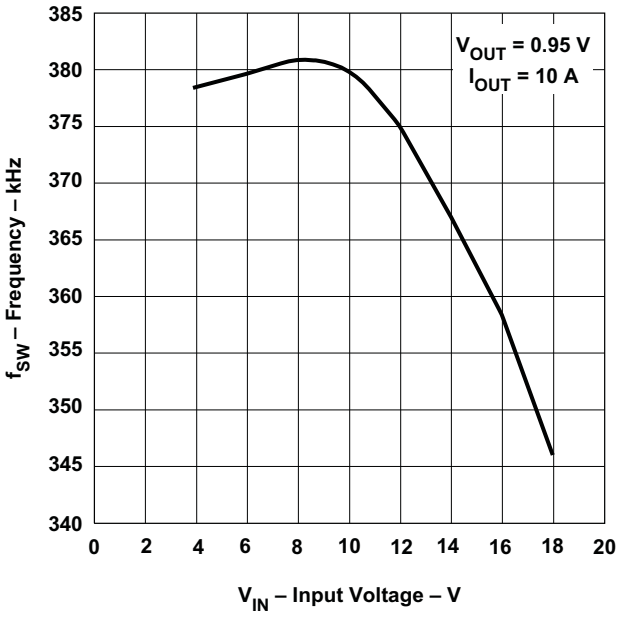


Figure 23.

TYPICAL CHARACTERISTICS (continued)

SWITCHING FREQUENCY vs OUTPUT VOLTAGE

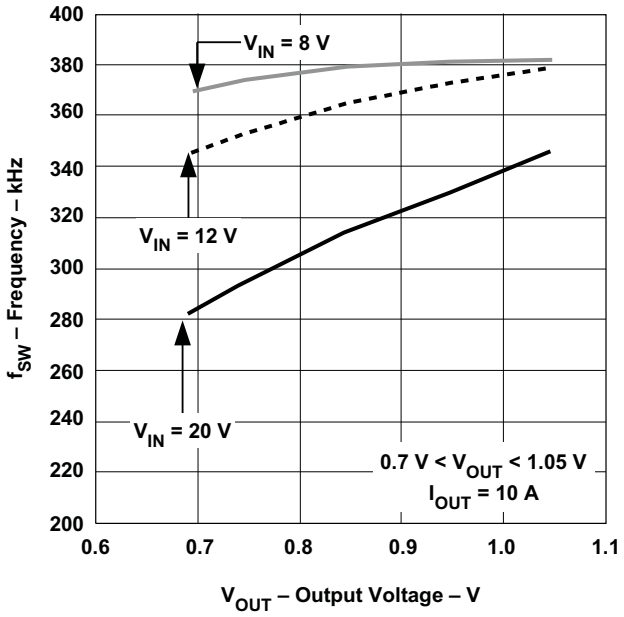


Figure 24.

REFERENCE VOLTAGE vs OUTPUT CURRENT

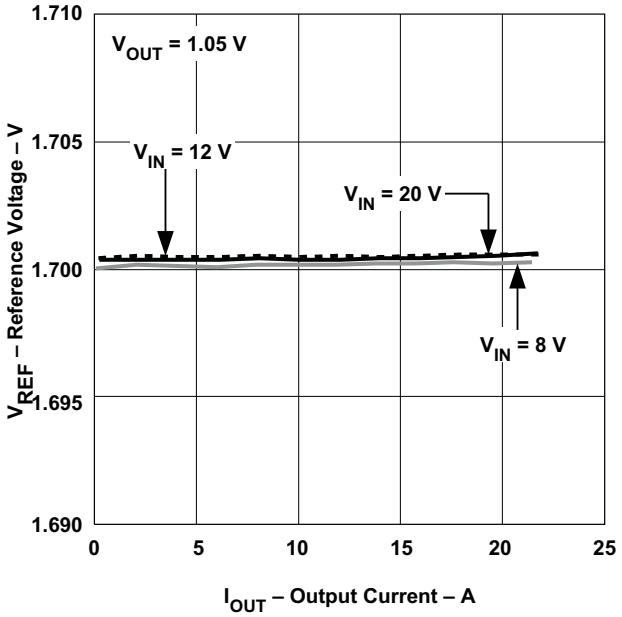


Figure 25.

CURRENT MONITOR VOLTAGE vs OUTPUT CURRENT

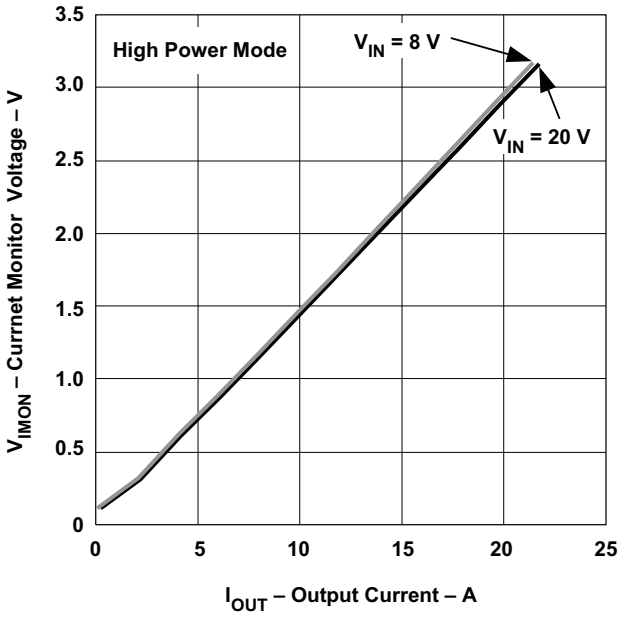


Figure 26.

SUPPLY CURRENT vs JUNCTION TEMPERATURE

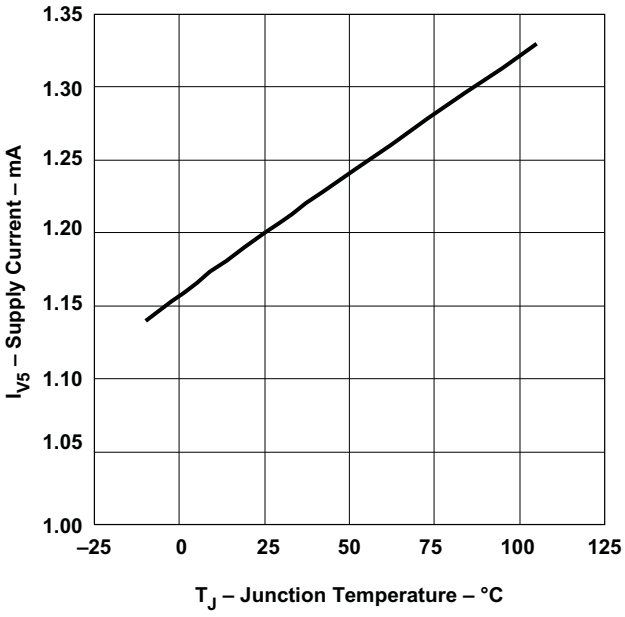


Figure 27.

TYPICAL CHARACTERISTICS (continued)

ON TIME vs JUNCTION TEMPERATURE

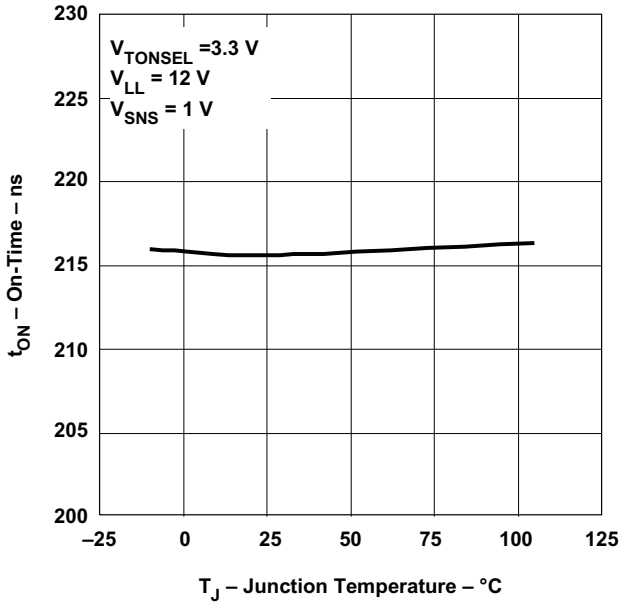


Figure 28.

DAC OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

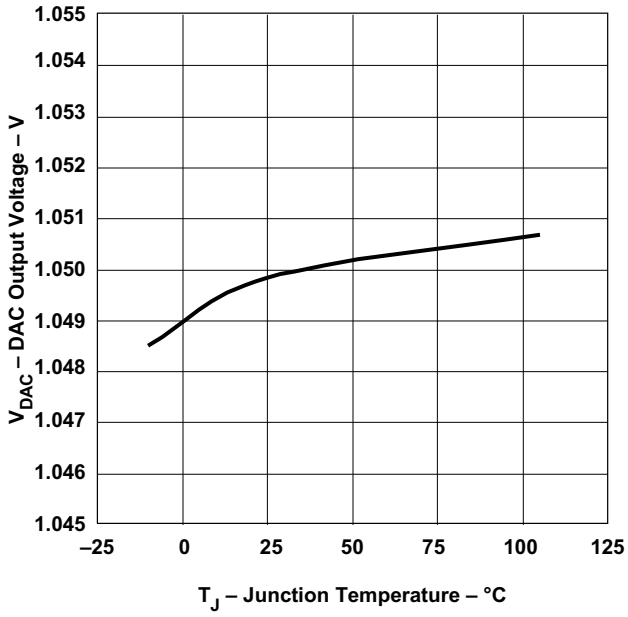


Figure 29.

REFERENCE VOLTAGE vs JUNCTION TEMPERATURE

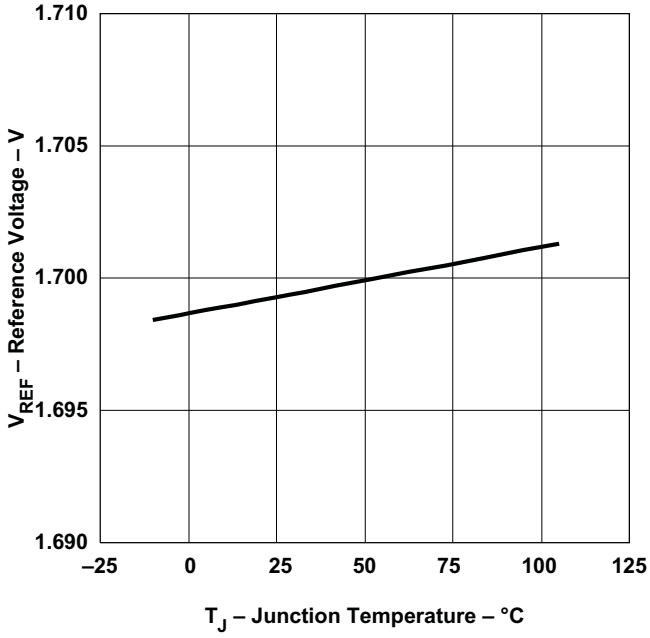


Figure 30.

TYPICAL CHARACTERISTICS

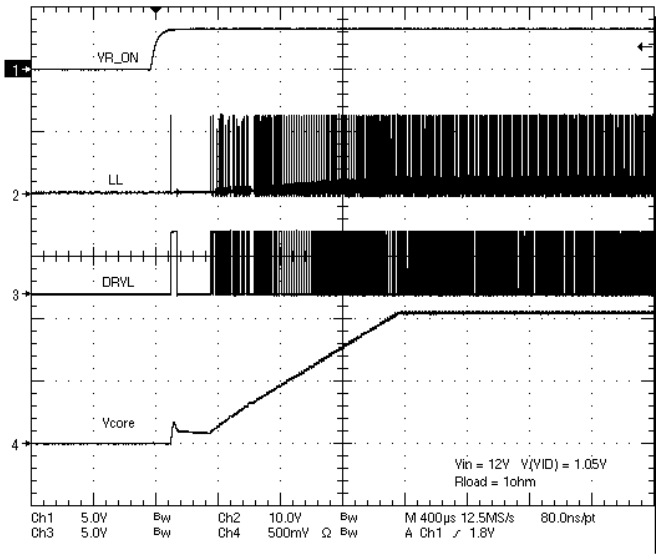


Figure 31. Startup

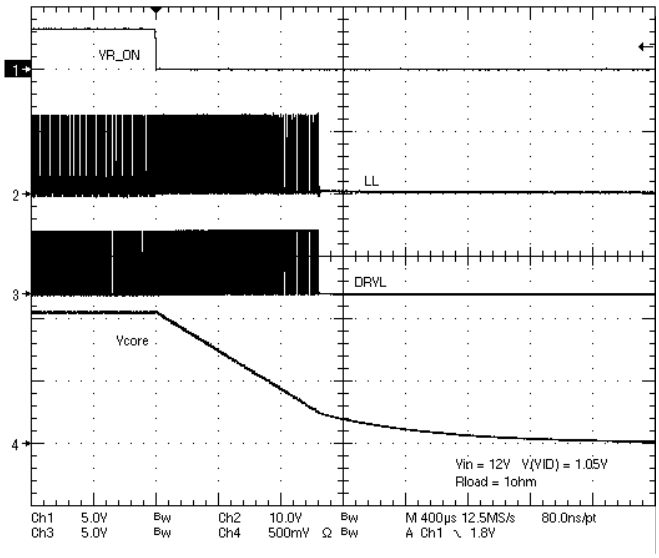


Figure 32. Soft-Stop

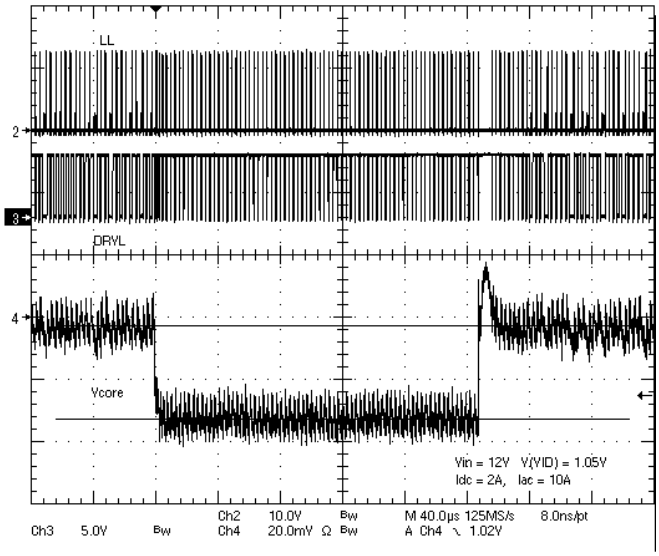


Figure 33. Load Transient Response With Droop

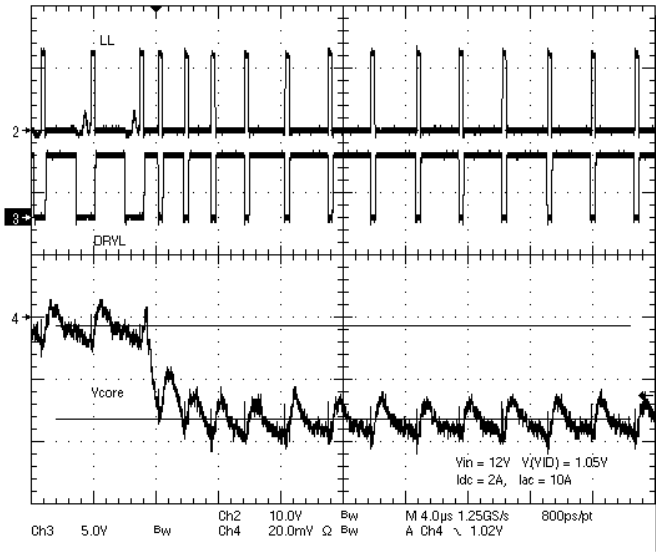


Figure 34. Load Onset With Droop

TYPICAL CHARACTERISTICS (continued)

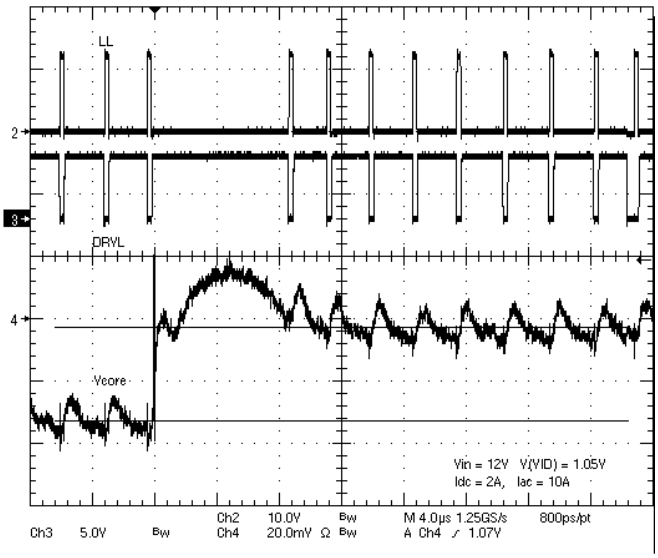


Figure 35. Transient Load Release With Droop

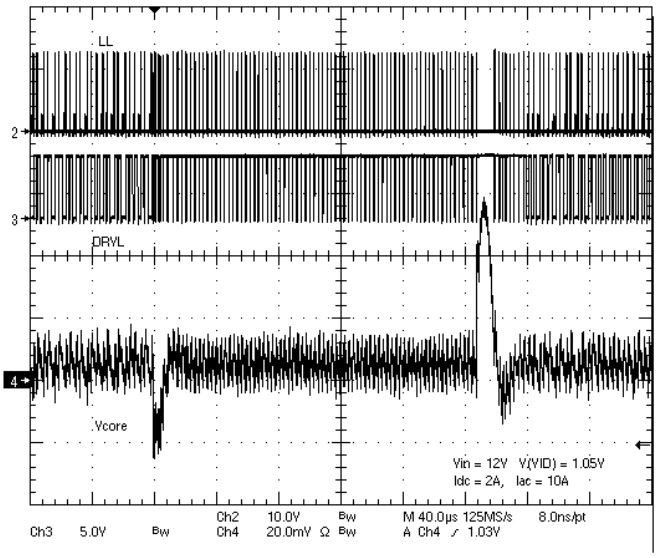


Figure 36. Transient Load Response Without Droop

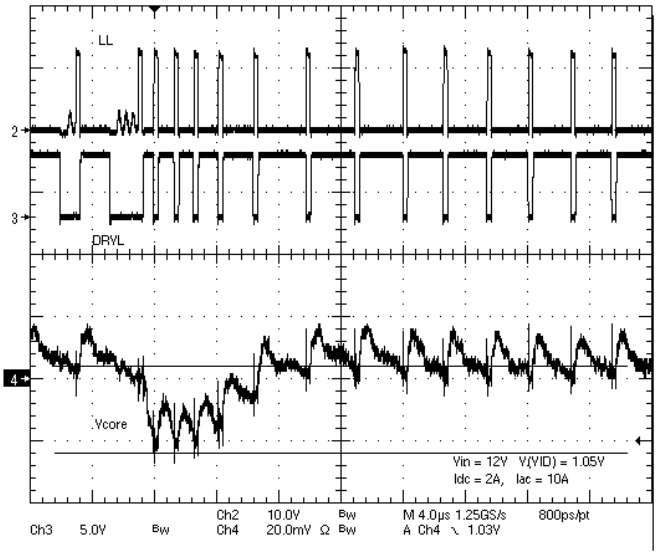


Figure 37. Transient Load Onset Without Droop

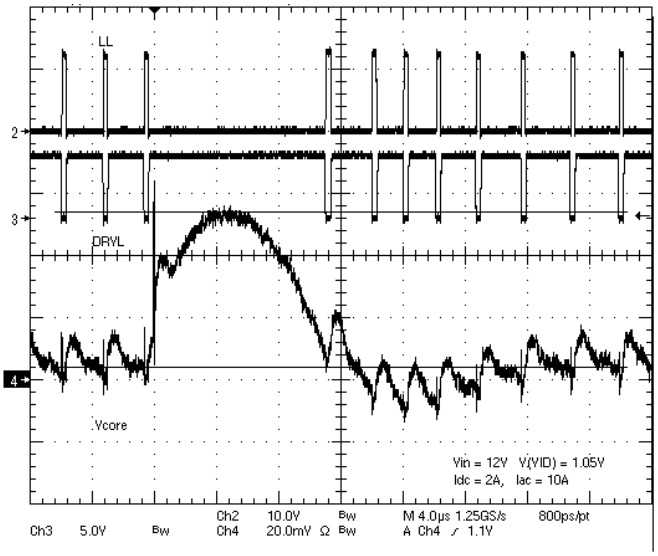


Figure 38. Transient Load Release Without Droop

REVISION HISTORY

Changes from Original (June 2009) to Revision A	Page
• Changed the FUNCTIONAL BLOCK DIAGRAM - DROOP pin number From: 32 To: 31	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51513RHBR	NRND	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 0	TPS 51513	
TPS51513RHBT	NRND	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 0	TPS 51513	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

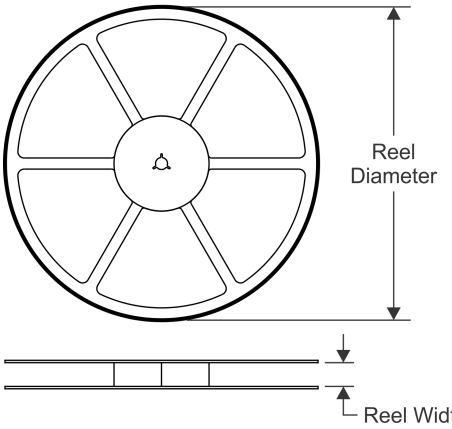
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

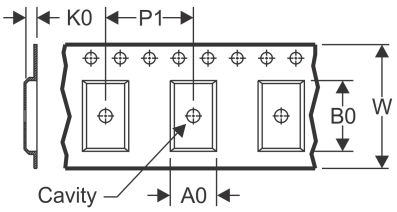
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

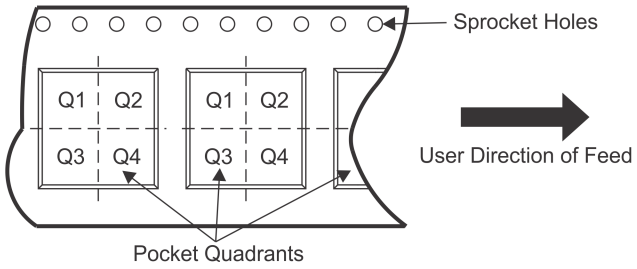


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

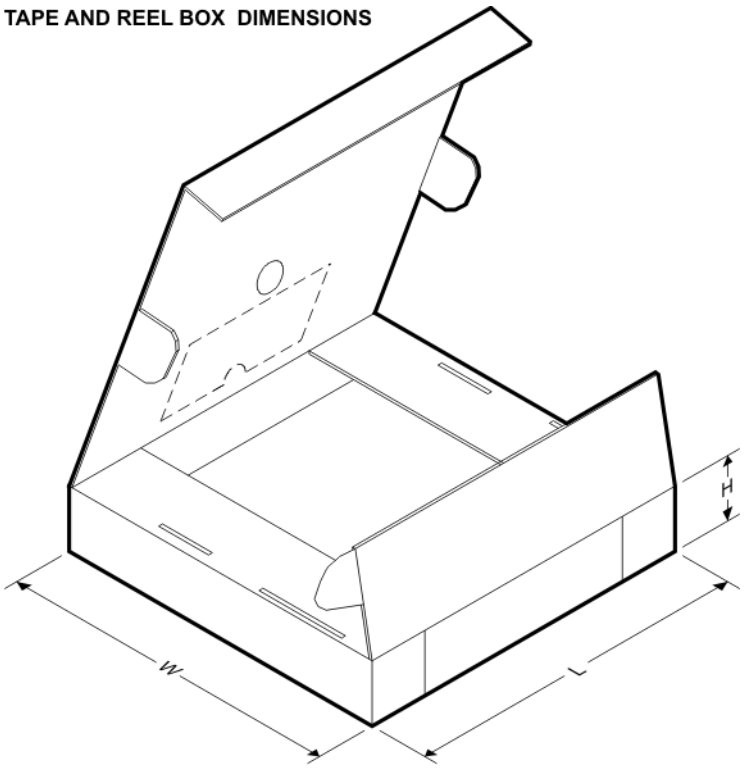
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51513RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS51513RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51513RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS51513RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

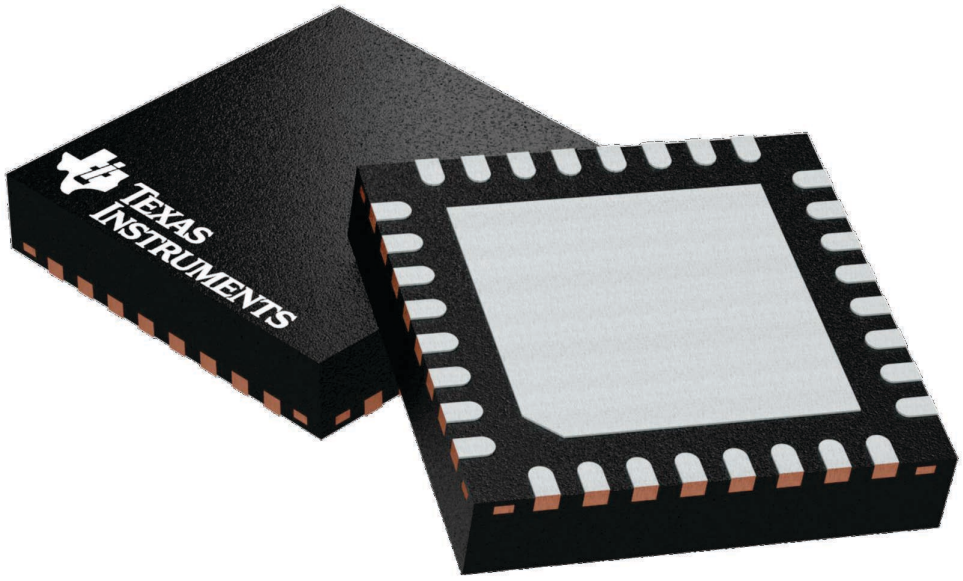
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

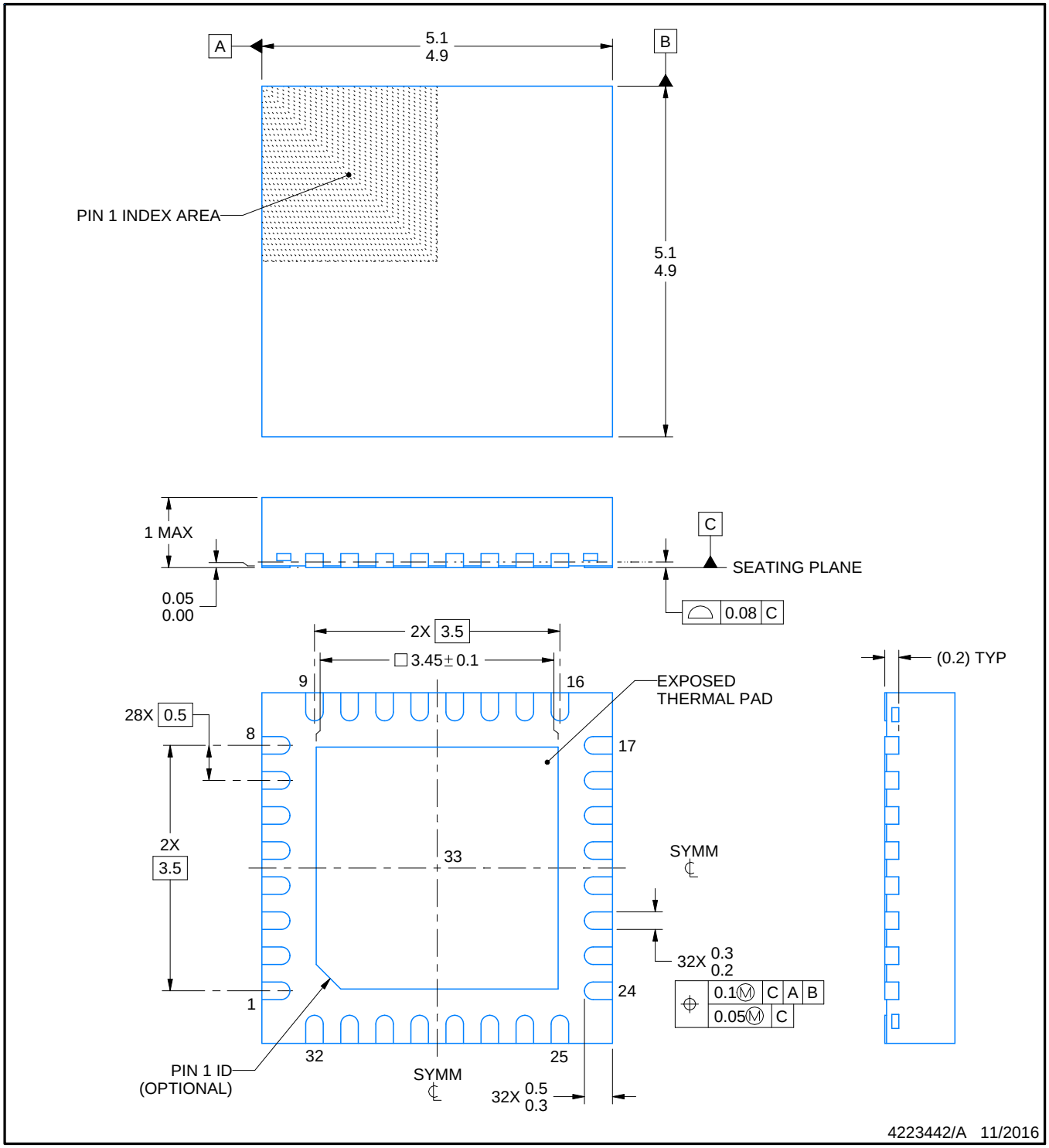
4224745/A

RHB0032E

PACKAGE OUTLINE

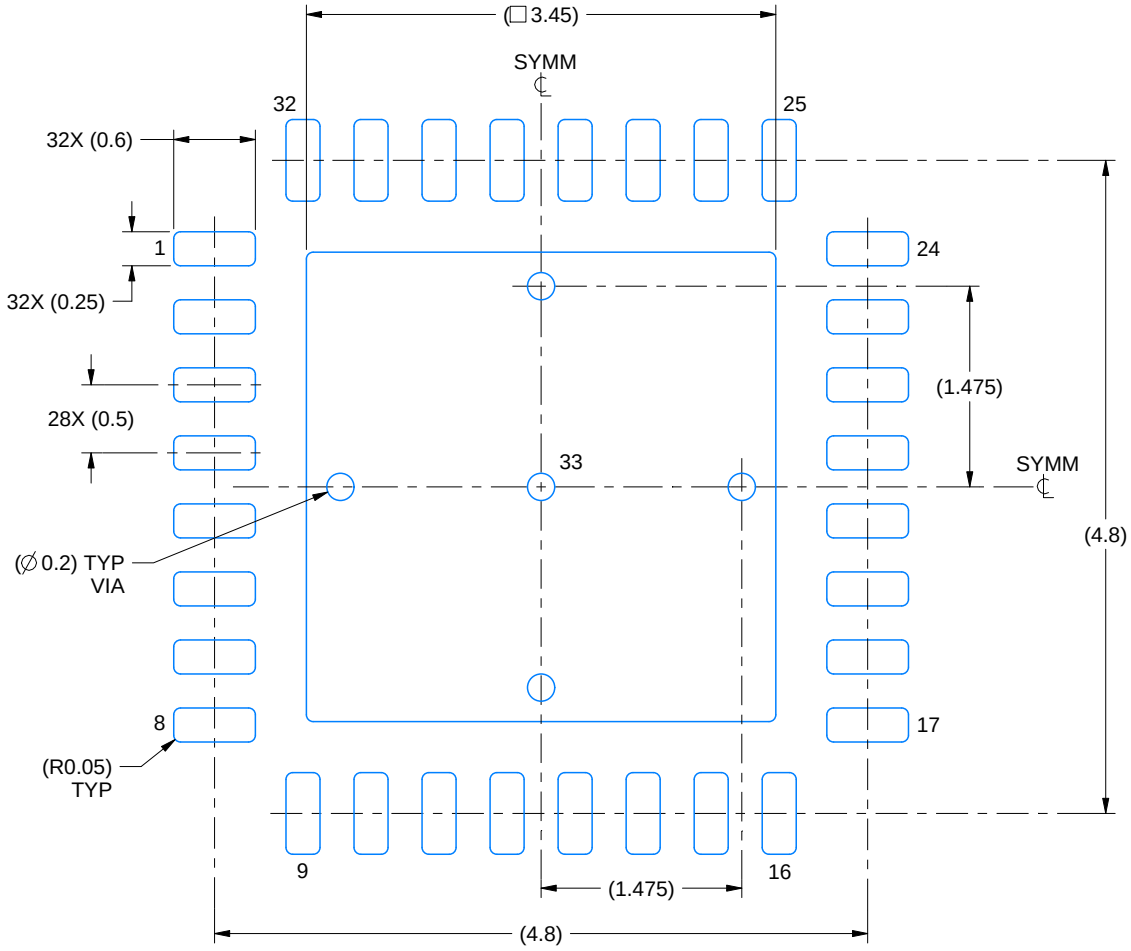
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

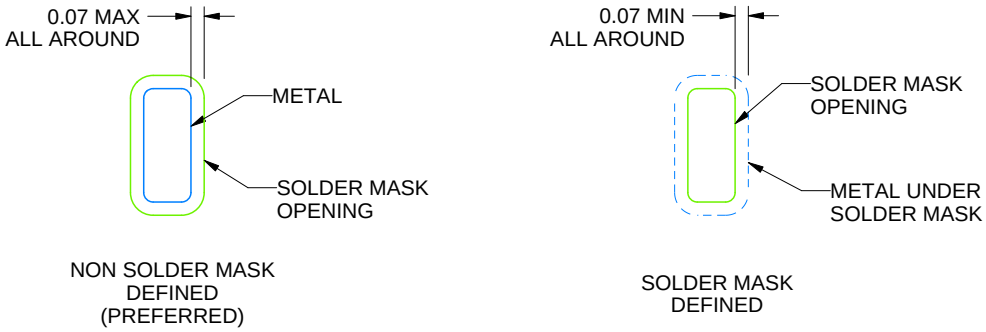


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

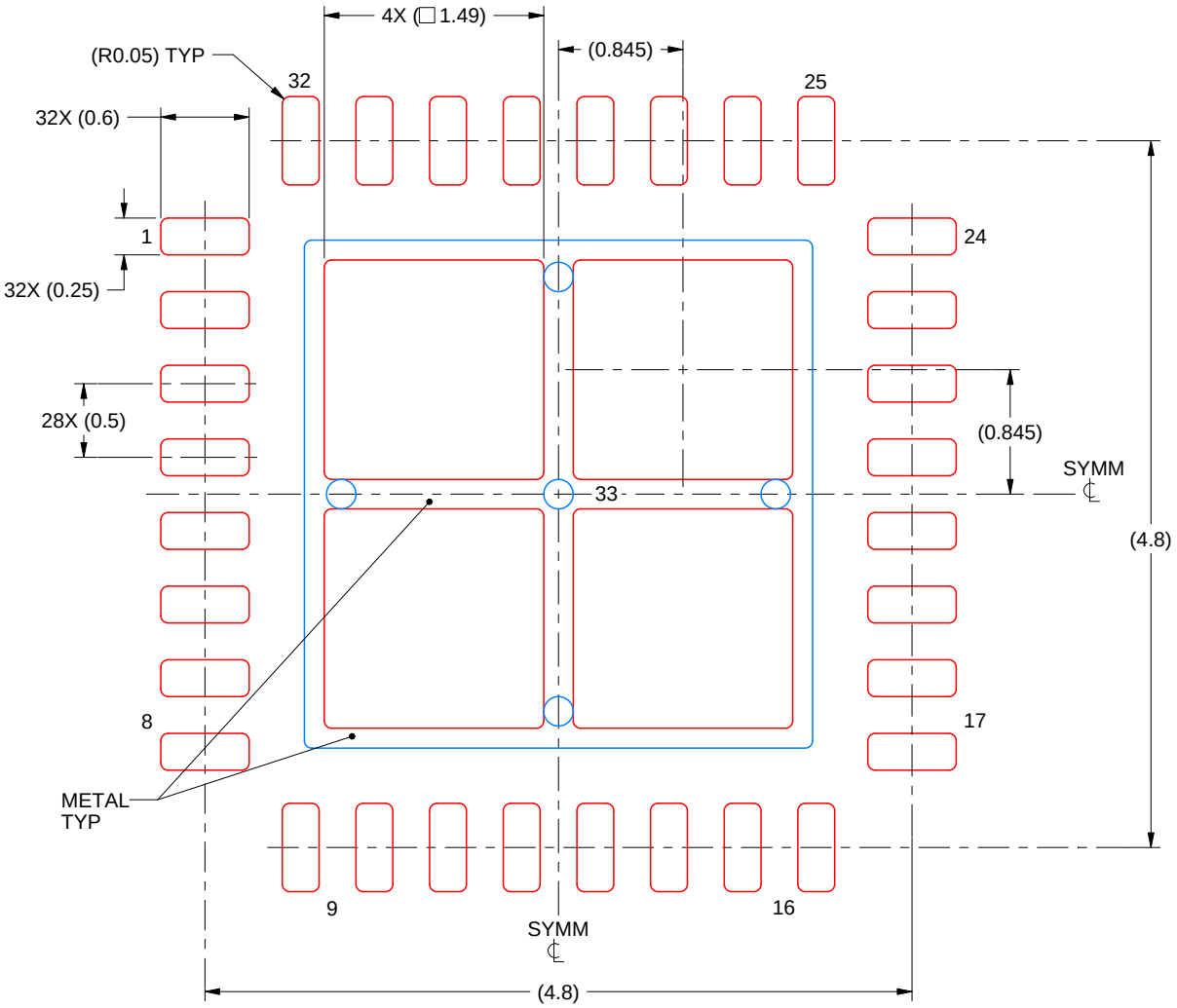


SOLDER MASK DETAILS

4223442/A 11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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