# Single-Phase, D-CAP™ and D-CAP2™ Controller with 2-Bit Flexible VID Control

**Check for Samples: TPS51518**

## FEATURES

- **Differential Voltage Feedback**
- **DC Compensation for Accurate Regulation**
- **Wide Input Voltage Range: 3 V to 28 V**
- **Flexible, 2-Bit VID Supports Output Voltage from 0.5 V to 2.0 V**
- **Adaptive On-Time Modulation with Selectable Control Architecture**
  - **D-CAP™ Mode at 350 kHz for Fast Transient Response**
  - **D-CAP2™ Mode at 350 kHz for Ultra-Low/Low ESR Output Capacitor**
- **4700 ppm/°C, Low-Side $R_{DS(on)}$ Current Sensing**
- **Programmable Soft-Start Time and Output Voltage Transition Time**
- **Built-In Output Discharge**
- **Power Good Output**
- **Integrated Boost Switch**
- **Built-In OVP/UVP/OCP**
- **Thermal Shutdown (Non-latched)**
- **3 mm × 3 mm, 20-Pin, QFN (RUK) Package**

## APPLICATIONS

- **Notebook Computers**
- **GFX Supplies**
- **System Agent for Intel Chief River Platform**

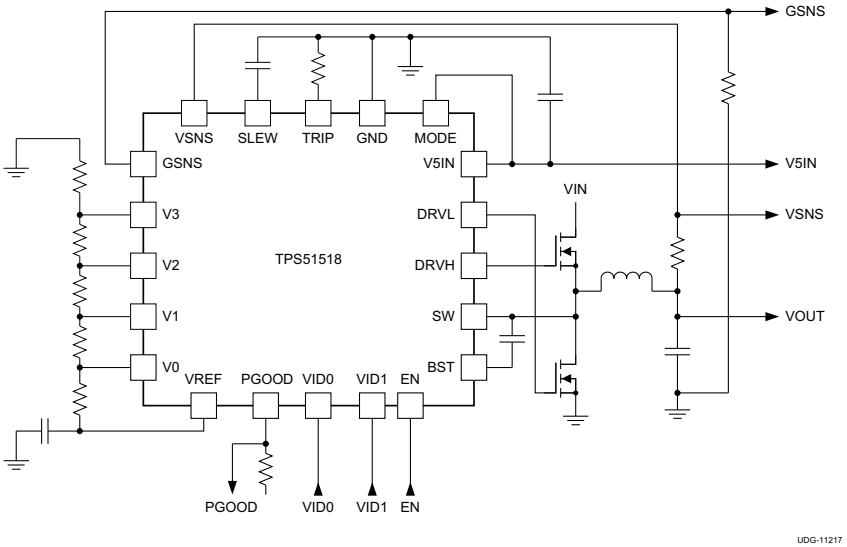
## DESCRIPTION

The TPS51518 is a single phase, D-CAP™/ D-CAP2™ synchronous buck controller with 2-bit VID inputs which can select up to four independent externally programmable output voltage levels where full external programmability in the voltage level, step setting and voltage transition slew rate is desired. It is used for GFX applications where multiple voltage levels are desired.

The TPS51518 supports all POS/SPCAP and/or all ceramic MLCC output capacitor options in applications where remote sense is a requirement. Tight DC load regulation is achieved through external programmable integrator capacitor.

The TPS51518 provides full protection suite, including OVP, OCL, 5-V UVLO and thermal shutdown. It supports the conversion voltage up to 28 V, and output voltages adjustable from 0.5 V to 2 V.

The TPS51518 is available in the 3 mm × 3 mm, QFN, 0.4-mm pitch package and is specified from –10°C to 105°C.




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP, D-CAP2 are trademarks of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)(2)

| $T_A$ | PACKAGE | ORDERABLE DEVICE NUMBER | PINS | OUTPUT SUPPLY | MINIMUM QUANTITY |
|---|---|---|---|---|---|
| –10°C to 105°C | PLASTIC QUAD FLAT PACK (QFN) | TPS51518RUKR | 20 | Tape and reel | 3000 |
| | | TPS51518RUKT | 20 | Mini reel | 250 |

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package

## ABSOLUTE MAXIMUM RATINGS(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range(2) | BST | | –0.3 | 36.0 | V |
| | BST(3) | | –0.3 | 6.0 | |
| | SW | | –5 | 30 | |
| | EN, TRIP, MODE, VID1, VID0 | | –0.3 | 5.5 | |
| | 5VIN | | –0.3 | 5.3 | |
| | SLEW, VSNS | | –0.3 | 3.6 | |
| | GSNS | | –0.35 | 0.35 | |
| | GND | | –0.3 | 0.3 | |
| Output voltage range(2) | DRVH | | –5 | 36 | V |
| | DRVH(3) | | –0.3 | 6.0 | |
| | DRVL | | –0.3 | 6.0 | |
| | | transient < 20 ns | –2.0 | 6.0 | |
| | PGOOD | | –0.3 | 6.0 | |
| | VREF, V0, V1, V2, V3 | | –0.3 | 3.6 | |
| Junction temperature, $T_J$ | | | –40 | 125 | °C |
| Storage temperature, $T_{STG}$ | | | –55 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

## RECOMMENDED OPERATING CONDITIONS(1)(2)

| | | | VALUE | | |
|---|---|---|---|---|---|
| | | | MIN | MAX | UNIT |
| Supply voltage | V5IN | | 4.50 | 5.25 | V |
| Input voltage range | BST | | –0.1 | 33.5 | V |
| | BST(1) | | –0.1 | 5.5 | |
| | SW | | –3 | 28 | |
| | SW(2) | | –4.5 | 28.0 | |
| | EN, TRIP, MODE, VID1, VID0 | | –0.1 | 5.5 | |
| | SLEW, VSNS | | –0.1 | 3.5 | |
| | GSNS | | –0.3 | 0.3 | |
| | GND | | –0.1 | 0.1 | |
| Output voltage range | DRVH | | –3.0 | 33.5 | V |
| | DRVH(2) | | –4.5 | 33.5 | |
| | DRVH(1) | | –0.1 | 5.5 | |
| | DRVL | | –0.1 | 5.5 | |
| | | transient < 20 ns | –1.5 | 5.5 | |
| | PGOOD | | –0.1 | 5.5 | |
| | VREF, V0, V1, V2, V3 | | –0.1 | 3.5 | |
| Operating free-air temperature, $T_A$ | | | –10 | 105 | °C |

(1) Voltage values are with respect to the SW terminal.
(2) This voltage should be applied for less than 30% of the repetitive period.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS51518 | UNITS |
|---|---|---|---|
| | | RUK (20) PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 94.1 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 58.1 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 64.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 31.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 58.0 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 5.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{V5IN}$= 5 V, $V_{MODE}$= 5 V, $V_{EN}$= 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{V5IN}$ | V5IN supply current | $T_A$ = 25°C, No load, $V_{EN}$ = 5 V, $V_{MODE}$ = 5 V | | 560 | | µA |
| $I_{V5SDN}$ | V5IN shutdown current | $T_A$ = 25°C, No load, $V_{EN}$ = 0 V | | 1 | | µA |
| **VREF OUTPUT** | | | | | | |
| $V_{VREF}$ | Output voltage | $I_{VREF}$ = 30 µA, w/r/t GSNS | | 2.000 | | V |
| $V_{VREFTOL}$ | Output voltage tolerance | 0 µA ≦ $I_{VREF}$ < 30 µA, 0°C ≦ $T_A$ < 85°C | –0.8% | | 0.8% | |
| | | 0 µA ≦ $I_{VREF}$ < 300 µA, –10°C ≦ $T_A$ < 105°C | –1% | | 1% | |
| $I_{VREFOCL}$ | Current limit | $V_{VREF-GSNS}$ = 1.7 V | 0.4 | 1.0 | | mA |
| **OUTPUT VOLTAGE** | | | | | | |
| $V_{SLEWCLP}$ | SLEW clamp voltage | $V_{REFIN}$ = 1 V | 0.92 | | 1.08 | V |
| $g_M$ | Error amplifier transconductance | $V_{REFIN}$ = 1 V | | 60 | | µS |
| $I_{VSNS}$ | VSNS input current | $V_{VSNS}$ = 1.0 V | –1 | | 1 | µA |
| $I_{VSNSDIS}$ | VSNS discharge current | $V_{EN}$ = 0 V, $V_{VSNS}$ = 0.5 V, $V_{MODE}$ = 0 V | | 12 | | mA |
| **SMPS FREQUENCY** | | | | | | |
| $f_{SW}$ | Switching frequency | $V_{IN}$ = 12 V, $V_{VSNS}$ = 1.0 V, $V_{MODE}$ = 0 V | | 350 | | kHz |
| $t_{ON(min)}$ | Minimum on-time | DRVH rising to falling | | 40 | | ns |
| $t_{OFF(min)}$ | Minimum off-time | DRVH falling to rising | | 320 | | ns |
| **DRIVERS** | | | | | | |
| $R_{DH}$ | High-side driver resistance | Source, $I_{DRVH}$ = 50 mA | | 1.7 | | Ω |
| | | Sink, $I_{DRVH}$ = 50 mA | | 0.8 | | Ω |
| $R_{DL}$ | Low-side driver resistance | Source, $I_{DRVL}$ = 50 mA | | 1.1 | | Ω |
| | | Sink, $I_{DRVL}$ = 50 mA | | 0.6 | | Ω |
| **INTERNAL BOOT STRAP SW** | | | | | | |
| $V_{FBST}$ | Forward voltage | $V_{V5IN-BST}$, $T_A$ = 25°C, $I_F$ = 10 mA | | 0.1 | 0.2 | V |
| $I_{BST}$ | BST leakage current | $T_A$ = 25°C, $V_{BST}$ = 33 V, $V_{SW}$ = 28 V | | 0.01 | 1.50 | µA |
| **LOGIC THRESHOLD AND TIMING** | | | | | | |
| $V_{VIDx(LL)}$ | VID1/VID0 low-level voltage | | | | 0.3 | V |
| $V_{VIDx(LH)}$ | VID1/VID0 high-level voltage | | 0.9 | | | V |
| $V_{VIDx(HYST)}$ | VID1/VID0 hysteresis voltage | | | 0.4 | | V |
| $I_{VIDx(LLK)}$ | VID1/VID0 input leakage current | | –1 | 0 | 1 | µA |
| $V_{EN(LL)}$ | EN low-level voltage | | | | 0.5 | V |
| $V_{EN(LH)}$ | EN high-level voltage | | 1.5 | | | V |
| $V_{EN(HYST)}$ | EN hysteresis voltage | | | 0.25 | | V |
| $I_{EN(LLK)}$ | EN input leakage current | | –1 | | 1 | nA |
| **SOFT START/SLEW RATE** | | | | | | |
| $I_{SS}$ | Soft-start current | Soft-start current source | | 10 | | µA |
| $I_{SLEW}$ | Slew control current | | | 50 | | µA |

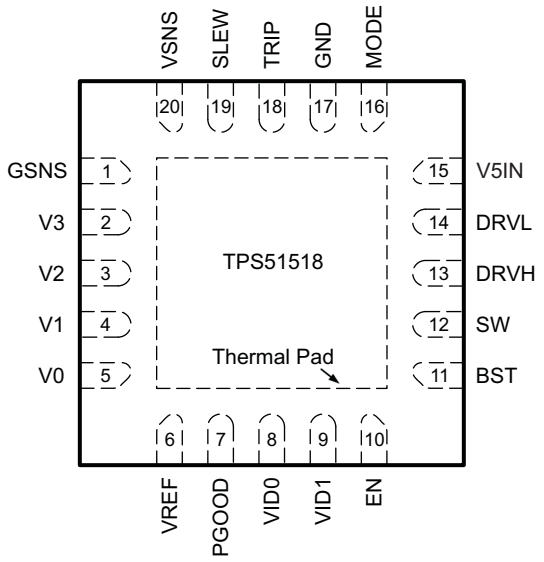
## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{V5IN}$= 5 V, $V_{MODE}$= 5 V, $V_{EN}$= 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PGOOD COMPARATOR** | | | | | | |
| $V_{PGTH}$ | PGOOD threshold | PGOOD in from higher | | 108% | | |
| | | PGOOD in from lower | | 92% | | |
| | | PGOOD out to higher | | 116% | | |
| | | PGOOD out to lower | | 84% | | |
| $I_{PG}$ | PGOOD sink current | $V_{PGOOD}$ = 0.5 V | | 6.0 | | mA |
| $t_{PGDLY}$ | PGOOD delay time | Delay for PGOOD in | | 1 | | ms |
| | | Delay for PGOOD out | | 0.2 | | µs |
| $t_{PGCMPSS}$ | PGOOD start-up delay time | PGOOD comparator wake up delay | | 1.5 | | ms |
| $I_{PGLK}$ | PGOOD leakage current | | –1 | 0 | 1 | µA |
| **CURRENT DETECTION** | | | | | | |
| $I_{TRIP}$ | TRIP source current | $T_A$ = 25°C, $V_{TRIP}$ = 0.4 V | 9 | 10 | 11 | µA |
| $TC_{ITRIP}$ | TRIP source current temperature coefficient(1) | | | 4700 | | ppm/°C |
| $V_{TRIP}$ | VTRIP voltage range | | 0.2 | | 3 | V |
| $V_{OCL}$ | Current limit threshold | $V_{TRIP}$ = 3.0 V | 360 | 375 | 390 | mV |
| | | $V_{TRIP}$ = 1.6 V | 190 | 200 | 210 | |
| | | $V_{TRIP}$ = 0.2 V | 20 | 25 | 30 | |
| $V_{OCLN}$ | Negative current limit threshold | $V_{TRIP}$ = 3.0 V | –390 | –375 | –360 | mV |
| | | $V_{TRIP}$ = 1.6 V | –212 | –200 | –188 | |
| | | $V_{TRIP}$ = 0.2 V | –30 | –25 | –20 | |
| $V_{ZC}$ | Zero cross detection offset | | | 0 | | mV |
| **PROTECTIONS** | | | | | | |
| $V_{UVLO}$ | V5IN UVLO threshold voltage | Wake-up | 4.3 | 4.4 | 4.6 | V |
| | | Shutdown | 3.8 | 4.0 | 4.2 | |
| $V_{OVP}$ | OVP threshold voltage | OVP detect voltage | 118% | 120% | 122% | |
| $t_{OVPDLY}$ | OVP propagation delay | With 100-mV overdrive | | 300 | | ns |
| $V_{UVP}$ | UVP threshold voltage | UVP detect voltage | 66% | 68% | 70% | |
| $t_{UVPDLY}$ | UVP delay | | | 1 | | ms |
| $t_{UVPENDLY}$ | UVP enable delay | | | 1.4 | | ms |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold(1) | Shutdown temperature | | 140 | | °C |
| | | Hysteresis | | 10 | | |

(1) Ensured by design. Not production tested.

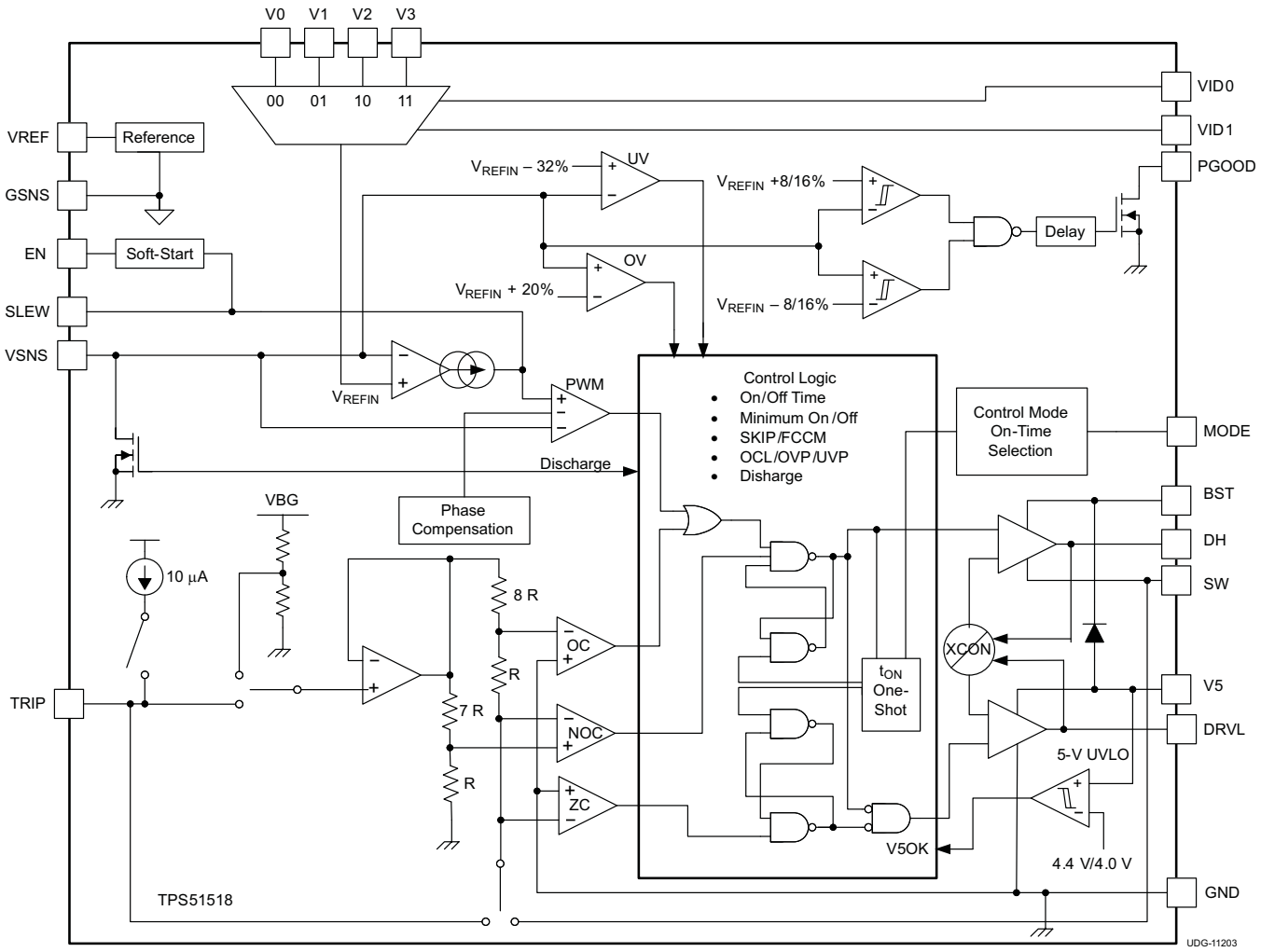
## DEVICE INFORMATION




## PIN DESCRIPTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| No. | NAME | | |
| 11 | BST | I | Supply input for high-side MOSFET driver (bootstrap terminal). Connect a capacitor from this pin to the SW pin. Internally connected to V5IN via the bootstrap MOSFET switch. |
| 13 | DRVH | O | High-side MOSFET gate driver output. |
| 14 | DRVL | O | Synchronous low-side MOSFET gate driver output. |
| 10 | EN | I | Enable input for the device. Support 3.3-V logic |
| 17 | GND | I | Combined AGND and PGND point. The positive on-resistance current sensing input. |
| 1 | GSNS | I | Voltage sense return tied directly to GND sense point of the load. Tie to GND with a 10-Ω resistor to close feedback if die sensing is used. Short to GND if remote sense is not used. |
| 16 | MODE | I | See Table 2. |
| 7 | PGOOD | O | PGOOD output. Connect pull-up resistor. |
| 19 | SLEW | I | Program the startup using 10 µA and voltage transition time using 50 µA from an external capacitor via current source. |
| 12 | SW | I/O | High-side MOSFET gate driver return. The $R_{DS(on)}$ current sensing input (–). |
| 18 | TRIP | I | Connect resistor to GND to set OCL at $V_{TRIP}$/8. Output 10 µA current at room temperature, $T_C$ = 4700ppm/°C. |
| 5 | V0 | I | Voltage set-point programming resistor input, corresponding to 00 |
| 4 | V1 | I | Voltage set-point programming resistor input, corresponding to 01 |
| 3 | V2 | I | Voltage set-point programming resistor input, corresponding to 10 |
| 2 | V3 | I | Voltage set-point programming resistor input, corresponding to 11 |
| 15 | V5IN | I | 5-V power supply input for internal circuits and MOSFET gate drivers |
| 8 | VID0 | I | Logic input for set-point voltage selector. Use in conjunction with VID1 pin to select among four set-point reference voltages. Support 1-V and 3.3-V logic. |
| 9 | VID1 | I | Logic input for set-point voltage selector. Use in conjunction with VID0 pin to select among four set-point reference voltages. Support 1-V and 3.3-V logic. |
| 6 | VREF | O | 2 V, 300-µA voltage reference. Bypass to GND with a 1-µF ceramic capacitor. |
| 20 | VSNS | I | Voltage sense return tied directly to the load voltage sense point. Tie to $V_{OUT}$ with a 10-Ω resistor to close feedback if die sensing is used. |
| Thermal Pad | | | Connect directly to system GND plane with multiple vias. |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

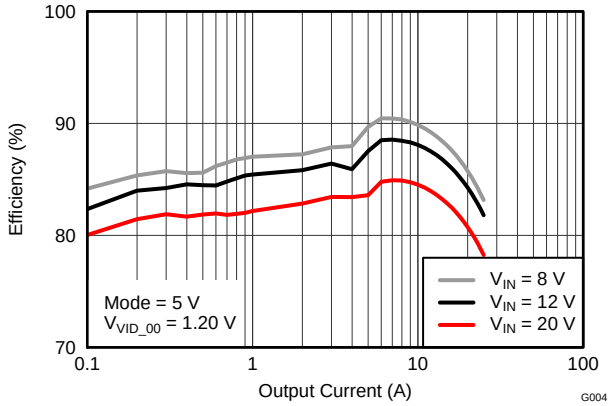



**Figure 1. GFX Efficiency**

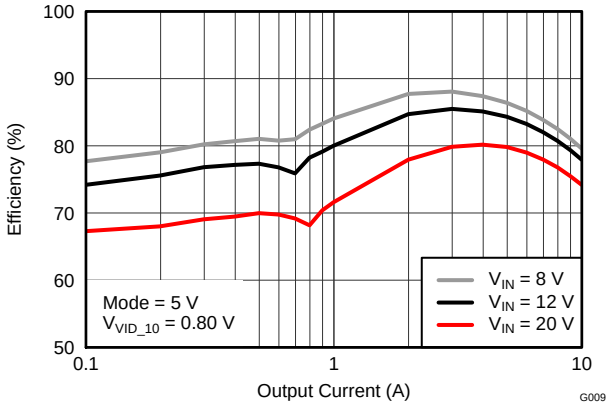



**Figure 2. SA Efficiency**

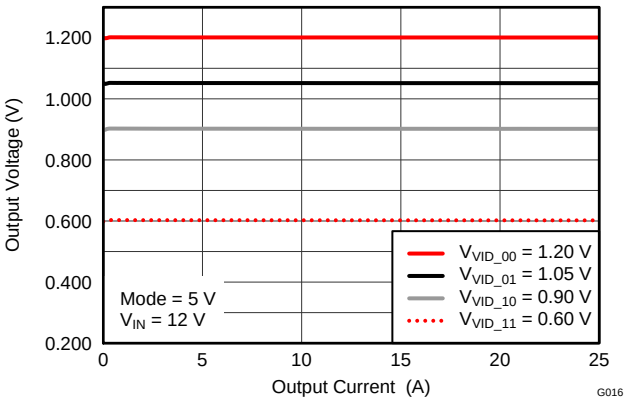



**Figure 3. GFX Load Regulation**

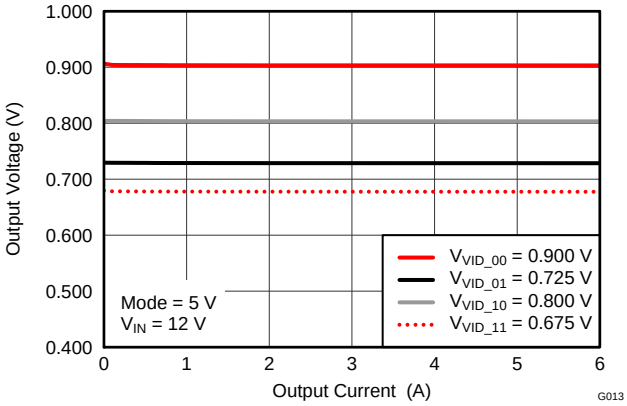



**Figure 4. SA Load Regulation**

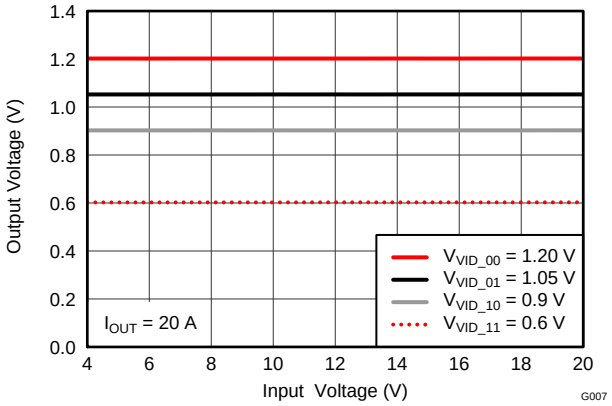



**Figure 5. GFX Line Regulation**

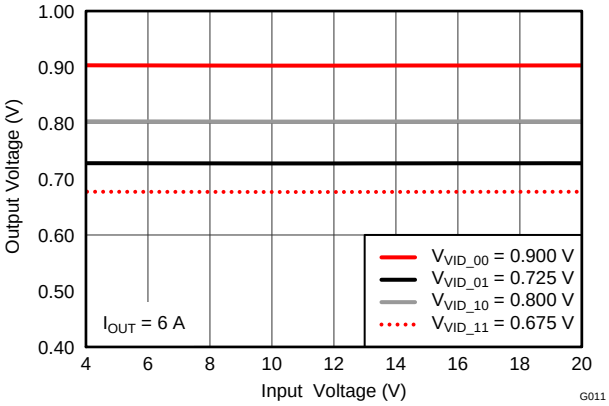



**Figure 6. SA Line Regulation**

## TYPICAL CHARACTERISTICS (continued)

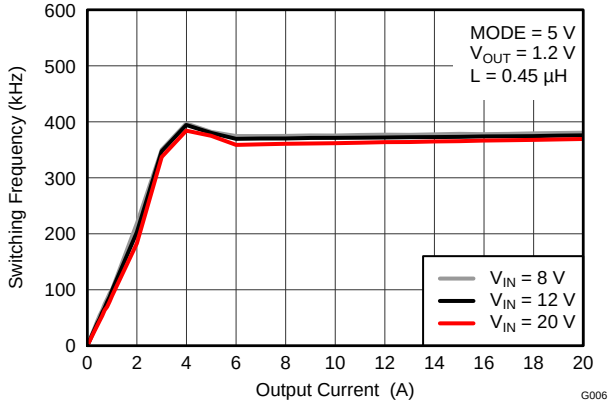



**Figure 7. GFX Frequency vs. Load Current**

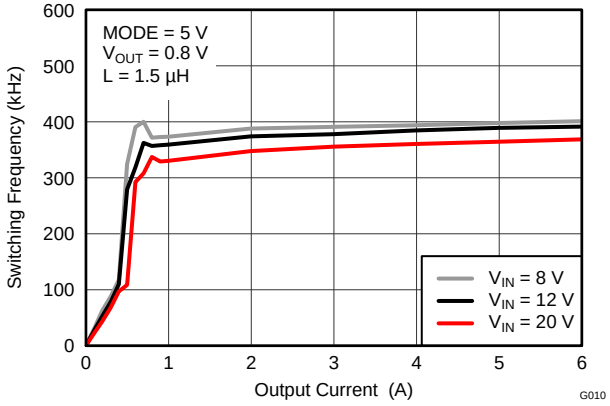



**Figure 8. SA Frequency vs. Load Current**

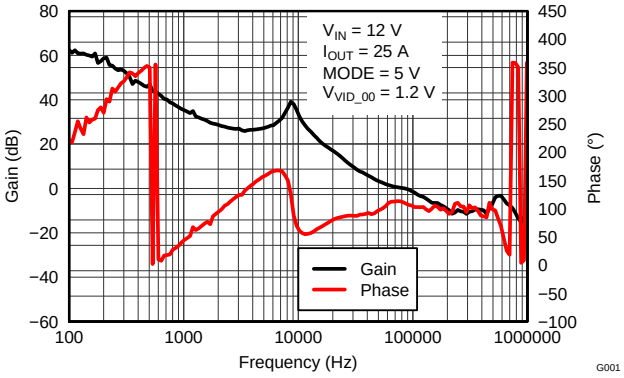



**Figure 9. GFX Bode Plot**

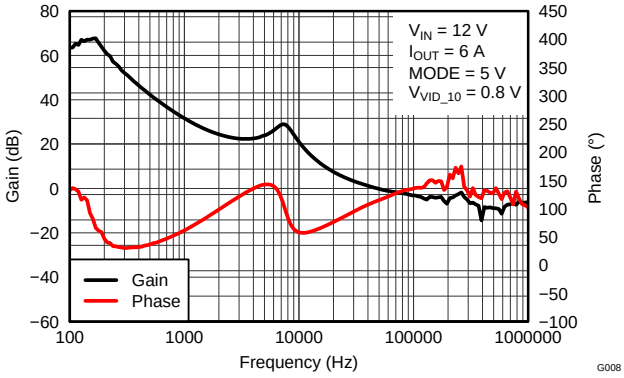



**Figure 10. SA Bode Plot**

## TYPICAL CHARACTERISTICS

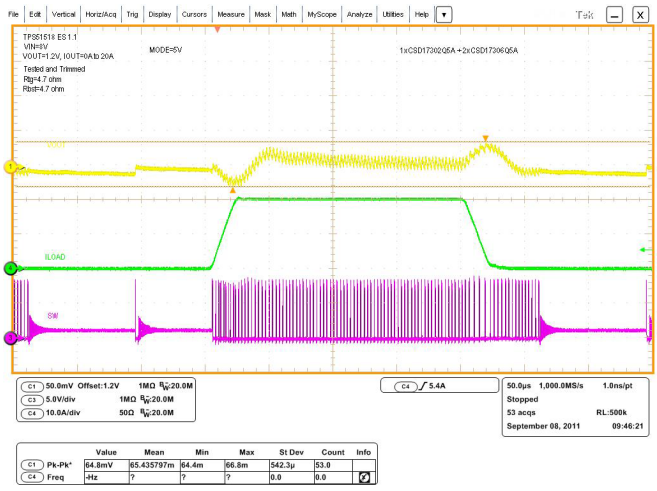



Figure 11. Load Transient

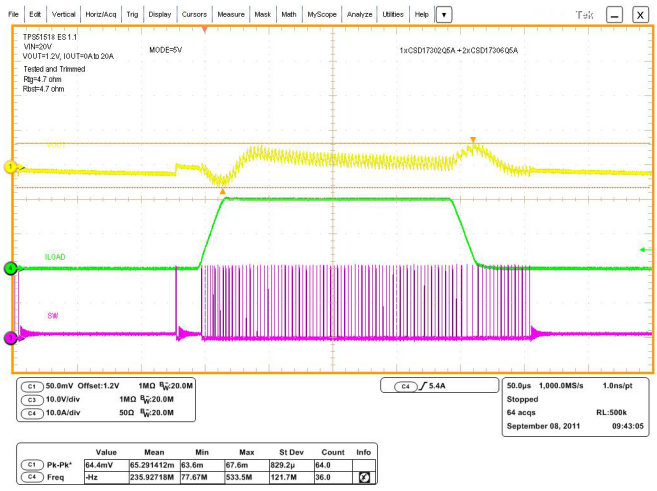



Figure 12. Load Transient

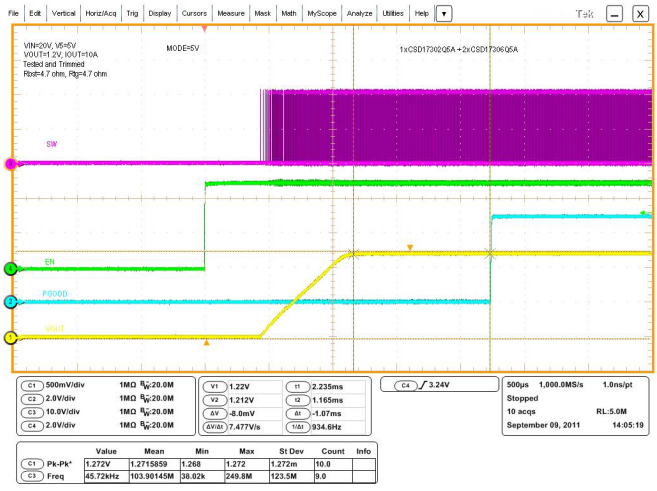



Figure 13. Startup

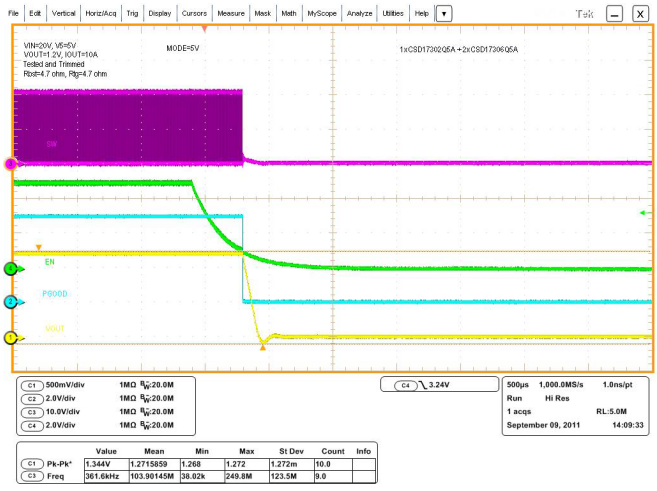



Figure 14. Shutdown

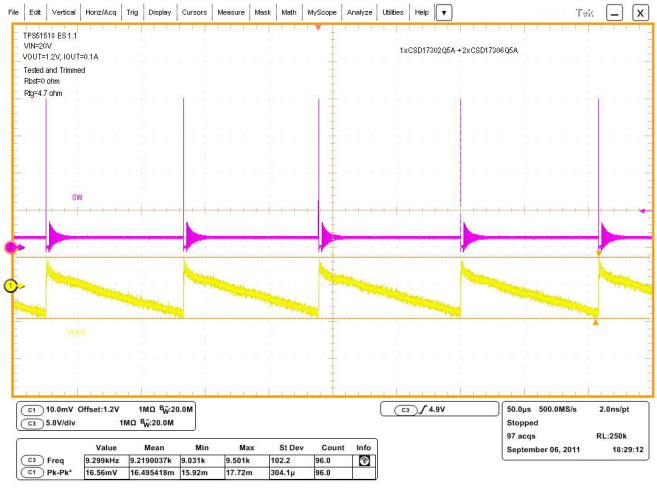



Figure 15. Steady-State Ripple, $I_{LOAD}$ = 0.1 A

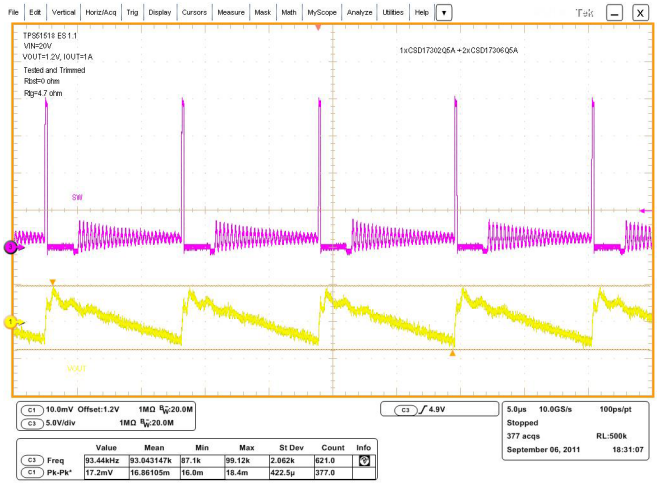



Figure 16. Steady-State Ripple, $I_{LOAD}$ = 1 A

## TYPICAL CHARACTERISTICS (continued)

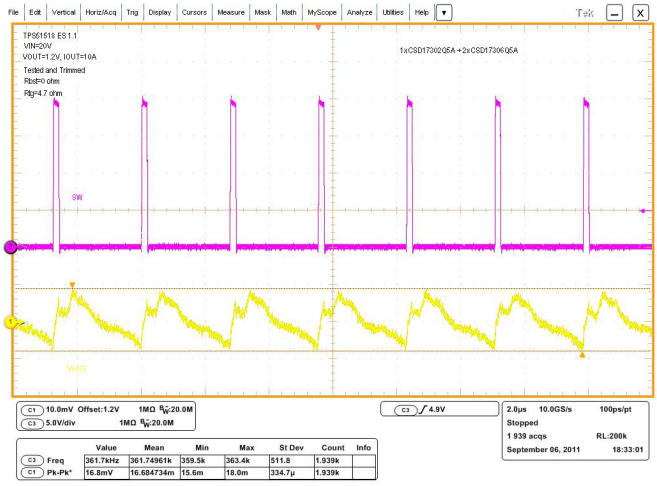



Figure 17. Steady-State Ripple, $I_{LOAD}$ = 10 A

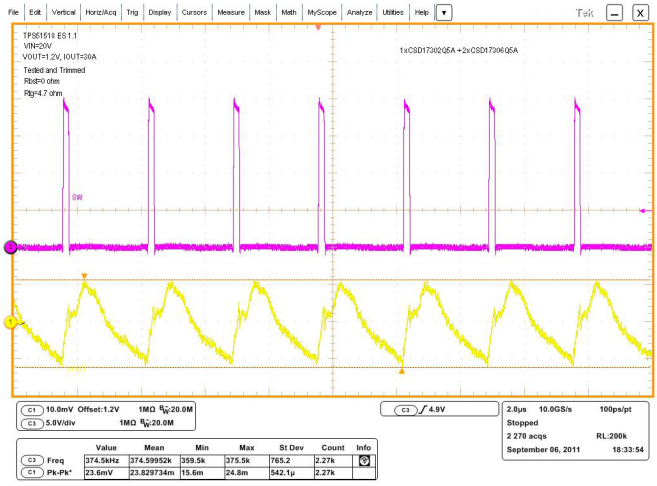



Figure 18. Steady-State Ripple, $I_{LOAD}$ = 30 A

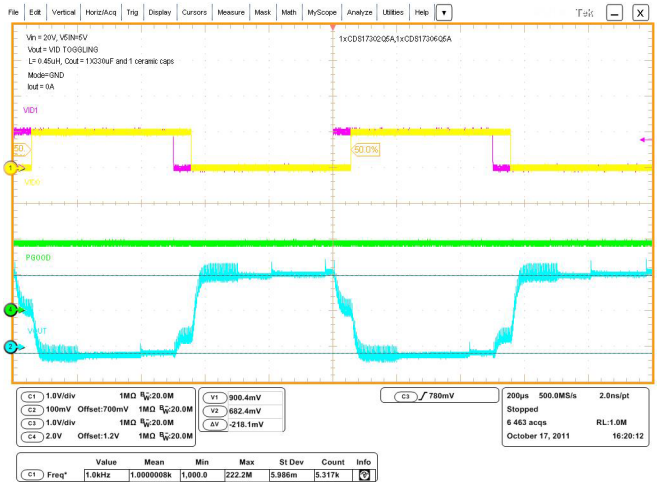



Figure 19. VID transition, $I_{LOAD}$ = 0 A

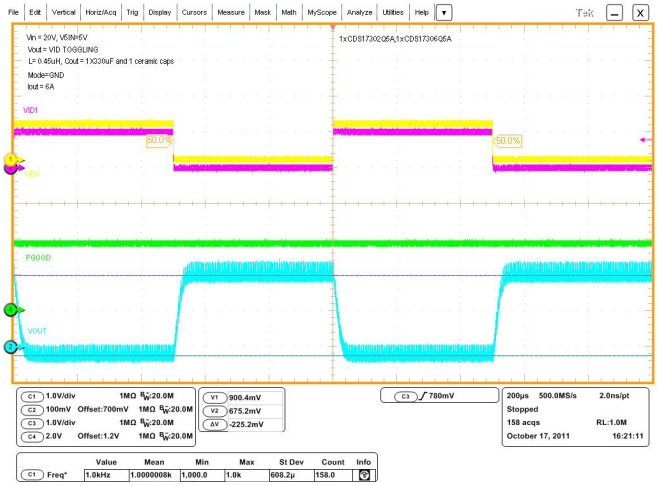



Figure 20. VID transition, $I_{LOAD}$ = 6 A

## Switch Mode Power Supply Control

The TPS51518 is a high performance, single-synchronous step-down controller with differential voltage feedback. It realizes accurate regulation at the specific load point over wide load range.

The TPS51518 supports two control architectures, D-CAP™ mode and D-CAP2™ mode. Both control modes do not require complex external compensation networks and are suitable for designs with small external components counts. The D-CAP™ mode provides fast transient response with appropriate amount of equivalent series resistance (ESR) on the output capacitors. The D-CAP2™ mode is dedicated for a configuration with very low ESR output capacitors such as multi-layer ceramic capacitors (MLCC). For the both modes, an adaptive on-time control scheme is used to achieve pseudo-constant frequency. The TPS51518 adjusts the on-time ($t_{ON}$) to be inversely proportional to the input voltage ($V_{IN}$) and proportional to the SMPS output voltage ($V_{OUT}$). The switching frequency remains nearly constant over the variation of input voltage at the steady-state condition. Control modes are selected by the MODE pin described in Table 2.

## VREF, V0, V1, V2, V3 and Output Voltage

The device provides a 2.0-V, accurate voltage reference from the VREF pin. This output has a 300-µA current sourcing capability to drive V0, V1, V2 and V3 input voltages through a voltage divider circuit as shown in Figure 21. If higher overall system accuracy is required, the sum of total resistance (R1+R2+R3+R4+R5) from VREF to GND should be designed to be more than 67 kΩ. A MLCC capacitor with a value of 0.1-µF or larger should be attached close to the VREF pin.

The device also provides 2-bit VID flexible output voltage control. Up to four voltage levels can be programmed externally by a voltage divider circuit. V0 corresponds to VID 00, V1 coresponds to VID 01, V2 coresponds to VID 10 and V3 coresponds to VID 11. It is not necessary to match the voltage set point ($V_{SET1}$, $V_{SET2}$, $V_{SET3}$ or $V_{SET4}$) to any particular V0, V1, V2 or V3 input. Assignment of the input voltage is entirely dependent on the user requirement, which makes the device very easy and flexible to use.

The device can also be configured to provide 1-bit VID flexible output voltage operation. Up to two voltage levels can be programmed externally by a voltage divider circuit. Normally, if 1-bit VID operation is desired, the VID0 pin is generally used (the VID1 pin should be grounded if not used).

In the applications where fewer than four input voltage levels are needed, the remaining input voltage pins cannot be left floating. Connection from the unused pins to GND is required for proper operation.

**Table 1. VID Settings**

| | VID1 | VID0 | |
|---|---|---|---|
| V0 | 0 | 0 | $V_{SET1}$, $V_{SET2}$, $V_{SET3}$, $V_{SET4}$ |
| V1 | 0 | 1 | $V_{SET1}$, $V_{SET2}$, $V_{SET3}$, $V_{SET4}$ |
| V2 | 1 | 0 | $V_{SET1}$, $V_{SET2}$, $V_{SET3}$, $V_{SET4}$ |
| V3 | 1 | 1 | $V_{SET1}$, $V_{SET2}$, $V_{SET3}$, $V_{SET4}$ |

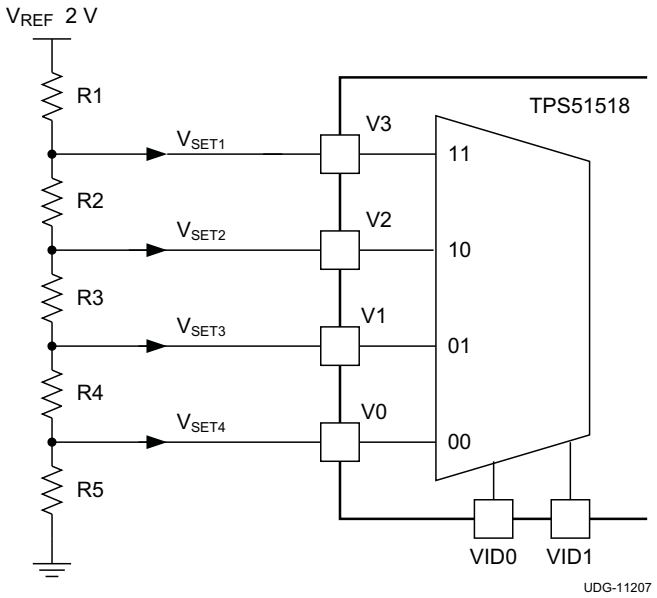



**Figure 21. Setting the Output Voltage**

## Soft-Start and Power Good

Prior to asserting EN high, the power stage conversion voltage and V5IN voltage should be ready. When EN is asserted high, TPS51518 provides soft start to suppress in-rush current during start-up. The soft start action is achieved by an internal SLEW current of 10 µA (typ) sourcing into a small external MLCC capacitor connected from SLEW pin to GND.

Use Equation 1 to determine the soft-start timing.

$$t_{SS} = C_{SLEW} \times \frac{V_{OUT}}{I_{SLEW}} \quad (1)$$

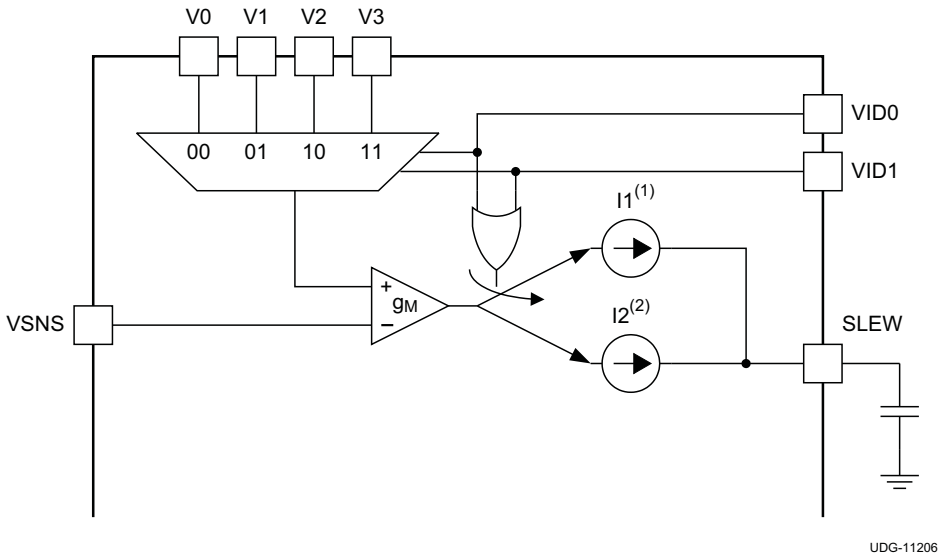
where

- $C_{SLEW}$ is the soft start capacitance
- $V_{OUT}$ is the output voltage
- $I_{SLEW}$ is the internal 10-µA current source

The TPS51518 has a powergood open-drain output that indicates the Vout voltage is within the target range. The target voltage window and transition delay times of the PGOOD comparator are ±8% (typ) and 1-ms delaly for assertion from low to high, and ±16% (typ) and 0.2-µs delay for de-assertion from high to low during operation.

## SLEW and VID Function

In addition to providing soft start function, SLEW is also used to program the VID transition time. TPS51518 supports 2-bit VID and 1-bit VID operations. VID0 and VID1 works with 1.05-V logic level signals with capability of supporting up to 3.3-V logic high.




(1) I1: Enable during VID transitioning, 50 µA.

(2) I2: Soft start, 10 µA.

**Figure 22. VID Configuration**

During VID transition:

- SLEW current is increased to 50 µA. Based on the VID transition time of the system, the amount of the SLEW capacitance can be calculated to meet such requirement. The minimum SLEW capacitance can be supported by the device is 2.7 nF.

$$C_{SLEW} = I_{SLEW\_VID} \times \frac{dt}{dV} \quad (2)$$

  where

  - $I_{SLEW}$ is 50 µA, dv is the voltage change during VID transition
  - dt is the required transition time

- FCCM (forced continuous conduction mode) operation is used regardless of the load level. In the meantime, the overcurrent level is temporality increased to 125% times the normal OCL level to prevent false OC trip during fast SLEW up transition. Power good, UVP and OVP functions are all blanked as well. All normal functions are resumed 16 internal clock cycles (64 µs) after VID transition is completed.
- Additional SLEW CLAMP is implemented. If severe output short occurs (either to GND or to some other high voltage rails in the system), SLEW is engaged into SLEW CLAMP, approximately 50 mV above or below the output voltage reference point. After 32 internal clockcycles, the CLAMP is engaged, UVP and OVP functions are activated to disable the controller at fault.

## MODE Pin Configuration

The TPS51518 reads the MODE pin voltage when the EN signal is raised high and stores the status in a register.Table 2 shows the MODE connection, corresponding control topology.

**Table 2. Mode States**

| MODE PIN CONNECTION | CONTROL TOPOLOGY | CURRENT SENSE | $f_{SW}$ (KHz) |
|---|---|---|---|
| GND | D-CAP | $R_{DS(on)}$ | 350 |
| 5-V Supply | D-CAP2 | | |

## D-CAP™ Mode

Figure 23 shows a simplified model of D-CAP™ mode architecture in the TPS51518.

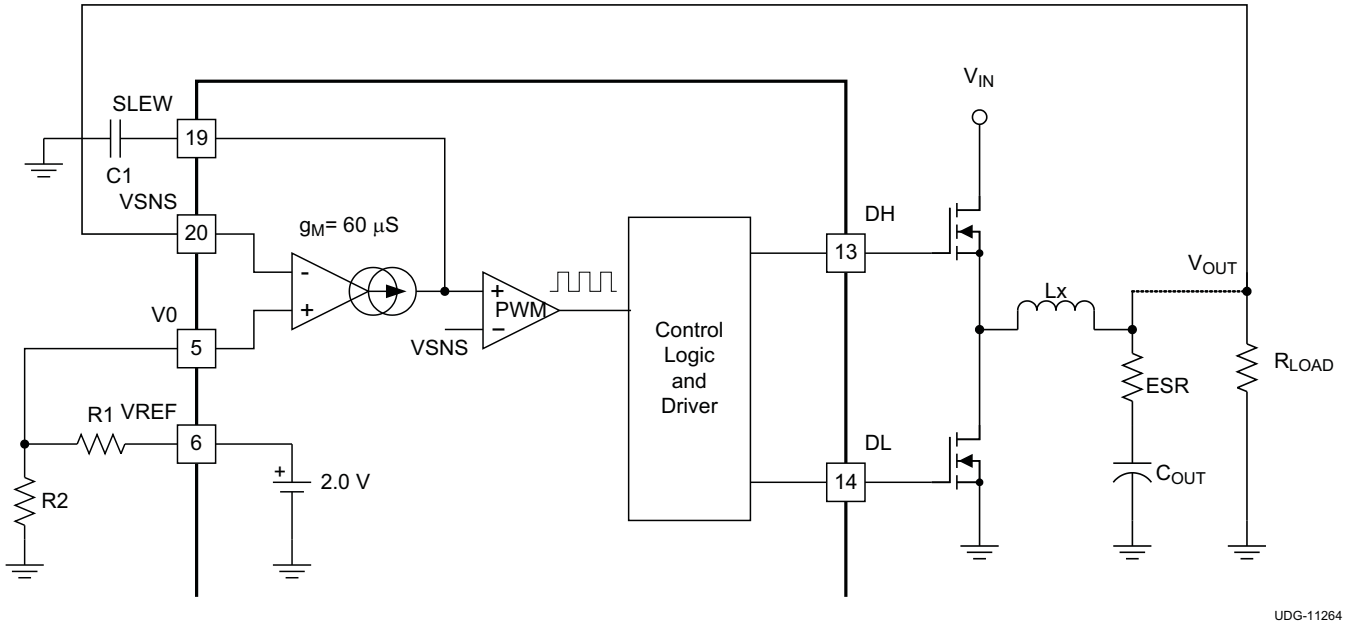



**Figure 23. D-CAP™ Mode Application**

The transconductance (gM) amplifier and SLEW capacitor (C1) forms an integrator. The ripple voltage generated by ESR of the output capacitor is inversed and averaged by the integrator. The small AC component is superimposed onto otherwise DC information and forms a reference input at the PWM comparator. As long as the integrator time constant is much larger than the inverse of the loop crossover frequency, the AC component is negligible. The VSNS voltage is directly compared to the SLEW voltage at the PWM comparator. The PWM comparator creates a set signal to turn on the high side MOSFET each cycle.

The PWM comparator creates a set signal to turn on the high-side MOSFET each cycle. The D-CAP™ mode offers flexibility on output inductance and capacitance selections with ease-of-use without complex feedback loop calculation and external components. However, it does require sufficient amount of ESR that represents inductor current information for stable operation and good jitter performance. Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

The requirement for loop stability is simple and is described in Equation 3. The 0-dB frequency, $f_0$, is recommended to be lower than 1/3 of the switching frequency to secure proper phase margin. The integrator time constant should be long enough compared to $f_0$, for example one decade low, as described in Equation 4.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{3}$$

where

- ESR is the effective series resistance of the output capacitor

- $C_{OUT}$ is the capacitance of the output capacitor
- $f_{SW}$ is the switching frequency (3)

$$\frac{g_M}{2\pi \times C1} \le \frac{f_0}{10}$$

where

- $g_M$ is transconductance of the error amplifier (typically 60 µS) (4)

Jitter is another attribute caused by signal-to-noise ratio of the feedback signal. One of the major factors that determine jitter performance in D-CAP™ mode is the down-slope angle of the VSNS ripple voltage. Figure 24 shows, in the same noise condition, that jitter is improved by making the slope angle larger.

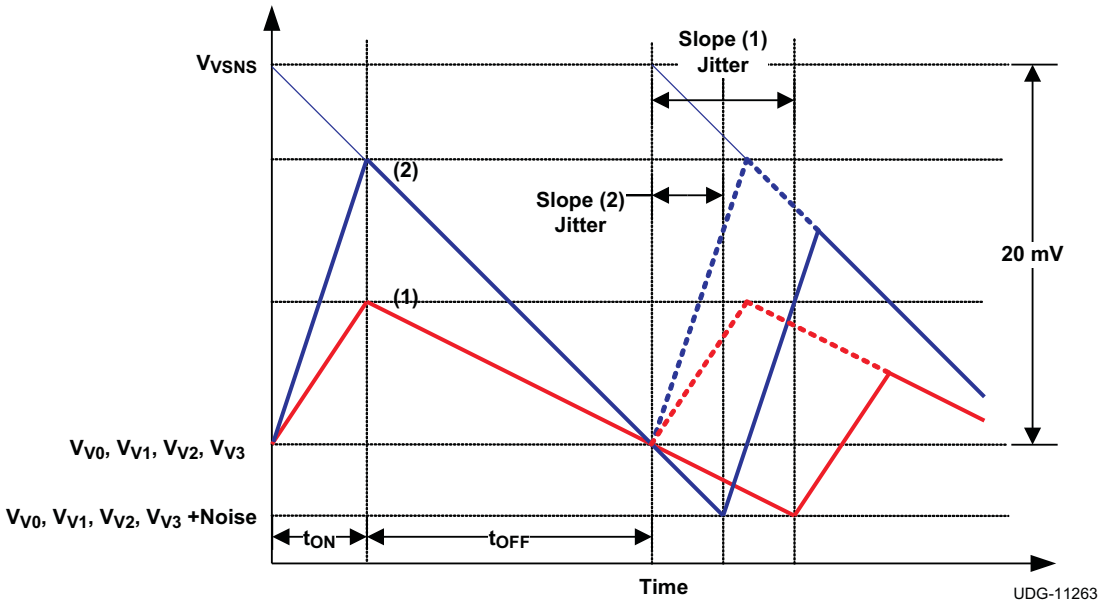



**Figure 24. Ripple Voltage Slope and Jitter Performance**

For a good jitter performance, use the recommended down slope of approximately 20 mV per switching period as shown in Figure 24 and Equation 5.

$$\frac{V_{OUT} \times ESR}{f_{SW} \times L_X} \ge 20\,mV$$

where

- $V_{OUT}$ is the SMPS output voltage
- $L_X$ is the inductance (5)

## D-CAP2™ Mode

Figure 25 shows a simplified model of D-CAP2™ mode architecture in the TPS51518.

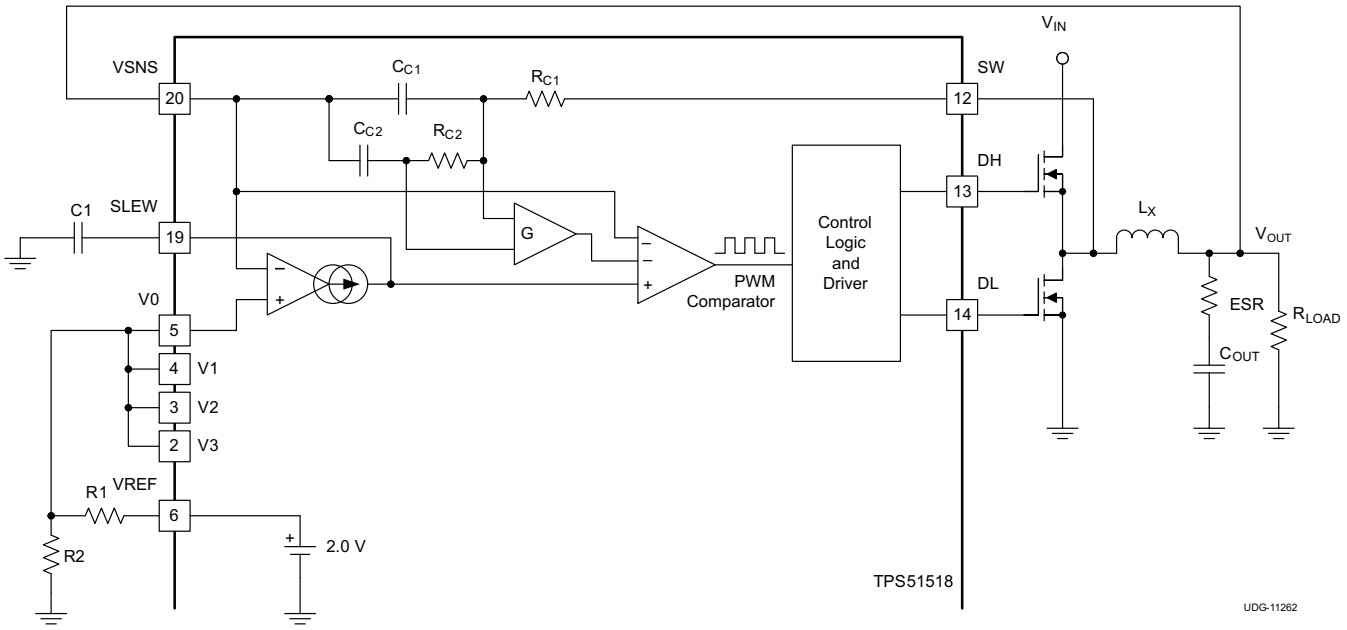



**Figure 25. Simplified D-CAP2 Mode Architecture**

When TPS51518 operates in D-CAP2 mode, it uses an internal phase compensation network ($R_{C1}$, $R_{C2}$, $C_{C1}$ and $C_{C2}$ and G) to work with very low ESR output capacitors such as multi-layer ceramic capacitors (MLCC). The role of such network is to sense and scale the ripple component of the inductor current information and then use it in conjunction with the voltage feedback to achieve loop stability of the converter.

The switching frequency used for D-CAP2 mode is 350 kHz and it is generally recommended to have a unity gain crossover (f0) of 1/4 or 1/3 of the switching frequency, which is approximately 90 kHz to 120 kHz for the purpose of this application.

Given the range of the recommended unity gain frequency, the power stage design is flexible, as long as Equation 6 is true.

$$\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}} \le \frac{1}{10}\times f_0 \tag{6}$$

When TPS51518 is configured in D-CAP2 mode, the overall loop response is dominated by the internal phase compensation network. The compensation network is designed to have two identical zeros at 5.2 kHz in the frequency domain, which serves the purpose of splitting the L-C double pole into one low frequency pole (same as the L-C double pole frequency) and one high-frequency pole (greater than the unity gain crossover frequency).

## Light-Load Operation

In auto-skip mode, the TPS51518 SMPS control logic automatically reduces its switching frequency to improve light-load efficiency. To achieve this intelligence, a zero cross detection comparator is used to prevent negative inductor current by turning off the low-side MOSFET. Equation 7 shows the boundary load condition of this skip mode and continuous conduction operation.

$$I_{LOAD(LL)} = \frac{(V_{IN} - V_{OUT})}{2\times L_X}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{f_{SW}} \tag{7}$$

## Out-of-Bound Operation

When the output voltage rises to 8% above the target value, the out-of-bound operation starts. During the out-of-bound condition, the controller operates in forced PWM-only mode. Turning on the low-side MOSFET beyond the zero inductor current quickly discharges the output capacitor. During this operation, the cycle-by-cycle negative overcurrent limit is also valid. Once the output voltage returns to within regulation range, the controller resumes to auto-skip mode.

## Current Sensing

In order to provide both cost effective solution and good accuracy, TPS51518 supports MOSFET $R_{DS(on)}$ sensing. For $R_{DS(on)}$ sensing scheme, TRIP pin should be connected to GND through the trip voltage setting resistor, $R_{TRIP}$. In this scheme, TRIP terminal sources 10μA of $I_{TRIP}$ current (at $T_A$ = 25°C) and the trip level is set to 1/8 of the voltage across the $R_{TRIP}$. The inductor current is monitored by the voltage between the GND pin and the SW pin so that the SW pin is connected to the drain terminal of the low-side MOSFET. $I_{TRIP}$ has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the sense resistor or the source terminal of the low-side MOSFET.

## Overcurrent Protection

TPS51518 has cycle-by-cycle overcurrent limiting protection. The inductor current is monitored during the off-state and the controller maintains the off-state when the inductor current is larger than the overcurrent trip level. The overcurrent trip level, $V_{OCTRIP}$, is determined by Equation 8.

$$V_{OCTRIP} = R_{TRIP} \times \left( \frac{I_{TRIP}}{8} \right) \tag{8}$$

Because the comparison is made during the off-state, $V_{OCTRIP}$ sets the valley level of the inductor current. The load current OCL level, $I_{OCL}$, can be calculated by considering the inductor ripple current.

Overcurrent limiting using $R_{DS(on)}$ sensing is shown in Equation 9.

$$I_{OCL} = \left( \frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{I_{IND(ripple)}}{2} = \left( \frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L_X} \times \frac{V_{OUT}}{f_{SW} \times V_{IN}} \tag{9}$$

where

- $I_{IND(ripple)}$ is inductor ripple current

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down.

## Overvoltage and Undervoltage Protection

The TPS51518 sets the overvoltage protection (OVP) when VSNS voltage reaches a level 20% (typ) higher than the target voltage. When an OV event is detected, the controller changes the output target voltage to 0 V. This usually turns off DRVH and forces DRVL to be on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, DRVL is turned off and DRVH is turned on, for a minimum on-time.

After the minimum on-time expires, DRVH is turned off and DRVL is turned on again. This action minimizes the output node undershoot due to LC resonance. When the VSNS reaches 0 V, the driver output is latched as DRVH off, DRVL on.

The undervoltage protection (UVP) latch is set when the VSNS voltage remains lower than 68% (typ) of the REFIN voltage for 1 ms or longer. In this fault condition, the controller latches DRVH low and DRVL low and discharges the $V_{OUT}$. UVP detection function is enabled after 1.2 ms of SMPS operation to ensure startup.

To release the OVP and UVP latches, toggle EN or adjust the V5IN voltage down and up beyond the undervoltage lockout threshold.

## V5IN Undervoltage Lockout Protection

TPS51518 has a 5-V supply undervoltage lockout protection (UVLO) threshold. When the V5IN voltage is lower than UVLO threshold voltage, typically 4.0 V, $V_{OUT}$ is shut off. This is a non-latch protection.

## Thermal Shutdown

TPS51518 includes an internal temperature monitor. If the temperature exceeds the threshold value, 140°C (typ), $V_{OUT}$ is shut off. The state of $V_{OUT}$ is open at thermal shutdown. This is a non-latch protection and the operation is restarted with soft-start sequence when the device temperature is reduced by 10°C (typ).

## Layout Considerations

Certain issues must be considered before designing a layout using the TPS51518.

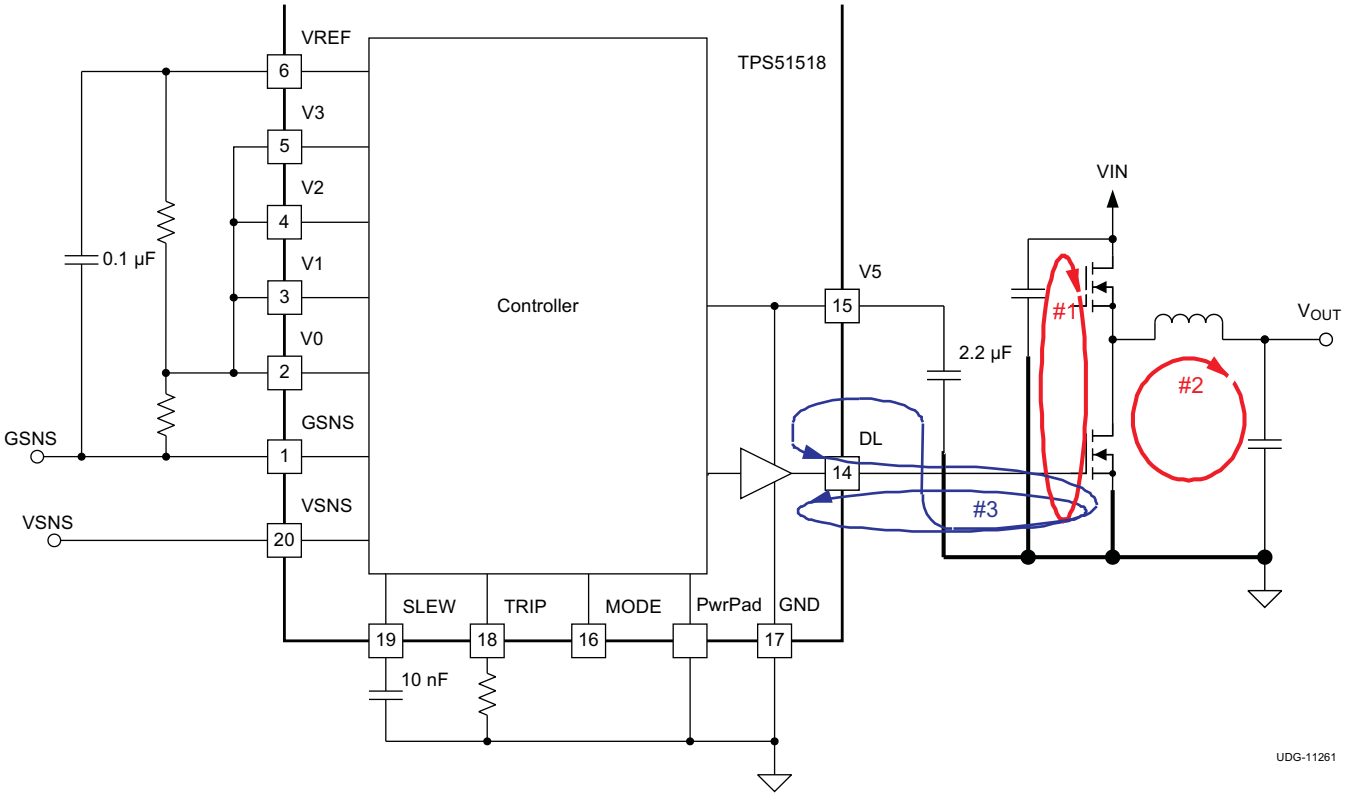



**Figure 26. DC/DC Converter Ground System**

- $V_{IN}$ capacitor(s), $V_{OUT}$ capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VSNS, SLEW, MODE, V0, V1, V2, V3, VREF and TRIP should be placed away from high-voltage switching nodes such as SW, DH, DL or BST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - Loop #1. The most important loop to minimize the area of is the path from the $V_{IN}$ capacitor(s) through the high and low-side MOSFETs, and back to the capacitor(s) through ground. Connect the negative node of the $V_{IN}$ capacitor(s) and the source of the low-side MOSFET at ground as close as possible. (Refer to loop #1 of Figure 26)
  - Loop #2. The second important loop is the path from the low-side MOSFET through inductor and $V_{OUT}$ capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of $V_{OUT}$ capacitor(s) at ground as close as possible. (Refer to loop #2 of Figure 26)
  - Loop #3. The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5 capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current

flows from gate of the low-side MOSFET through the gate driver and PGND, and back to source of the low-side MOSFET through ground. Connect negative node of V5 capacitor, source of the low-side MOSFET and PGND at ground as close as possible. (Refer to loop #3 of Figure 26)

- VSNS can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side. For additional noise filtering, insert a 10-Ω, 1-nF, R-C filter between the sense point and the VSNS pin. Connect GSNS to ground return point at the load device or the general ground plane/layer. VSNS and GSNS can be used for the purpose of remote sensing across the load device, however, care must be taken to minimize the routing trace to prevent excess noise injection to the sense lines.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as SW node, which connects to the source of the switching MOSFET, the drain of the rectifying MOSFET and the high-voltage side of the inductor, should be as short and wide as possible.
- In order to effectively remove heat from the package, prepare the thermal land and solder to the package thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps to dissipate heat. Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation.

## DESIGN EXAMPLES

This section describes three different applications for the TPS51518 controller. Design 1 is a 2-Bit VID $I_{CC(max)}$ = 25 A, D-CAP2™, 350-kHz application. Design 2 is a 2-Bit VID $I_{CC(max)}$ = 2 5A, D-CAP™, 350-kHz application. Design 3 is a 2-Bit VID $I_{CC(max)}$ D-CAP2™, 350-kHz for Intel Chief River System Agent application (SV processor).

### Design 1: 2-Bit VID $I_{CC(max)}$ = 25 A, D-CAP2™, 350-kHz Application

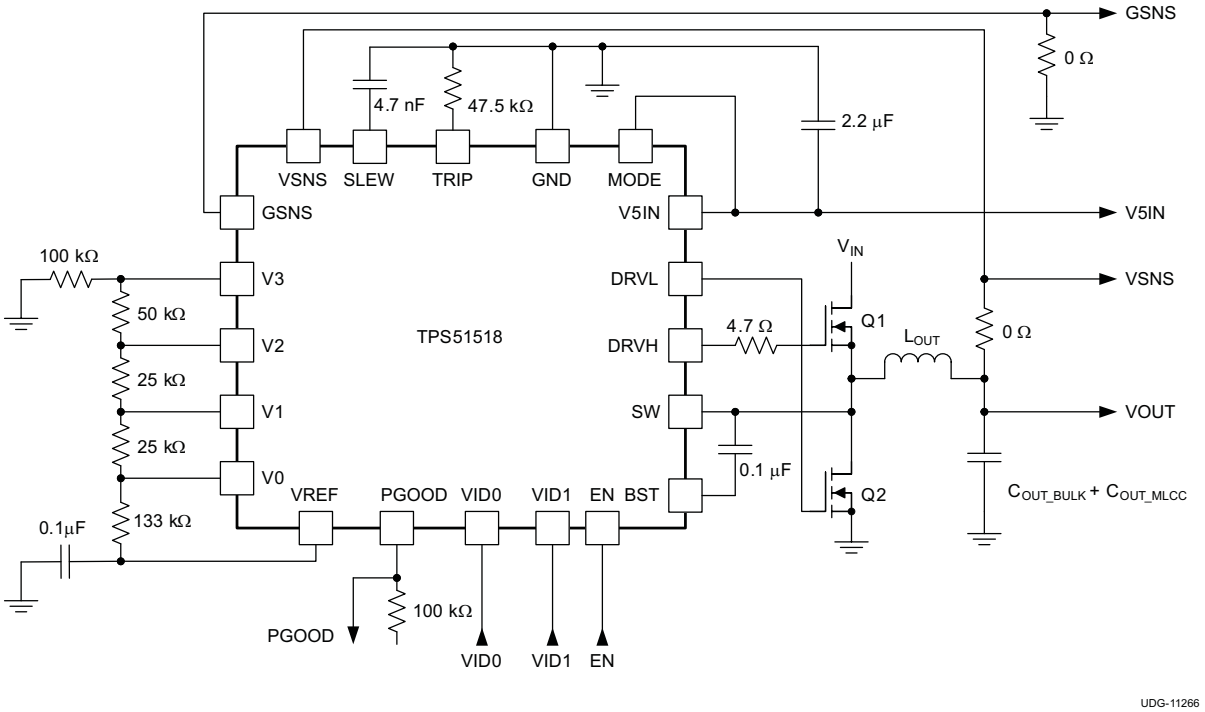



**Figure 27. Application Circuit for Design 1**

**Table 3. VID Table for Design 1**

| VID1 | VID0 | OUTPUT VOLTAGE (V) |
|---|---|---|
| 0 | 0 | 1.2 |
| 0 | 1 | 1.05 |
| 1 | 0 | 0.9 |
| 1 | 1 | 0.6 |

**Table 4. List of Materials for Design 1**

| REFERENCE DESIGNATOR | QTY | SPECIFICATION | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| $C_{IN}$ (not shown) | 4 | 10 µF, 25 V | Taiyo Yuden | TMK325BJ106MM |
| $C_{OUT\_BULK}$ | 3 | 330 µF, 2.5 V, 9 mΩ | Sanyo | 2TPE330M9 |
| $C_{OUT\_MLCC}$ | 10 | 22 µF, 6.3 V | Murata | GRM21BB30J226ME38 |
| $L_{OUT}$ | 1 | 0.45 µH, 17 A, 1.1 mΩ | Panasonic | ETQP4LR45XFC |
| Q1 | 1 | 30 V, 7.3 mΩ | Texas Instruments | CSD17302Q5A |
| Q2 | 2 | 30 V, 3.3 mΩ | Texas Instruments | CSD17306Q5A |

### Design 2: 2-Bit VID $I_{CC(max)}$ = 25 A, D-CAP™, 350-kHz, Application Circuit

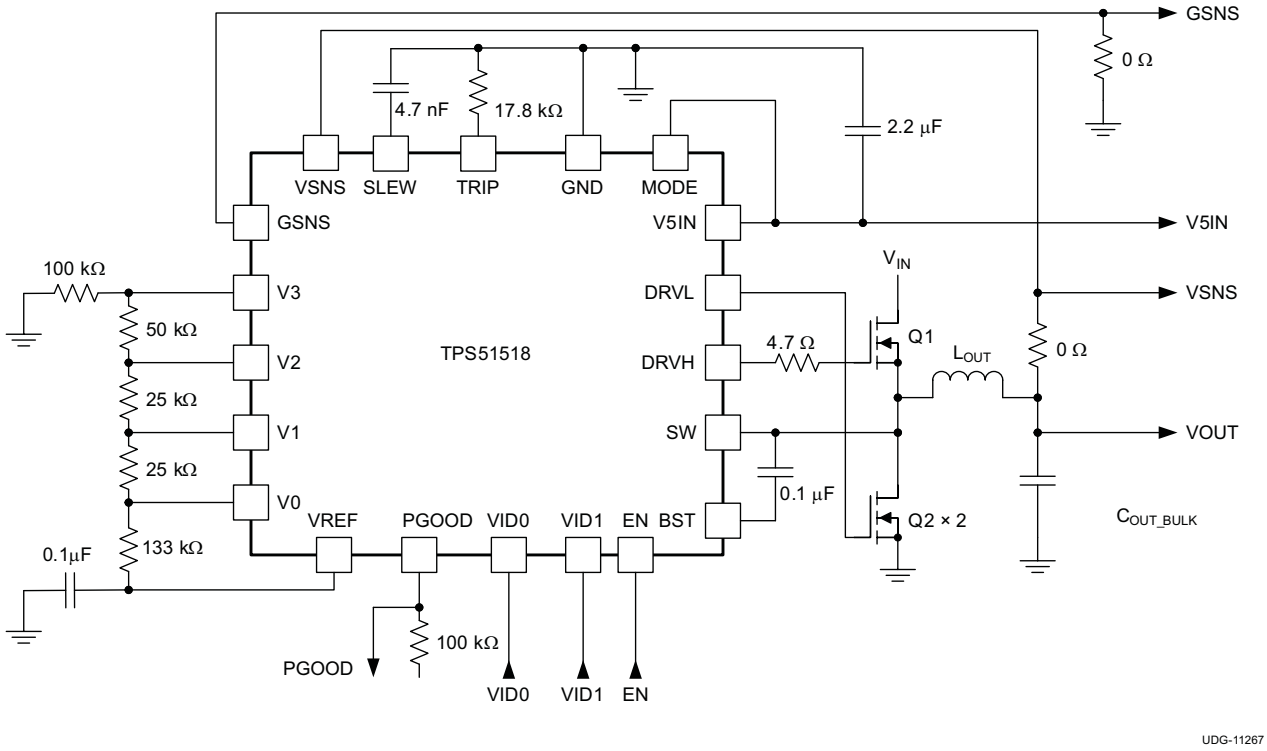



**Figure 28. Application Circuit for Design 2**

**Table 5. VID Table for Design 2**

| VID1 | VID0 | OUTPUT VOLTAGE (V) |
|---|---|---|
| 0 | 0 | 1.2 |
| 0 | 1 | 1.05 |
| 1 | 0 | 0.9 |
| 1 | 1 | 0.6 |

**Table 6. List of Materials for Design 2**

| REFERENCE DESIGNATOR | QTY | SPECIFICATION | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| $C_{IN}$ (not shown) | 4 | 10 µF, 25 V | Taiyo Yuden | TMK325BJ106MM |
| $C_{OUT\_BULK}$ | 3 | 330 µF, 2.5 V, 9 mΩ | Sanyo | 2TPE330M9 |
| $L_{OUT}$ | 1 | 0.45 µH, 17 A, 1.1 mΩ | Panasonic | ETQP4LR45XFC |
| Q1 | 1 | 30 V, 7.3 mΩ | Texas Instruments | CSD17302Q5A |
| Q2 | 2 | 30 V, 3.3 mΩ | Texas Instruments | CSD17306Q5A |

### Design 3: 2-Bit VID, $I_{CC(max)}$ = 6 A, D-CAP2™ 350-kHz for Intel Chief River System Agent Application (SV Processor)

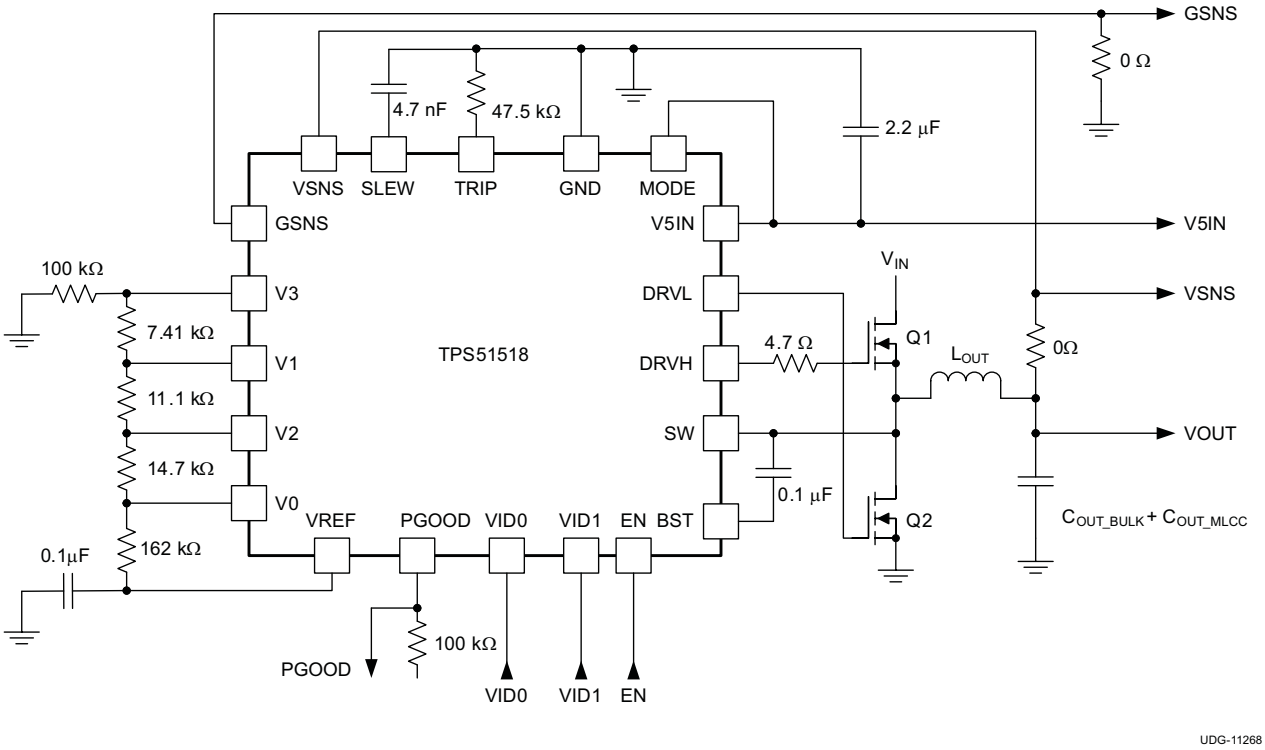



**Figure 29. Application Circuit for Design 3**

**Table 7. VID Table for Design 3**

| VID1 | VID0 | OUTPUT VOLTAGE (V) |
|---|---|---|
| 0 | 0 | 0.9 |
| 0 | 1 | 0.8 |
| 1 | 0 | 0.725 |
| 1 | 1 | 0.675 |

**Table 8. List of Materials for Design 3**

| REFERENCE DESIGNATOR | QTY | SPECIFICATION | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| $C_{IN}$ (not shown) | 2 | 10 µF, 25 V | Taiyo Yuden | TMK325BJ106MM |
| $C_{OUT\_BULK}$ | 1 | 220 µF, 2.5 V, 9 mΩ | Sanyo | 2TPE330M9 |
| $C_{OUT\_MLCC}$ | 1 | 22 µF, 6.3 V | Murata | GRM21BB30J226ME38 |
| $L_{OUT}$ | 1 | 1.5 µH, 10 A, 9.7 mΩ | Panasonic | ETQP4LR45XFC |
| Q1 | 1 | 30 V, 7.3 mΩ | Texas Instruments | CSD17302Q5A |
| Q2 | 1 | 30 V, 3.3 mΩ | Texas Instruments | CSD17306Q5A |

## DESIGN PROCEDURE

The simplified design procedure is done for a system agent rail for IMVP7 Intel platform application using the TPS51518 controller.

**Step One: Determine the specifications.**

The system agent rail requirements provide the following key parameters:

- $V_{00}$ = 0.90 V
- $V_{01}$ = 0.725 V
- $V_{10}$ = 0.80 V
- $V_{11}$ = 0.675 V
- $I_{CC(max)}$ = 6 A
- $I_{DYN(max)}$ = 2 A

**Step Two: Determine system parameters.**

The input voltage range and operating frequency are of primary interest.

In this example:

- 9 V ≤ $V_{IN}$ ≤ 20 V
- $f_{SW}$ = 350 kHz

**Step Three: Determine inductor value and choose Inductor.**

Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. In this example, use 25%:

$I_{P-P}$ = 6 A × 0.25 = 1.5 A

At $f_{SW}$ = 350 kHz with a 20-V input and a 0.80-V output:

$$L = \frac{V \times dT}{I_{P-P}} = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{V_{10}}{f_{SW} \times V_{IN}}\right)}{I_{P-P}} = \frac{(20\,V - 0.8\,V) \times \left(\frac{0.8\,V}{350\,kHz \times 20\,V}\right)}{1.5\,A} \quad (10)$$

For this application, a 1.5-µH, 9.7-mΩ inductor from TDK with part number SPM6530T-1R5M100 is used.

**Step Four: Set the output voltages.**

Set the output voltage levels. for V0, V1, V2 and V3 pins ).

- VID 00, V0 = $V_{SET1}$ = 0.9 V
- VID 10, V2 = $V_{SET2}$ = 0.8 V
- VID 01, V1 = $V_{SET3}$ = 0.725 V
- VID 11, V3 = $V_{SET4}$ = 0.675 V

Follow the TPS51518 Design Tool_1.0.xls (in the ***VID_Config*** section) to determine the resistor values:

- $V_{REF}$ = 2 V
- R1 = 162 kΩ
- R2 = 14.7 kΩ
- R3 = 11.1 kΩ
- R4 = 7.41 kΩ
- R5 = 100 kΩ

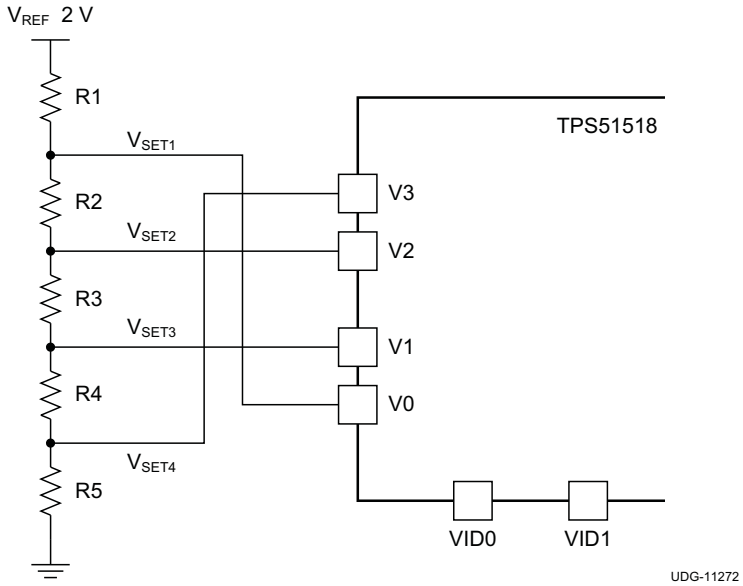



**Figure 30. Setting the Output Voltage**

### Step Five: Calculate SLEW capacitance.

SLEW can be used to program the soft-start time and voltage transition timing. During soft-start operation, the current source used to program the SLEW rate is 10 µA (nominal). During VID transition, the current source is switched to a higher current of 50 µA.

In this design example, the requirement is to complete VID_00 to VID_11 transition within 20 µs, calculate the SLEW capacitance based on Equation 11.

$$C_{SLEW} = I \times \frac{dt}{dV} = 50\ \mu A \times \frac{20\,\mu s}{0.9\,V - 0.675\,V} = 4.7\,nF \tag{11}$$

For $V_{OUT}$ = 0.9 V, the soft start timing based on $C_{SLEW}$ is 423 µs.

The slower slew rate is desired to minimize large inductor current perturbation during startup and voltage transition, thus reducing the possibility of acoustic noise.

### Step Six

TPS51518 uses a low-side on-resistance ($R_{DS(on)}$ ) sensing scheme. The TRIP pin sources 10 µA of current and the trip level is set to 1/8 of the voltage across the TRIP resistor ($R_{TRIP}$ ). The overcurrent trip level is determined by $R_{TRIP}$ × ($I_{TRIP}$ /8). Because the comparison is done during the off state, the trip voltage sets the valley current. The load current can be calculated by considering the inductor ripple current.

$$R_{TRIP} = \frac{8 \times \left( I_{OCL} - \left( \frac{(V_{IN} - V_{OUT})}{(2 \times Lx)} \right) \times \frac{(V_{OUT})}{(f_{SW} \times V_{IN})} \right) \times R_{DS(on)}}{I_{TRIP}} \tag{12}$$

where

- $V_{IN}$ is the input voltage
- $V_{OUT}$ is the output voltage
- $f_{SW}$ is the switching frequency (350 kHz)
- $R_{DS(on)}$ is the low-side FET on resistance
- $I_{TRIP}$ is the trip current, 10 µA (nominal)
- Lx is the output inductance

**Step Seven: Determine the output capacitance.**

***D-CAP™ Mode***

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine the ESR value to meet small signal stability and recommended ripple voltage. A quick reference is shown in Equation 13 and Equation 14.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{3}$$
$$\frac{g_M \times ESR}{2 \times \pi \times C1} \le \frac{f_0}{10} \quad (13)$$

where

- $g_M$ is the 60 µS
- C1 is the SLEW capacitance (14)

$$\frac{V_{OUT} \times ESR}{f_{SW} \times Lx} \ge 20\,mV \quad (15)$$

***D-CAP2™ Mode***

The switching frequency for D-CAP2™ mode is 350 kHz and it is generally recommend to have a unity gain crossover ($f_0$) of 1/4 or 1/3 of the switching frequency, which is approximately 90 kHz to 120kHz for the purpose of this application.

$$f_0 = \frac{f_{SW}}{3} = 90\,kHz \quad or \quad f_0 = \frac{f_{SW}}{4} = 120\,kHz \quad (16)$$

Given the range of the recommended unity gain frequency, the power stage design is flexible, as long as the LC double pole frequency is less than 10% of $f_0$.

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \le \frac{1}{10} \times f_0 = 9\,kHz \Leftrightarrow 12\,kHz \quad (17)$$

As long as the LC double pole frequency is designed to be less than 1/10 of $f_0$, the internal compensation network provides sufficient phase boost at the unity gain crossover frequency in order for the converter to be stable with enough margin (> 60°).

When the ESR frequency of the output bulk capacitor is in the vicinity of the unity gain crossover frequency of the loop, additional phase boost is achieved. This applies to POSCAP and/or SPCAP output capacitors.

When the ESR frequency of the output capacitor is beyond the unity gain crossover frequency of the loop, no additional phase boost is achieved. This applies to low/ultra low ESR output capacitors, such as MLCCs.

Equation 18 and Equation 19 can be used to estimate the amount of capacitance needed for a given dynamic load step/release. Note that there are other factors that may impact the amount of output capacitance for a specific design, such as ripple and stability. Equation 18 and Equation 19 are used only to estimate the transient requirement, the result should be used in conjuction with other factors of the design to determine the necessary output capacitance for the application.

$$C_{OUT(min\_under)} = \frac{L \times \left(\Delta I_{LOAD(max)}\right)^2 \times \left(\frac{V_{OUT} \times t_{SW}}{V_{IN(min)}} + t_{MIN(off)}\right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)}}\right) \times t_{SW} - t_{MIN(off)}\right) \times V_{OUT}} \quad (18)$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)}\right)^2}{2 \times \Delta V_{LOAD(release)} \times V_{OUT}} \quad (19)$$

Equation 18 and Equation 19 calculate the minimum $C_{OUT}$ for meeting the transient requirement, which is 72.9 µF assuming ±3% voltage allowance for load step and release.

**Step Eight: Select decoupling and peripheral components.**

For the TPS51518, peripheral capacitors use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

- V5IN decoupling ≥2.2 µF, ≥ 10 V
- VREF decoupling 0.22 µF to 1 µF, ≥ 4 V
- Bootstrap capacitors ≥ 0.1 µF, ≥ 10 V
- Pull-up resistors on PGOOD, 100 kΩ

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS51518RUKR | ACTIVE | WQFN | RUK | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -10 to 105 | 51518 | Samples |
| TPS51518RUKT | ACTIVE | WQFN | RUK | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -10 to 105 | 51518 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

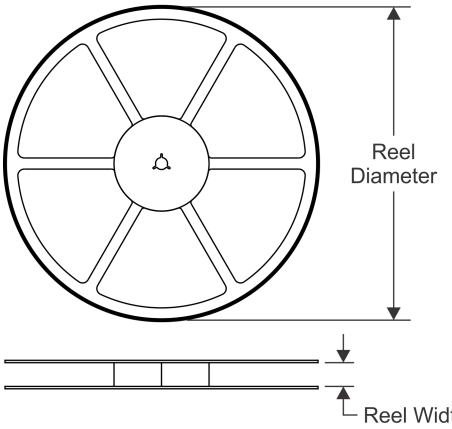
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

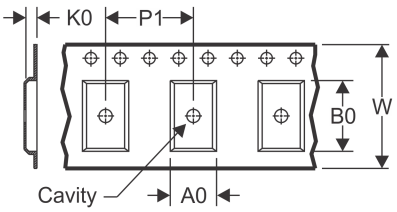
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

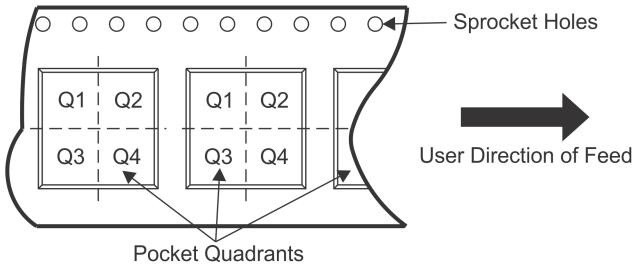



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

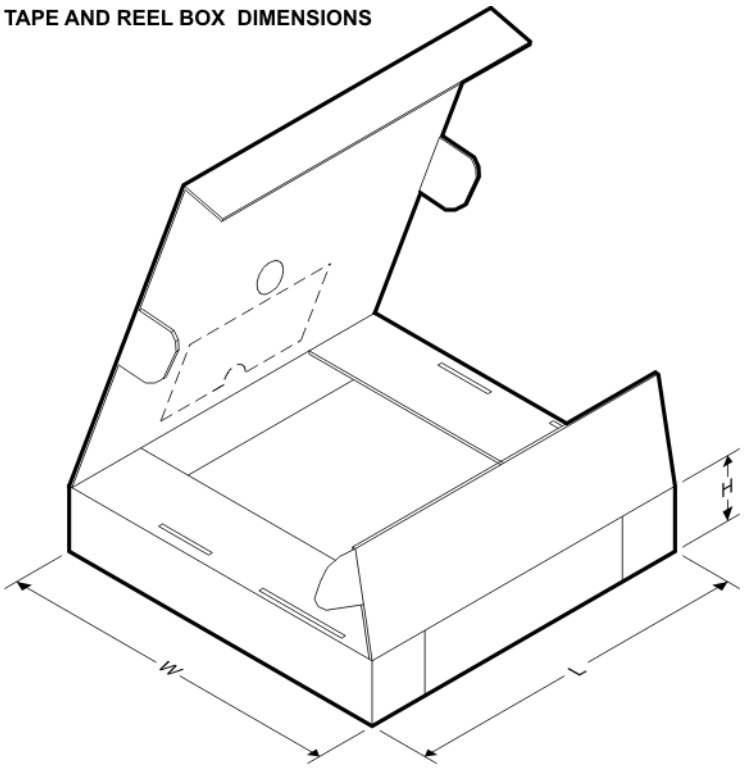
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS51518RUKR | WQFN | RUK | 20 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS51518RUKT | WQFN | RUK | 20 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

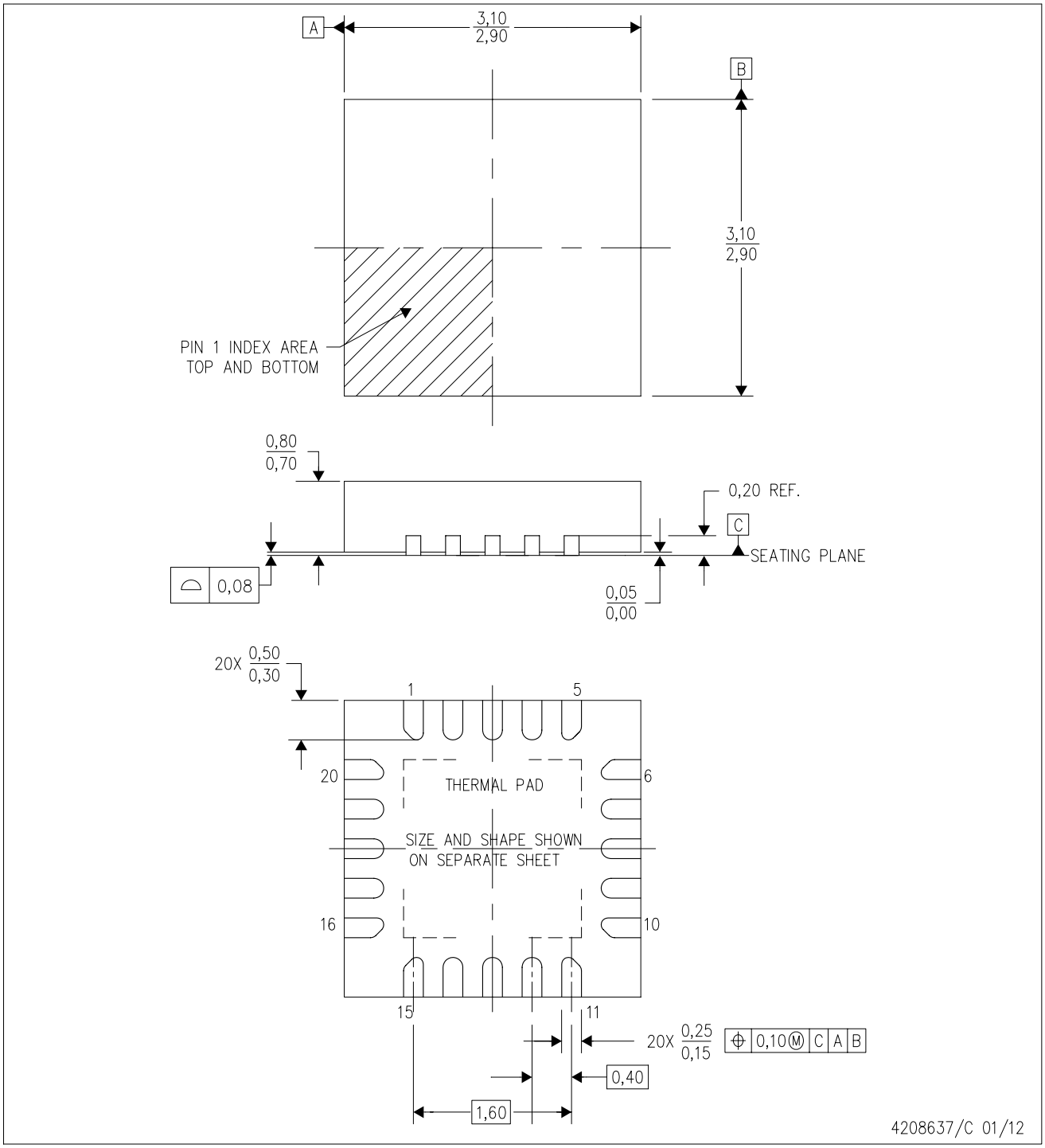
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS51518RUKR | WQFN | RUK | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS51518RUKT | WQFN | RUK | 20 | 250 | 210.0 | 185.0 | 35.0 |

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

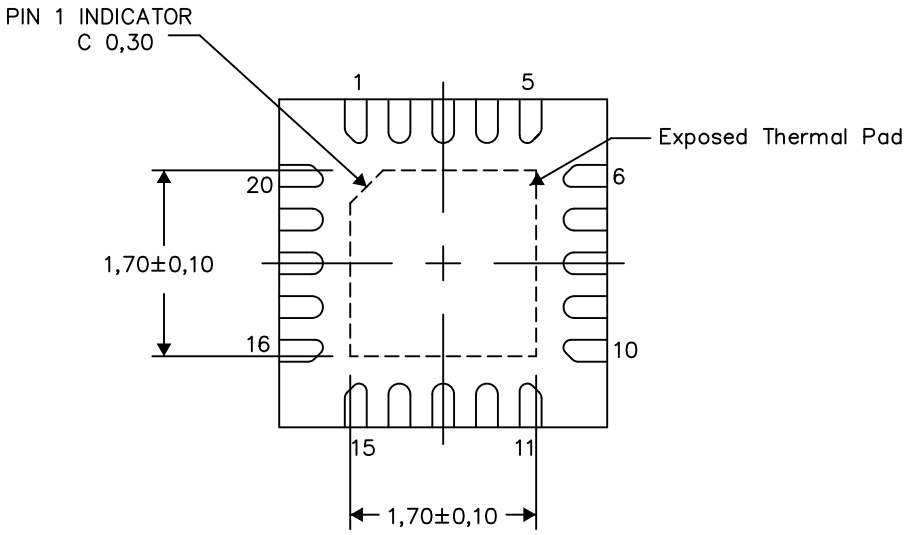
RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



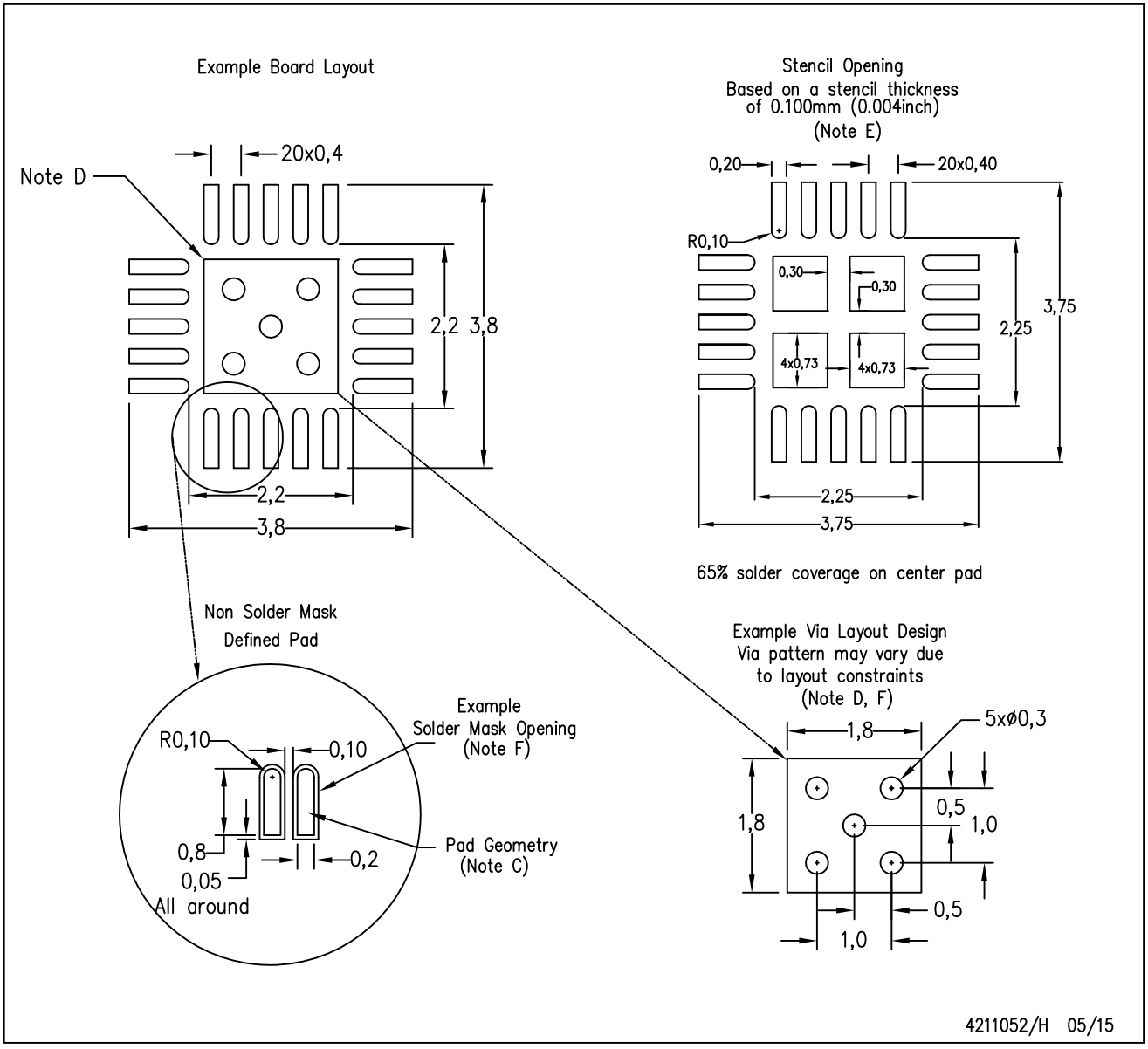

Bottom View

Exposed Thermal Pad Dimensions

4209762/I 05/15

NOTE: All linear dimensions are in millimeters

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265