DUAL-PHASE, ECO-MODE™ STEP-DOWN POWER MANAGEMENT IC FOR 50-A+ APPLICATIONS

FEATURES

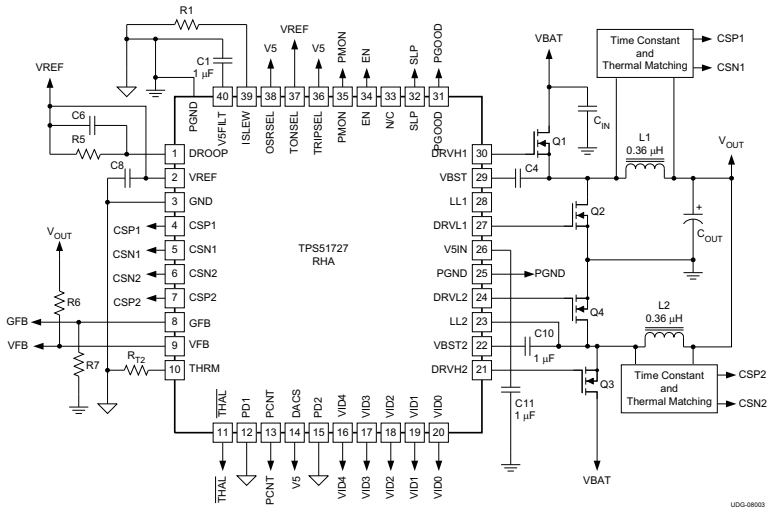
- **Seamless Phase Add/Drop Enables Maximum Efficiency Under Any Load Condition**
- **Minimum External Parts Count**
- **±8 mV VOUT Accuracy Over Line/Load/Temp.**
- **5-Bit DAC with 0.4-V to 1.25-V Output Range Supports Wide Range of Applications**
- **Optimized Efficiency at Light & Heavy Loads**
- **Patent Pending Output Overshoot Reduction (OSR™)**
- **Accurate, Adjustable Voltage Positioning**
- **Selectable 200/300/400/500 kHz Frequency**
- **Pat. pending AutoBalance™ Phase Balancing**
- **Supports Resistor or Inductor DCR Current Sensing**
- **Accurate, Selectable Current Limit**
- **4.5-V to 28-V Conversion Voltage Range**
- **Fast MOSFET Driver w/Integrated Boost Diode**
- **Integrated OVP Can Be Disabled Thermal Sensor and Output Power Monitor**
- **Small 6 × 6, 40-Pin QFN PowerPAD™ Package**

APPLICATIONS

- **High-Current, Low-Voltage Applications for Adapter, Battery, NVDC or 5-V/12-V Rails**

DESCRIPTION

The TPS51727 is a complete, step down controller with integrated gate drivers. The PCNT pin enables operation in dual or single-phase mode to optimize efficiency depending on the load requirements. The advanced D-CAP+™ architecture provides fast transient response with minimum output capacitance. The DAC supports VID-on-the-fly transitions to optimize the output voltage to the operating state of the system to meet idle power requirements. The auto-skip feature of the TPS51727 optimizes light-load efficiency in both single and dual phase operation. System management features include an adjustable thermal sensor, output power monitoring and sleep state controls. Adjustable control of VOUT slew rate and voltage positioning are provided. In addition, the TPS51727 includes two high-current MOSFET gate drivers to drive high and low side N-channel MOSFETs with exceptionally high speed and low switching loss The PCNT and VID0 through VID4, pins have flexible LV I/O thresholds that enable interface with logic voltages from 1.0 V to 3.6 V. The TPS51727 is packaged in a space saving, thermally enhanced, RoHS compliant 40-pin QFN and is rated to operate from –10°C to 100°C.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
–10°C to 100°C	Plastic Quad Flat Pack (QFN)	TPS51727RHAT	40	Tape-and-reel	250	Green (RoHS and no Sb/Br)
		TPS51727RHAR			2500	

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND.) (1)

PARAMETER			VALUE	UNIT
Input voltage range(2)		VBST1, VBST2	–0.3 to 36	V
		VBST1, VBST2 to LL1 or LL2	–0.3 to 6	
		CSP1, CSN1, CSP2, CSN2, THRM, VID0, VID1, VID2, VID3, VID4, PD1, PD2, DACS, VFB, SLP, OSRSEL, GFB V5IN, V5FILT, PCNT, TRIPSEL TONSEL, ISLEW, EN	–0.3 to 6	
Output voltage range(2)		LL1, LL2	–5.0 to 30	V
		DRVH1, DRVH2	–5.0 to 36	
		DRVH1, DRVH2 to LL1 or LL2	–0.3 to 6	
		VREF, DROOP, DRVL1, DRVL2, PMON, PGOOD	–0.3 to 6	
		PGND, GFB	–0.3 to 0.3	
T_J	Operating junction temperature		+150	°C
T_{stg}	Storage junction temperature		–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 100°C POWER RATING
40-pin RHA	3.125 W	31.25 mW /°C	0.781 W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Supply voltages	Conversion voltage (no pin assigned)	3.0		28.0	V
	V5IN, V5FILT	4.50		5.25	
Voltage range, conversion pins	VBST1, VBST2	-0.1		34	
	DRVH1, DRVH2	-0.8		34	
	LL1, LL2	-0.8		28	
Voltage range, 5-V pins	VFB, CSP1, CSN1, CSP2, CSN2, PMON, DROOP, ISLEW, DRVL1, DRVL2, THRM, PGOOD, DACS, VREF, TRIPSEL, TONSEL, OSRSEL	-0.1		5VIN	
Voltage range, 3.3-V pins	SLP, EN, PCNT, VID0, VID1, VID2, VID3, VID4, PD1, PD2, $\overline{\text{THAL}}$	-0.1		3.6	
Voltage range, ground pins	PGND, GND, GFB	-0.1		0.1	
T_J, Operating junction temperature		-10		100	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	MIN	TYP	MAX	UNIT
Human body model	2000			V
CDM	1500			V

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V5IN = V5FILT = 5.0 V GFB = PGND = GND, VFB = V_{OUT} (Unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: CURRENTS, UVLO AND POWER-ON RESET						
I_{V5}	V5IN + V5FILT supply current	$V_{DAC} < V_{FB} < V_{DAC}$ + 100 mV, EN = HI		2.5	4.0	mA
I_{V5STBY}	V5IN + V5FILT standby current	EN = LO			1	µA
V_{UVLOH}	V5FILT UVLO OK threshold	V5FILT = V5IN, VFB < 200 mV, Ramp up; EN = HI; Switching begins	4.25	4.40	4.50	V
V_{UVLOL}	V5FILT UVLO fault threshold	V5FILT = V5IN. Ramp down; EN = HI, VFB = 100 mV, Restart if 5 V dips below V_{POR} then rises > V_{UVLOH} or V_{EN} is toggled with 5 V > V_{UVLOH}	4.05	4.15	4.30	V
V_{POR}	V5FILT fault latch reset threshold	V5FILT=V5IN, Ramp Down, EN = HI, Can restart if 5V goes up to V_{UVLOH} and no other faults present	1.60	1.89	2.25	V
REFERENCES: DAC, VREF, VBOOT AND DRVL DISCHARGE						
V_{VIDSTP}	VID Step Size	Change VID0 HI to LO to HI		25		mV
V_{DAC1}	VFB No Load Active	0.750 V ≤ VFB ≤ 1.250 V, +15°C ≤ T_J ≤ 105°C	–0.55%		0.55%	
V_{DAC2}	VFB No Load Active/Sleep	0.500 V ≤ VFB ≤ 0.750 V	–8		8	mV
V_{DAC3}	VFB Deeper Sleep	0.300V ≤ VFB ≤ 0.500 V	–12		12	mV
V_{VREF}	VREF Output	V5FILT = 4.5 V to 5.5 V, IREF = 0	1.675	1.710	1.745	V
$V_{VREFSRC}$	VREF Output Source	IREF = 0 µA to 250 µA	–9	–3		mV
$V_{VREFSNK}$	VREF Output Sink	IREF = –250 µA to 0 µA		10	35	mV
V_{DLDQ}	DRVL Discharge Threshold	VFB < 200 mV, DRVL goes high for 1ms	200	250	325	mV
VOLTAGE SENSE: VFB AND GFB						
I_{VFB}	VFB Input Bias Current	Not in Fault, Disable or UVLO; VFB = 2 V, GFB = 0 V		9	20	µA
I_{VFBDQ}	VFB Input Bias Current, Discharge	Fault, Disable or UVLO, VFB = 100 mV	90	125	175	µA
I_{GFB}	GFB Input Bias Current	Not in Fault, Disable or UVLO; VFB = 2 V, GFB = 0 V	–20	–8		µA
V_{DELGND}	GFB Differential			±300		mV
$A_{GAINGND}$	GFB/GND Gain		0.993	1.000	1.007	V/V
V_{VFBCOM}	VFB Common Mode Input		–0.3		2.0	V
CURRENT SENSE: OVERCURRENT, ZERO CROSSING, VOLTAGE POSITIONING AND PHASE BALANCING						
V_{OCPP}	OCP Voltage Set (Valley Current Limit)	TRIPSEL = GND	7.3	11.0	15.5	mV
		TRIPSEL = REF	10.7	14.3	19.2	
		TRIPSEL = 3.3 V	14.3	18.2	22.9	
		TRIPSEL = V5FILT	19.7	23.8	28.4	
V_{OCPN}	Negative OCP Voltage (Minimum Magnitude)	TRIPSEL = GND	10.3	14.9	19.0	mV
		TRIPSEL = REF	15.4	20.0	24.5	
		TRIPSEL = 3.3 V	20.4	25.0	29.8	
		TRIPSEL = V5FILT	27.3	31.7	37.0	
V_{OCPCC}	Channel-to-Channel OCP matching	(V_{CSP1}–V_{CSN1}) – (V_{CSP2}–V_{CSN2}) at OCP for each channel		±1.0		mV
I_{CS}	CS Pin Input Bias Current	CSPx and CSNx	–1.00	0.02	1.00	µA
V_{ZXOFF}	Zero Crossing Comp. Internal Offset	CSPx – CSNx, SLP = High (Skip Mode)	–4.0	–0.8	4.0	mV
$G_{M\text{-}DROOP}$	Droop Amplifier Transconductance	VFB = 1 V	485	500	515	µS
I_{DROOP}	Droop Amplifier Sink/Source Current		50	100	150	µA
I_{BAL_TOL}	Internal Current Share Tolerance	V_{DAC} = 0.750 V; $V_{CSP1} – V_{CSN1} = V_{CSP2} – V_{CSN2} = V_{OCP\_MIN}$	–3%		3%	
A_{CSINT}	Internal Current Sense Gain	Gain from CSPx – CSNx to PWM comparator	5.85	5.95	6.05	V/V

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V5IN = V5FILT = 5.0 V GFB = PGND = GND, VFB = V_{OUT} (Unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER MONITOR						
V_{PWRLK}	Leakage Level Power Output	V_{DAC} = 0.5 V, ΣΔCS = 5 mV		125	280	mV
V_{PWRLO}	Low Level Power Output	V_{DAC} = 1 V, ΣΔCS = 10 mV	180	500	750	mV
V_{PWRMID}	Mid Level Power Output	V_{DAC} = 1.2 V, ΣΔCS = 20 mV	0.75	1.10	1.41	V
V_{PWRHI}	High Level Power Output	V_{DAC} = 1.2875 V, ΣΔCS = 40 mV	1.92	2.25	2.56	V
K_{PWR}	Gain Factor			47.6		V/V
I_{PWRSRC}	Power Monitor Source	V_{PWR} – 30 mV	800	900	1100	µA
I_{PWRSNK}	Power Monitor Sink	V_{PWR} + 30 mV	130	200	350	µA
DRIVERS: HIGH SIDE, LOW SIDE, CROSS CONDUCTION PREVENTION AND BOOST RECTIFIER						
R_{DRVH}	DRVH On Resistance	VBSTx – LLx = 5 V, HI State, VBST – VDRVH = 0.25 V		1.2	2.5	Ω
		VBSTx – LLx = 5V, LO State, VDRVH – VLL = 0.25 V		0.8	2.5	
I_{DRVH}	DRVH Sink/Source Current(1)	DRVHx =2.5 V, VBSTx – LLx = 5 V, Src		2.2		A
		DRVHx =2.5 V, VBSTx – LLx = 5 V, Snk		2.2		
T_{DRVH}	DRVH Transition Time	DRVHx 10% to 90% or 90% to 10%, C_{DRVHx} = 3 nF		21	40	ns
				15	40	
R_{DRVL}	DRVL On Resistance	HI State, V5IN – VDRVL = 0.25 V		0.9	2	Ω
		LO State, VDRVL – PGND = 0.25 V		0.4	1	
I_{DRVL}	DRVL Sink/Source Current(1)	DRVLx = 2.5 V, Source		2.7		A
		DRVLx = 2.5 V, Sink		8		
T_{DRVL}	DRVL Transition Time	DRVLx 90% to 10%, CDRVLx = 3 nF		10	35	ns
		DRVLx 10% to 90%, CDRVLx = 3 nF		20	35	
$T_{NONOVLP}$	Driver Non Overlap Time	LLx falls to 1V to DRVLx rises to 1 V	10	23	35	ns
		DRVLx falls to 1V to DRVHx rises to 1 V	15	30	43	
V_{FBST}	BST Rectifier Forward Voltage	V5IN – VBST, IF = 5 mA, T_A = 25°C	0.6	0.7	0.8	V
I_{BSTLK}	BST Rectifier Leakage Current	V_{VBST} = 34 V, V_{LL} = 28 V		0.1	1	µA
OVERSHOOT REDUCTION (OSR) THRESHOLD SETTING						
V_{OSR}	OSR Voltage Set	OSRSEL = GND	75	110	140	mV
		OSRSEL = REF	105	145	180	
		OSRSEL = 3.3 V	145	190	235	
		OSRSEL = V5FILT		OFF		
V_{OSRHYS}	OSR Voltage Hysteresis(1)	All settings		20		mV

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V5IN = V5FILT = 5.0 V GFB = PGND = GND, VFB = V_{OUT} (Unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMERS: SLEW RATE, ISLEW, ON-TIME AND I/O TIMING						
$I_{SLEW\ 1}$	R_{SLEW} to GND Current	R_{SLEW} = 125 kΩ from ISLEW to GND	9.90	10.00	10.15	µA
$I_{SLEW\ 2}$	R_{SLEW} to VREF Current	R_{SLEW} = 45 kΩ from VREF to ISLEW	9.5	10.2	10.8	µA
SL_{STRT}	VFB VID Change Slew Rate	I_{SLEW} = |10 µA|, EN goes 'HI' (soft-start), VID Slew, Non-OVP Fault = Soft-stop	9	13	16	mV/µs
$T_{PGDDGLTO}$	PGOOD Deglitch Time	Time from V_{VFB} out of +200 mV V_{DAC} boundary to PGOOD low	40	74	100	µs
$T_{PGDDGLTU}$	PGOOD Deglitch Time	Time from V_{VFB} out of –300 mV V_{DAC} boundary to PGOOD low	50	105	150	µs
T_{TON}	On-Time Control	V_{TON} = GND, V_{LLx} = 12 V, V_{VFB} = 1 V	285	370	460	ns
		V_{TON} = REF, V_{LLx} = 12 V, V_{VFB} = 1 V	200	250	300	
		V_{TON} = 3.3V, V_{LLx} = 12 V, V_{VFB} = 1 V	160	195	230	
		V_{TON} = V5FILT, V_{LLx} = 12 V, VFB = 1	140	170	200	
T_{MIN}	Controller Minimum OFF time	Fixed Value	95	129	155	ns
$T_{VIDDBNC}$	VID Debounce Time (2)		100			ns
$T_{PCNTBNC}$	PCNT Debounce Time(2)		100			ns
T_{VCCVID}	VID Change to VFB Change(2)				1500	ns
T_{ENPGD}	EN Low to PGOOD Low		20	74	100	ns
T_{PGDVCC}	PGOOD Low to VFB Change(2)				100	ns
$T_{THALDGLT}$	$\overline{THAL}$ Deglitch Time		0.7	1.1	3.0	ms
R_{SFTSTP}	Soft-stop Transitor Resistance		600	850	1100	Ω
PROTECTION: OVP, UVP, PGOOD, $\overline{THAL}$, "FAULTS OFF" AND INTERNAL THRMAL SHUTDOWN						
V_{OVPH}	Fixed OVP Voltage	V_{VFB} > V_{OVPH} for 1 µs, DRVL turns ON	1.65	1.70	1.75	V
V_{PGDH}	PGOOD High Threshold	Measured at the VFB pin wrt / VID code. Device latches OFF, begins soft-stop	180	220	255	mV
V_{PGDL}	PGOOD Low Threshold	Measured at the VFB pin wrt / VID code. IC latches off, begins soft-stop	–365	–325	–285	mV
V_{THRM}	Thermal Alarm Voltage	Measured at THRM; $\overline{THAL}$ goes LO	0.72	0.75	0.82	V
I_{THRM}	THRM Current	Measure I_{THRM} to GND	57	61	67	µA
V_{NOFLT}	All Faults OFF	V_{THRM} > (V_{V5FILT} + V_{TH}); not latched	4.75	4.90	5.00	V
TH_{INT}	Internal Controller Thermal Shutdown(2)	Not final tested. Latch off controller, attempt soft-stop		160		°C
TH_{HYS}	Thermal Shutdown Hysteresis(2)	Not final tested. Controller starts again after temperature has dropped		10		°C
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{THALL}	$\overline{THAL}$ Pull Down Voltage	Pull down voltage with 20-mA sink current		0.15	0.4	V
I_{THALLK}	$\overline{THAL}$ Leakage Current	Hi-Z Leakage Current, Apply 5-V in off state	–2.0	0.2	2.0	µA
V_{PGL}	PGOOD Pull Down Voltage	Pull down voltage with 3-mA sink current		0.1	0.4	V
I_{PGLK}	PGOOD Leakage Current	Hi-Z Leakage Current, Apply 5 V in off state	–2.0	0.1	2.0	µA
V_{LV_H}	LV I/O Logic High	PCNT, VID0, VID1, VID2, VID3, VID4		0.6	0.7	V
V_{LV_L}	LV I/O Logic Low	PCNT, VID0, VID1, VID2, VID3, VID4	0.3	0.4		V
I_{LV_LK}	LV I/O Leakage	Leakage current, V_{VID} = V_{PCNT} = 1.0 V, V_{SLP} = 3.3 V, V_{EN} = 0 V	–1.0	0.01	1.0	µA
I_{VIDLK}	LV I/O Leakage	Leakage current, V_{VID} = V_{PCNT} = 1.0 V, V_{EN} = 3.3 V	5	10	15	µA
V_{V3P3H}	I/O 3.3 V Logic High	EN, SLP		1.3	2.3	V
V_{V3P3L}	I/O 3.3 V Logic Low	EN, SLP	0.8	1.1		V
I_{ENH}	I/O 3.3 V Leakage	Leakage current, V_{EN} = 3.3 V	10.0		25.0	µA
I_{SLPH}	I/O 3.3 V Leakage	Leakage current, V_{EN} = 3.3 V; V_{SLP} = 3.3 V	20.0		45.0	µA
I_{VIDL}		V_{VID0} = V_{VID1} = V_{VID2} = V_{VID3} = V_{VID4} = 0 V, V_{EN} = 3.3 V	–3	–1.5	1	µA
I_{DACS}		V_{DACS} = 5 V, V_{EN} = 3.3 V	25		75	µA
I_{SELECT}		$V_{TRIPSEL}$ = V_{OSRSEL} = V_{TONSEL} = 5 V	–2	1.5	5	µA

(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

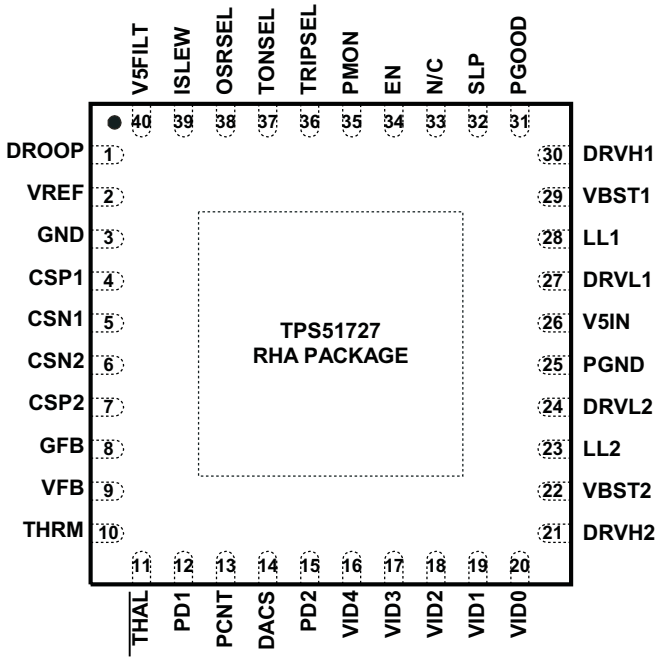
over recommended free-air temperature range, V5IN = V5FILT = 5.0 V GFB = PGND = GND, VFB = V_{OUT} (Unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CTRL}	V_{PCNT} = V_{SLP} = 0 V; V_{EN} = 3.3 V	–1		1	µA

DEVICE INFORMATION

TERMINAL CONFIGURATION

RHA Package Terminal Configuration
(Top View)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CSN1	5	I	Negative current sense inputs. Connect to the most negative node of current sense resistor or inductor DCR sense RC network.
CSN2	6		
CSP1	4	I	Positive current sense inputs. Connect to the most positive node of current sense resistor or inductor DCR sense RC network.
CSP2	7		
DACS	14	I	DAC range selection input. Tie to V5FILT.
DROOP	1	O	Output of GM error amplifier. A resistor to VREF sets the droop gain. A capacitor to VREF helps shape the transient response.
DRVH1	30	O	Top N-channel MOSFET gate drive outputs
DRVH2	21		
DRVL1	27	O	Synchronous N-channel MOSFET gate drive outputs.
DRVL2	24		
EN	34	I	Enable signal. 3.3V I/O level; 100ns de-bounce. Regulator enters controlled “soft-stop” when brought low.
GFB	8	I	Voltage sense return. Tie to GND with a 100-Ω resistor to close feedback when voltage sensing through a socket.
GND	3	-	Analog / signal ground. Tie to quiet ground plane.
ISLEW	39	I	Precision slew rate control setting. All voltage transitions, including start-up and shutdown, occur at the rated defined by the ISLEW resistor. Tie the ISLEW resistor to GND to enable OVP or VREF to disable OVP.
LL1	28	I/O	Top N-channel MOSFET gate drive return. Also, input for adaptive gate drive timing.
LL2	23		
N/C	33	-	Do not connect anything to this pin

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
OSRSEL	38	I	Overshoot reduction (OSR) setting. The OSR threshold can be selected or OSR can be disabled.
PAD	-	-	Thermal pad; Connect directly to system GND plane with multiple vias.
PCNT	13	I	Phase control input. 0.5-V threshold logic. High is dual phase mode.
PD1	12	I	Test pin. Tie to GND.
PD2	15		
PGOOD	31	O	Open-drain PWRGD output.
PGND	25	-	Synchronous N-channel MOSFET gate drive return.
PMON	35	O	Power monitor output. $V_{PMON} = V_{OUT} \times \Sigma V_{ISENSE} \times K$. See applications section for more detail.
SLP	32	I	Sleep mode control. 3.3-V I/O Level; disallows switching when entering sleep mode.
$\overline{\text{THAL}}$	11	O	Thermal alarm; open drain output, Active low. 1-ms de-glitch filter.
THRM	10	I/O	Thermal sensor input. An internal 60-µA current source flows into an NTC thermistor connected to GND. The voltage threshold is 0.75-V. Also is a 'Faults off' input, ($V_{THRM} = V_{V5FILT}$) for debug mode.
TONSEL	37	I	On-time selection pin. The operating frequency can be set between 200-kHz and 500-kHz in 100-kHz steps. Frequency can be changed during operation.
TRIPSEL	36	I	Overcurrent protection (OCP) setting. The valley current limit at the CS inputs can be selected in a range between approximately 10-mV to 20-mV.
V5IN	26	I	5-V power input for drivers; bypass to PGND with ≥ 1µF ceramic capacitor.
V5FILT	40	I	5-V power input for control circuitry. Has internal, 3-Ω resistor to 5VFILT. Bypass to GND with ≥ 1-µF ceramic capacitor.
VBST1	22	I	Top N-channel MOSFET bootstrap voltage inputs.
VBST2	29		
VFB	9	I	Voltage sense line tied directly to VOUT. Tie to VOUT with a 100-Ω resistor to close feedback when voltage sensing through a socket.
VID0	20	I	DAC programming bits most significant bit (MSB) to least significant bit (LSB). 0.5-V threshold logic.
VID1	19		
VID2	18		
VID3	17		
VID4	16		
VREF	2	O	1.7-V, 250-µA voltage reference. Bypass to GND with a 0.22-µF ceramic capacitor.

FUNCTIONAL BLOCK DIAGRAM

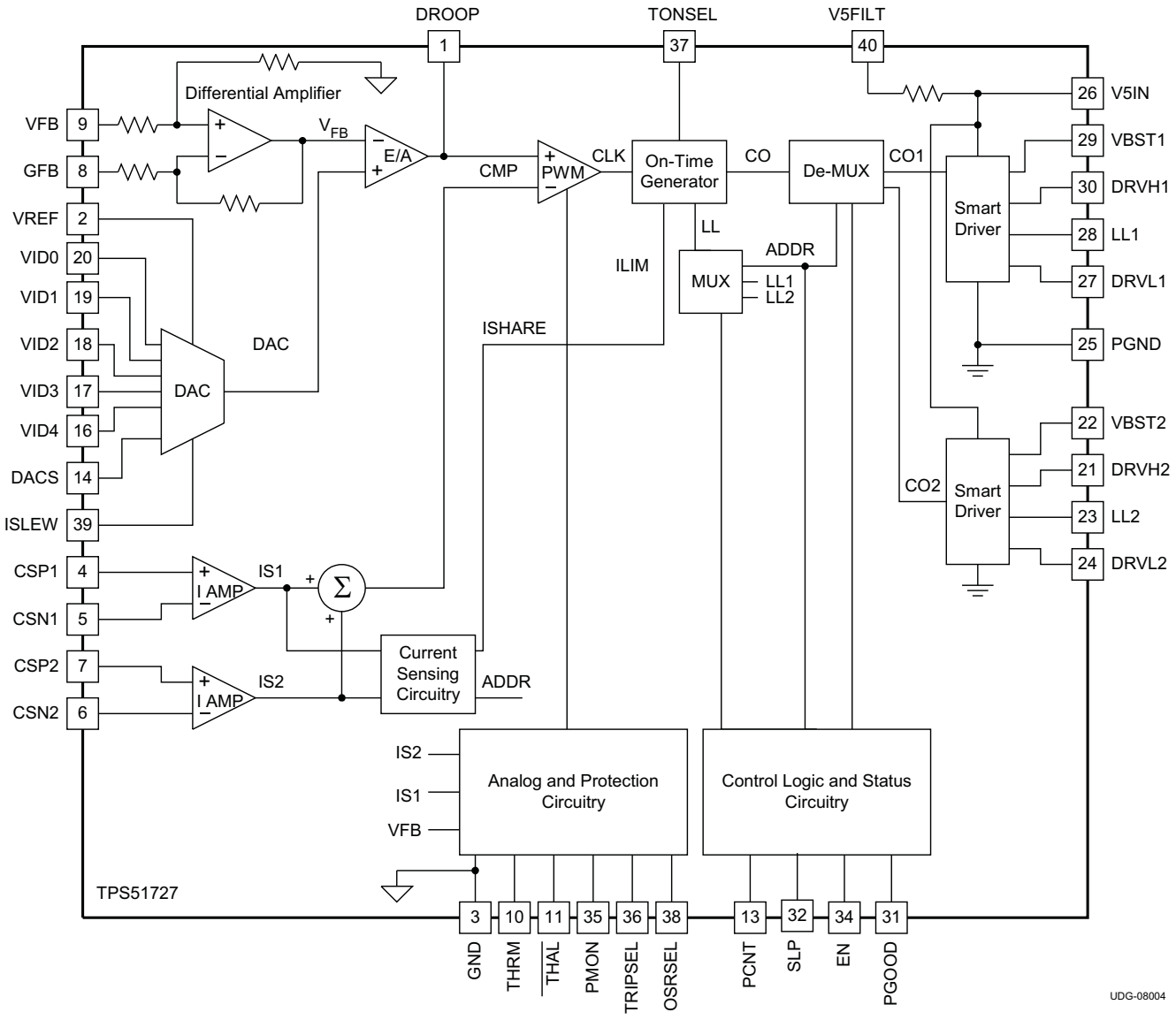


Figure 1. TPS51727 Functional Block Diagram

APPLICATION DIAGRAMS

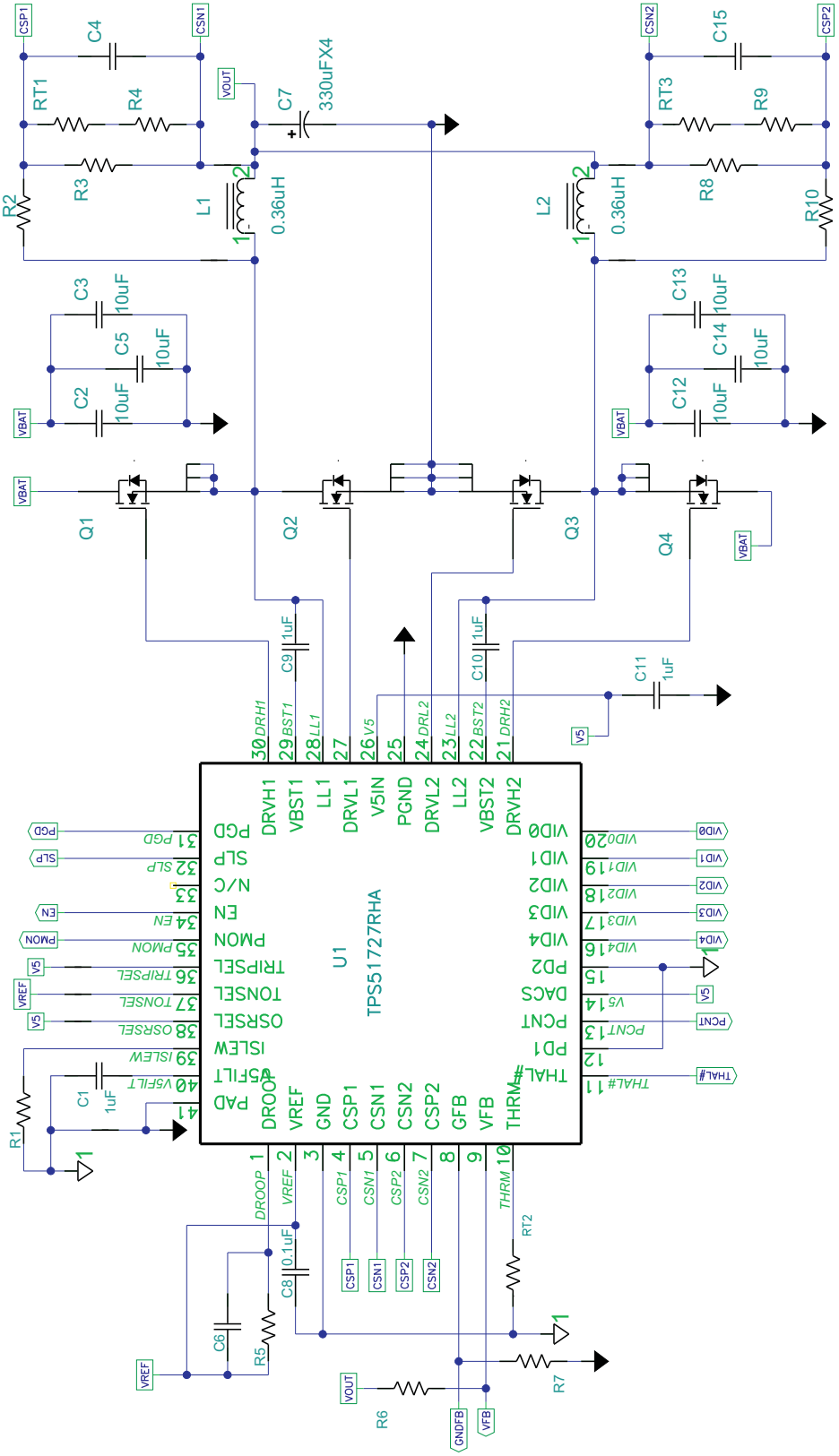


Figure 2. Inductor DCR Sense Application Diagram

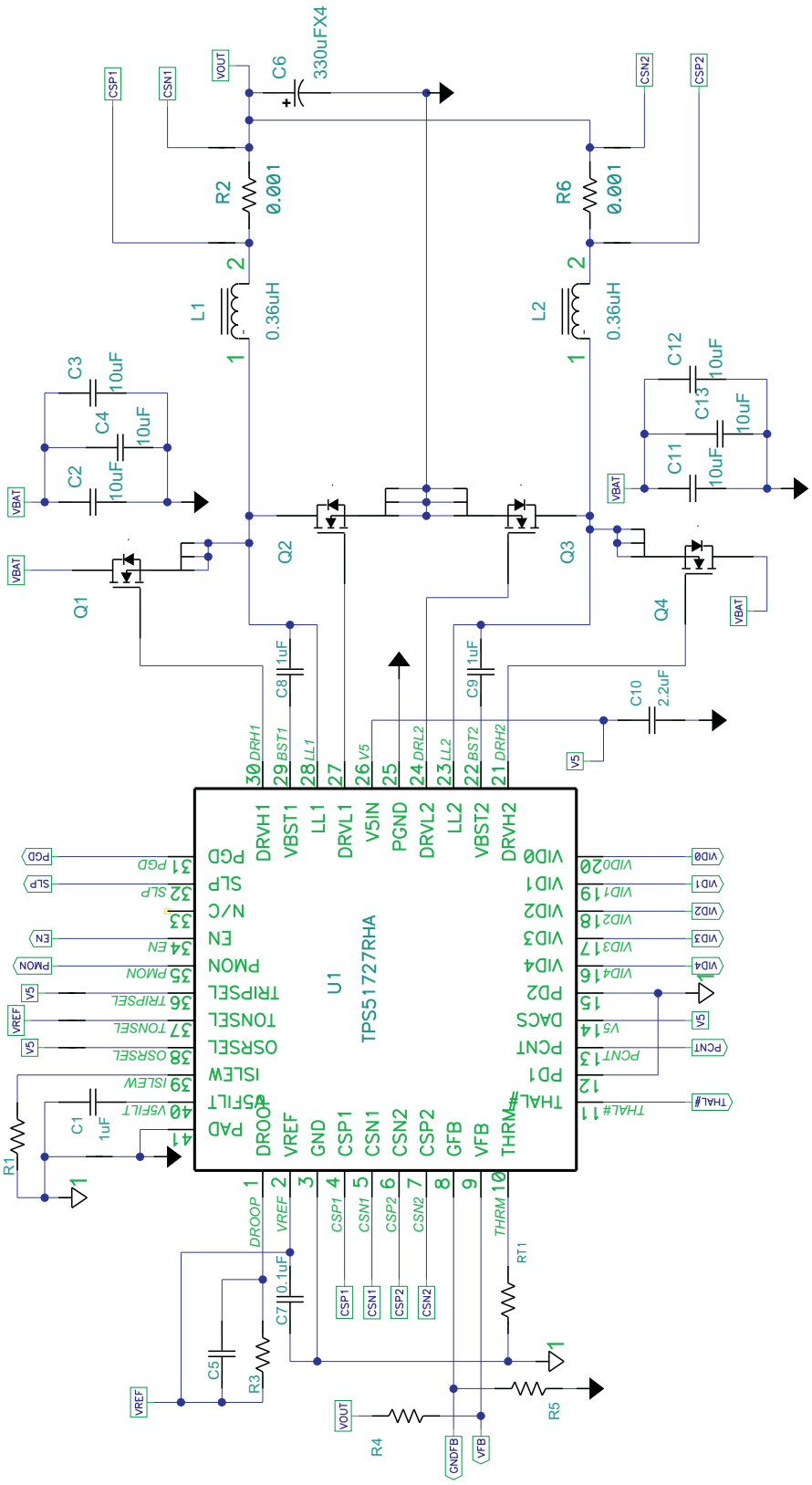


Figure 3. Resistor Sense Application Diagram

APPLICATION CIRCUIT LIST OF MATERIALS

Recommended parts for key external components for the circuits in Figure 2 and Figure 3 are in Table 1. These components have passed applications tests.

Table 1. Key External Component Recommendations

FUNCTION	MANUFACTURER	COMPONENT NUMBER
High-side MOSFET	Infineon	BSC080N03MSG
Low-side MOSFET (x2)	Infineon	BSC030N03MSG
Inductors	Panasonic	ETQP4LR36WFC
	Tokin	MPCG1040LR36
	Toko	FDUE10140D-R36M
Bulk Output Capacitors	Panasonic	EEFSX0D331XE
	NEC Proadlizer	PFAF250E127MNS
Ceramic Output Capacitors	Panasonic	ECJ2FB0J106K
	Murata	GRM21BR60J106KE19L
Sense Resistor (Figure 3 only)	Panasonic	ERJM1WTJ1M0U
NTC Thermistors	Panasonic	ERTJ1VV154J
	Murata	NCP18XF151J03RB

TYPICAL CHARACTERISTICS

TURBO MODE OUTPUT VOLTAGE
vs
OUTPUT CURRENT

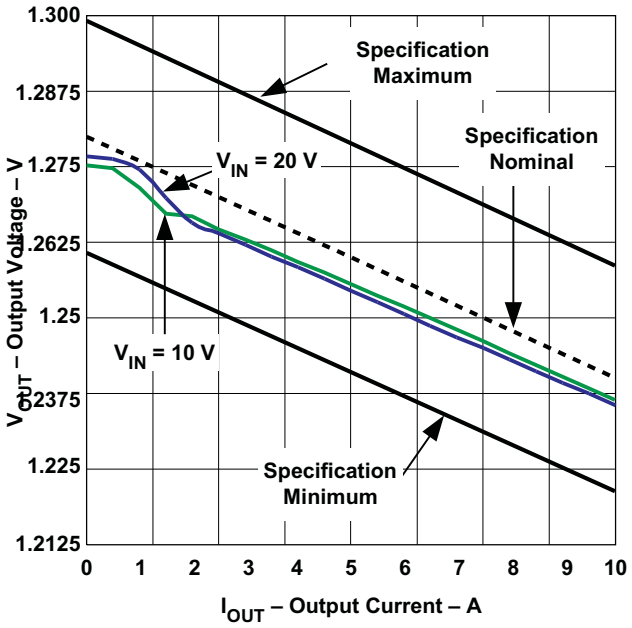


Figure 4.

NORMAL MODE OUTPUT VOLTAGE
vs
OUTPUT CURRENT

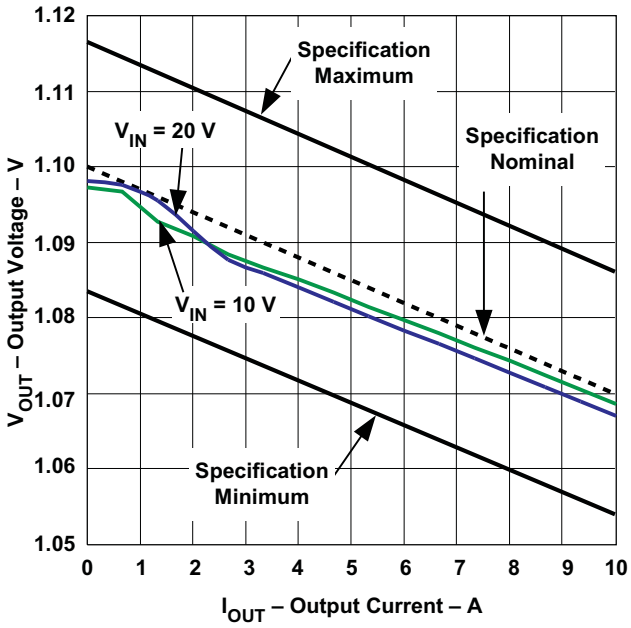


Figure 5.

SLEEP MODE OUTPUT VOLTAGE
vs
OUTPUT CURRENT

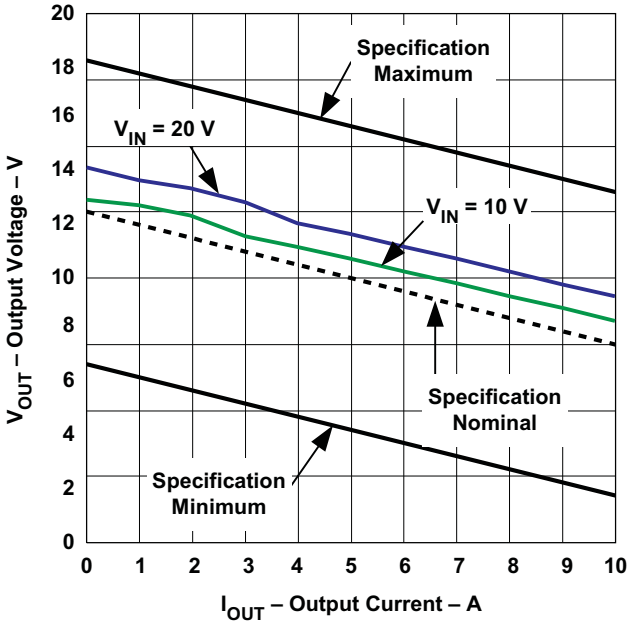


Figure 6.

TURBO MODE EFFICIENCY
vs
OUTPUT CURRENT

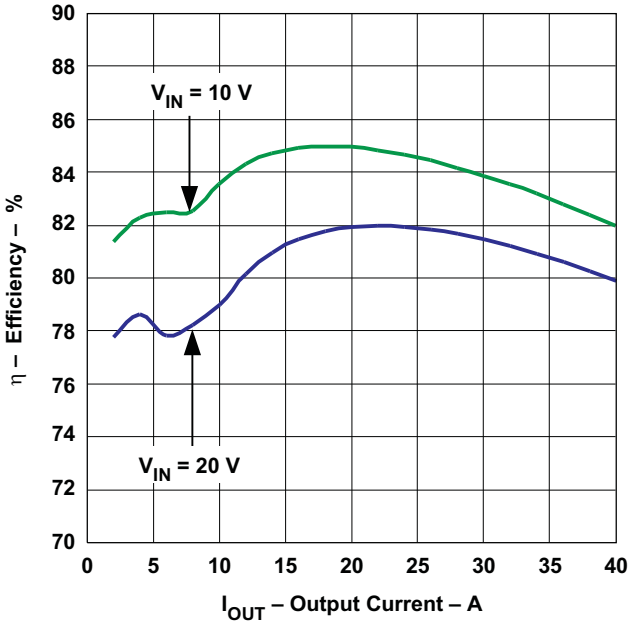


Figure 7.

TYPICAL CHARACTERISTICS (continued)

NORMAL MODE EFFICIENCY
vs
OUTPUT CURRENT

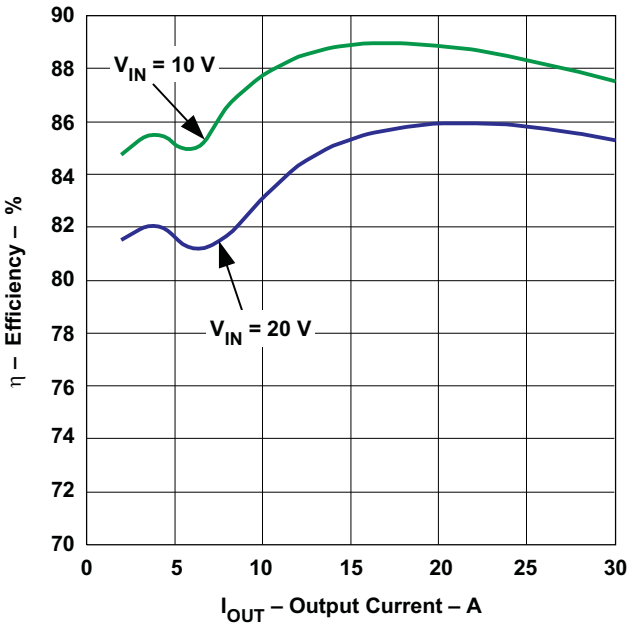


Figure 8.

SLEEP MODE EFFICIENCY
vs
OUTPUT CURRENT

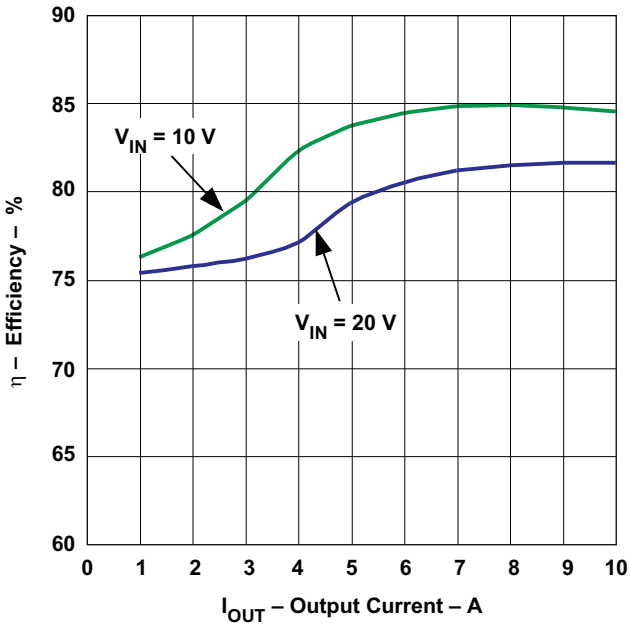


Figure 9.

CURRENT SHARE IMBALANCE
vs
OUTPUT CURRENT

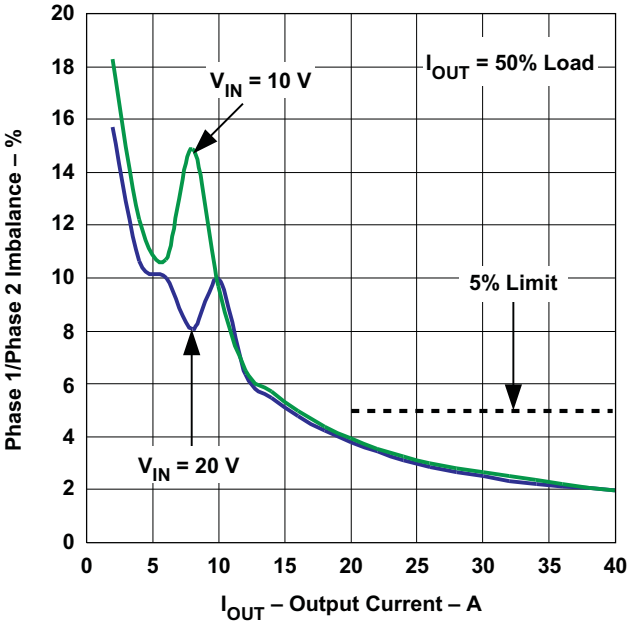


Figure 10.

POWER MONITOR VOLTAGE
vs
OUTPUT CURRENT

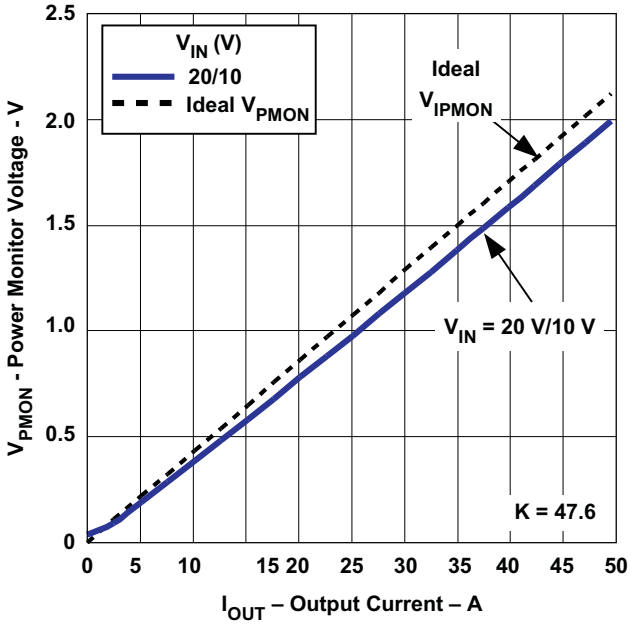


Figure 11.

TYPICAL CHARACTERISTICS (continued)

VOLTAGE REFERENCE
vs
OUTPUT CURRENT

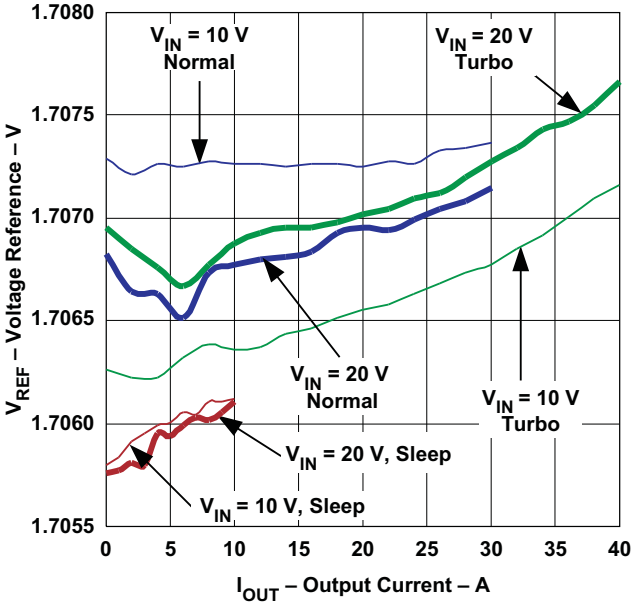


Figure 12.

OPERATING FREQUENCY
vs
OUTPUT CURRENT

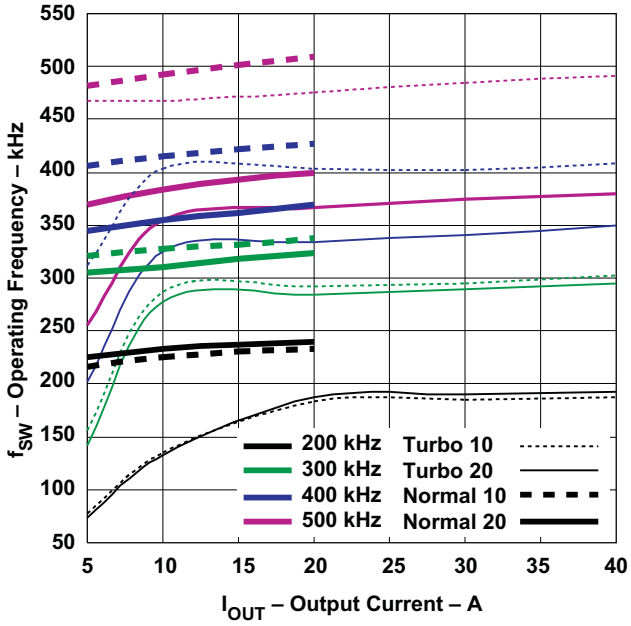


Figure 13.

EFFICIENCY
vs
OUTPUT VOLTAGE

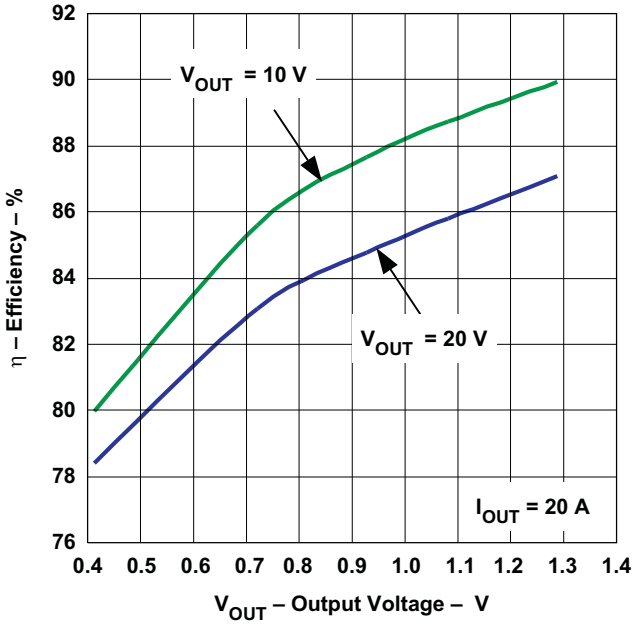


Figure 14.

EFFICIENCY
vs
INPUT VOLTAGE

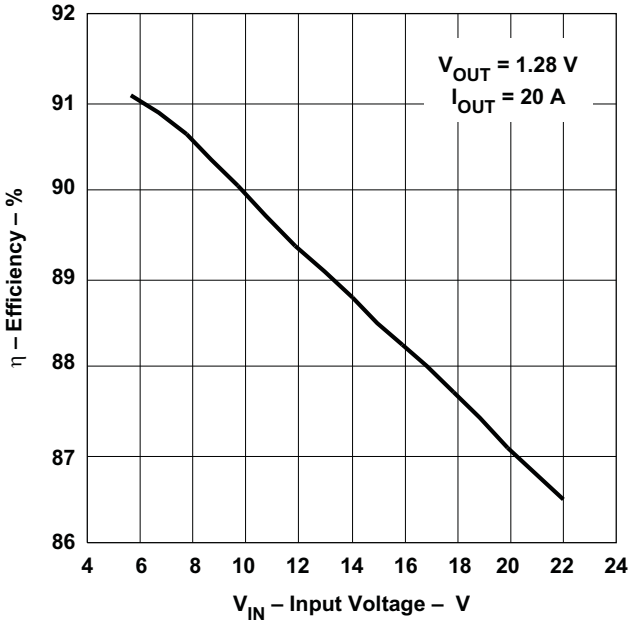


Figure 15.

TYPICAL CHARACTERISTICS

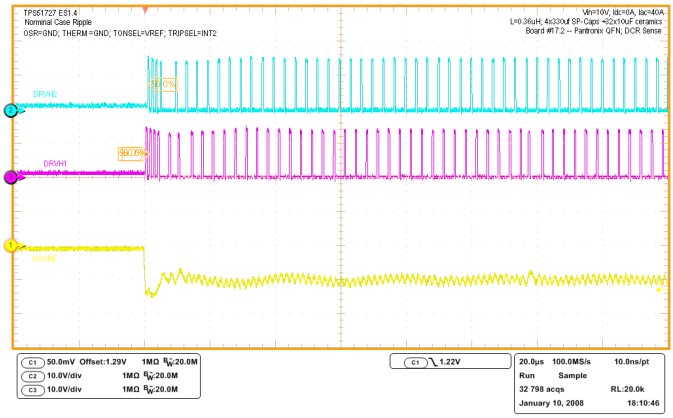


Figure 16. Transient Load Onset, V_{IN} = 10 V

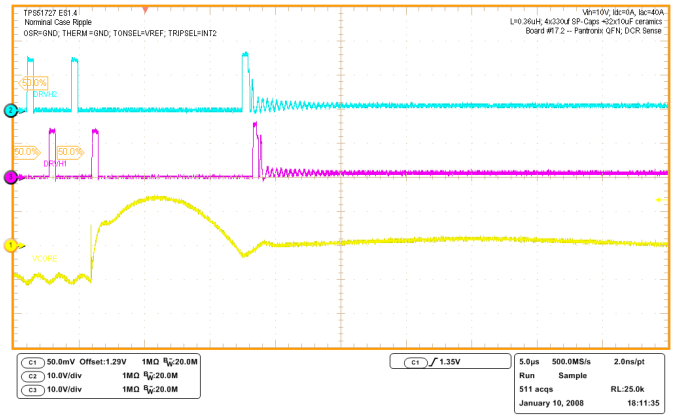


Figure 17. Transient Load Release, V_{IN} = 10 V

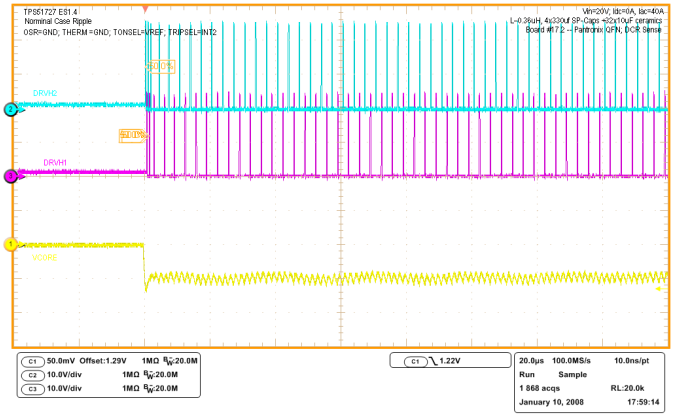


Figure 18. Transient Load Onset, V_{IN} = 20 V

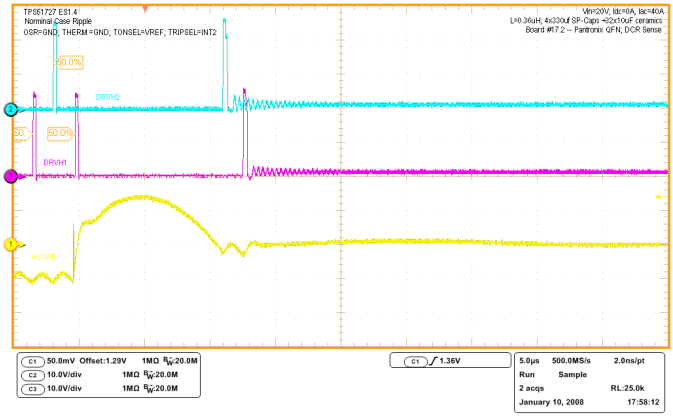


Figure 19. Transient Load Release, V_{IN} = 20 V

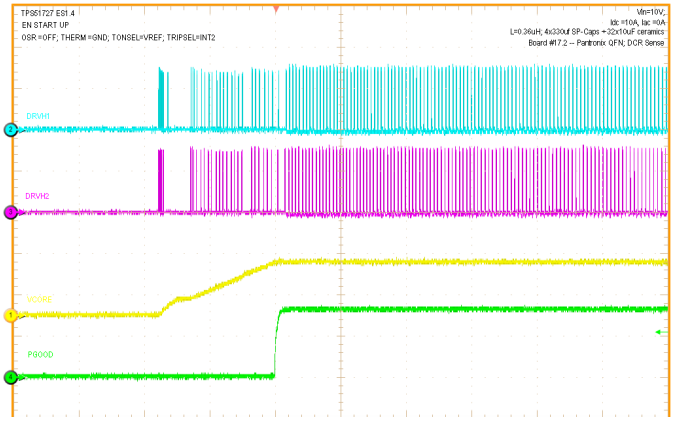


Figure 20. Typical Start-Up to 1.1-V VID

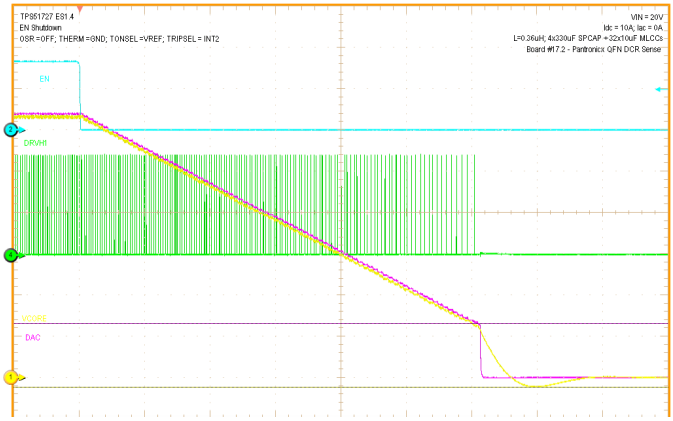


Figure 21. Typical Soft-Stop Waveform

TYPICAL CHARACTERISTICS (continued)

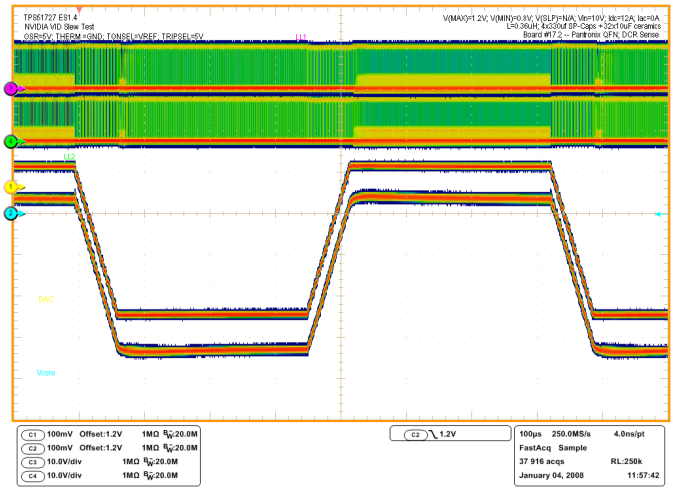


Figure 22. Typical VID Slew (Envelope Mode)

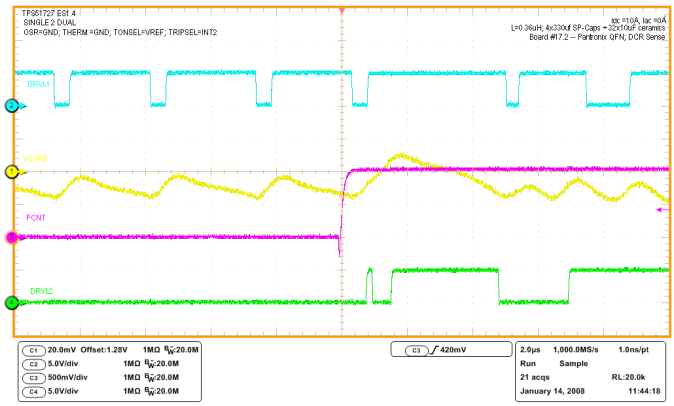


Figure 23. Typical PCNT Phase Add

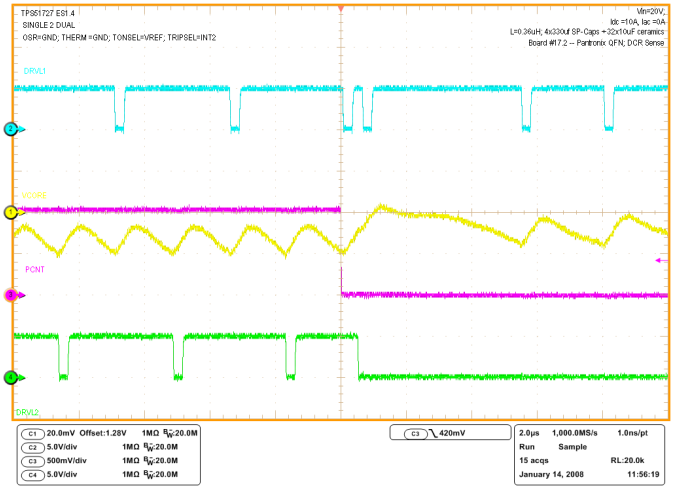


Figure 24. Typical PCNT Phase Drop

DETAILED DESCRIPTION

FUNCTIONAL OVERVIEW

The TPS51727 is a DCAP+™ mode adaptive on-time converter. The output voltage is set using the 5-bit VID code defined in Table 3. "VID-on-the-fly" transitions are supported with the slew rate controlled by a single resistor on the ISLEW pin. Two powerful integrated drivers support output currents in excess of 50 A. The converter enters single phase mode under PCNT control to optimize light-load efficiency. Four switching frequency selections are provided in 100-kHz increments from 200-kHz to 500-kHz per phase to enable optimization of the power chain for the cost, size and efficiency requirements of the design. (See Table 2)

Table 2. Frequency Selection Table

TONSEL VOLTAGE (V_{TONSEL}) (V)	FREQUENCY (kHz)
GND	200
VREF	300
3.3	400
5	500

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS51727, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the DAC voltage and the feedback voltage.

This approach has two advantages:

1. The amplifier DC gain sets an accurate linear load-line; this is required for many processing applications.
2. The error voltage input to the PWM comparator is filtered to improve the noise performance.

In a steady-state condition, the two phases of the TPS51727 switch 180° out-of-phase. The phase displacement is maintained both by the architecture (which does not allow both top gate drives to be on in any condition) and the current ripple (which forces the pulses to be spaced equally). The controller forces current sharing adjusting the on-time of each phase. Current balancing requires no user intervention, compensation, or extra components.

Multi-Phase, PWM Operation

Referring to Figure 1, in dual-phase steady state, continuous conduction mode, the converter operates as follows: Starting with the condition that both top MOSFETs are off and both bottom MOSFETs are on, the summed current feedback (V_{CMP}) is higher than the error amplifier output (V_{DROOP}). V_{CMP} falls until it hits V_{DROOP}, which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.

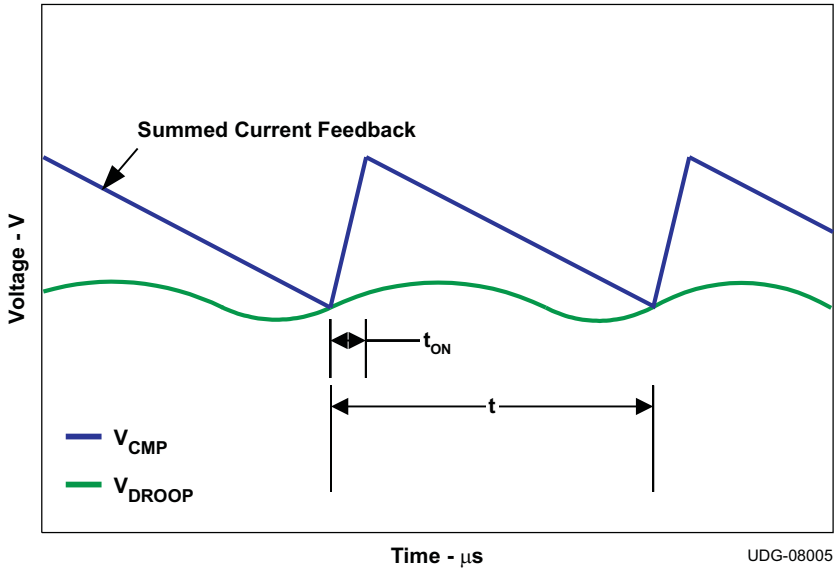


Figure 25. D-CAP+™ Mode Basic Waveforms

The summed current feedback is an amplified and filtered version of the CSPx and CSNx inputs. The TPS51727 provides dual independent channels of current feedback to increase the system accuracy and reduce the dependence of circuit performance on layout compared to an externally summed architecture.

PWM Frequency and Adaptive on Time Control

The on-time (at the LL node) is determined by Equation 1.

$$t_{ON} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f_{SEL}}\right) + 30\,ns \quad (1)$$

where

- f_{SEL} is the frequency selected by the connection of the TONSEL pin

The on-time pulse is sent to the top MOSFET. The inductor current and summed current feedback rise to their maximum value, and the multiplexer and de-multiplexer switch to the next phase. Each ON pulse is latched to prevent double pulsing. The current sharing circuitry compares the average values of the individual phase currents, then adds or subtracts a small amount from each on-time in order to bring the phase currents into line. No user design is required.

Accurate droop is provided by the finite gain of the droop amplifier. The equation for droop is shown in Equation 2.

$$V_{DROOP} = \frac{R_{CS} \times A_{CS} \times \sum I(L)}{R_{DROOP} \times G_M} \quad (2)$$

In Equation 2, R_{CS} is the effective current sense resistance, when using a sense resistor or inductor DCR is used. A_{CS} is the gain of the current sense amplifier, ΣI(L) is the DC sum of inductor currents, R_{DROOP} is the value of resistor from the DROOP pin to VREF, and G_M(droop) is the transconductance of the droop amplifier.

The capacitor in parallel with R_{DROOP} matches the slew rate of the DROOP pin with the current feedback signals to prevent *ring-back* during transient load conditions.

AutoBalance™ Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase. The block diagram is shown in Figure 26.

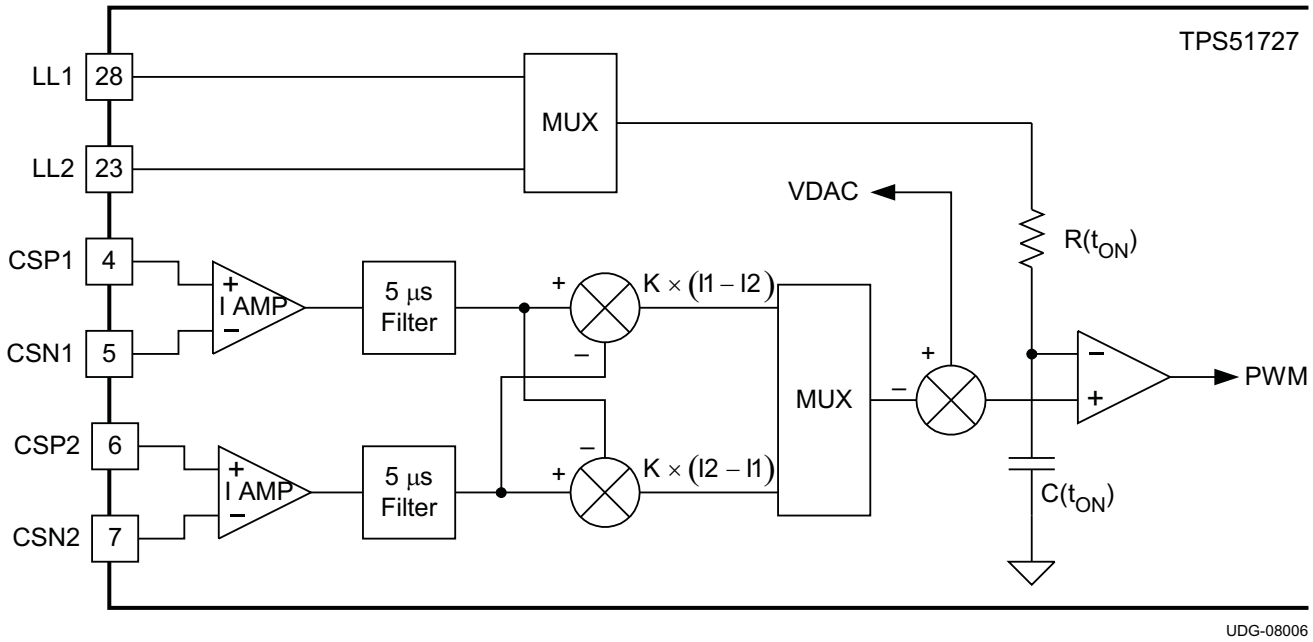


Figure 26. Current Sharing Block Diagram

Figure 26 also shows the TI D-Cap™ constant on-time modulator. The PWM comparator (not shown) starts a pulse when the feedback voltage meets the reference. This pulse turns on the gate of the high-side MOSFET. After the MOSFET turns on, the LL voltage for that phase is driven up to the battery input. This charges $C(t_{ON})$ through $R(t_{ON})$. The pulse is terminated when the voltage at $C(t_{ON})$ matches the t_{ON} reference, normally the DAC voltage (V_{DAC}).

The block diagram in Figure 26 and Figure 27 show the circuit action at the level of an individual pulse (PWM1). First assume that the 5-µs averaged value of I1 = I2. In this case, the PWM modulator terminates at V_{DAC}, and the normal pulse width is delivered to the system.

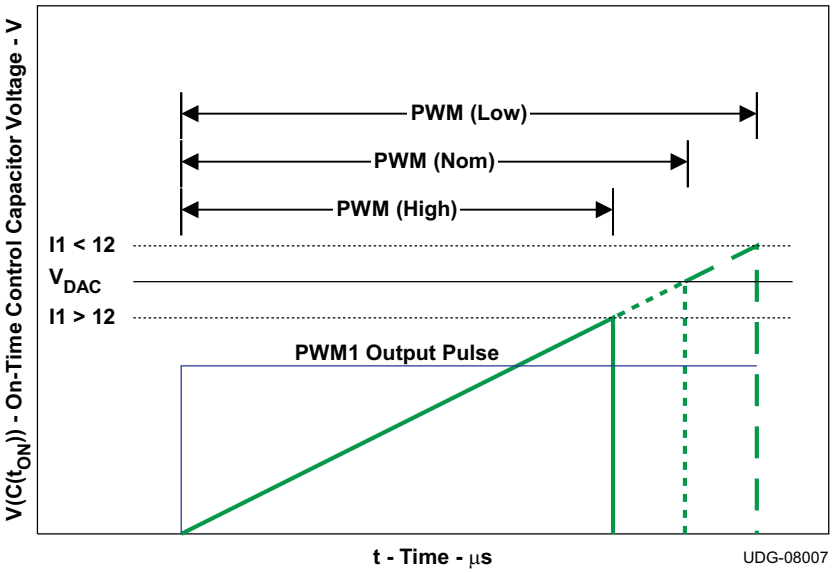


Figure 27. Current Sharing Operation

If instead, I1 > I2, then an offset is subtracted from V_{DAC}, and the pulse width for phase one is shortened, reducing the current in phase one to compensate. If I1 < I2, then a longer pulse is produced, again compensating on a pulse-by-pulse basis.

Because the increase in pulse width is proportional to the difference between the actual phase current and the ideal current, the system converges smoothly to equilibrium. Because the filtering is so much lighter than conventional current sharing schemes, the settling time is very fast. Analysis shows the response to be single pole with a bandwidth in the tens of kHz depending on circuit parameters. Detailed analysis of the current sharing circuit is available upon request.

The speed advantage allows the TPS51727 to quickly move from full speed to idle and back to save power when processing light and moderate loads. A multi-phase converter that takes milliseconds to implement current sharing will never be in equilibrium and thermal hot-spots can result. The TPS51727 allows rapid dynamic current and output voltage changes while maintaining current balance.

Overshoot Reduction (OSR™) Feature

The problem of overshoot in low duty-cycle synchronous buck converters results from the output inductor having a small voltage (V_{OUT}) with which to respond to a transient load release.

In Figure 28, a single phase converter is shown for simplicity. In an ideal converter, with the common values of 12-V input and 1.2-V output, the inductor has 10.8 V (12 V – 1.2 V) to respond to a transient step, and 1.2 V to respond once the load releases.

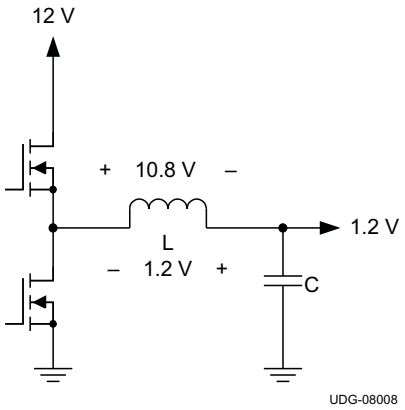


Figure 28. Synchronous Converter

Figure 29 shows a two-phase converter. The energy in the inductor is transferred to the capacitance on the V_{OUT} node above and the output voltage (green trace) overshoots the desired level (lower cursor, also green). In this case, the magnitude of the overshoot is approximately –40 mV. The LLx waveforms (yellow and blue traces) remain flat during the overshoot, indicating the DRVLx signals are on.

The performance of the same dual phase circuit, but with OSR enabled is shown in Figure 30. In this case, the low side FETs shut off when overshoot is detected and the energy in the inductor is partially dissipated by the body diodes. The overshoot is reduced by 20 mV. The dips in the LLx waveforms show the DRVLx signals are OFF only long enough to reduce the overshoot.

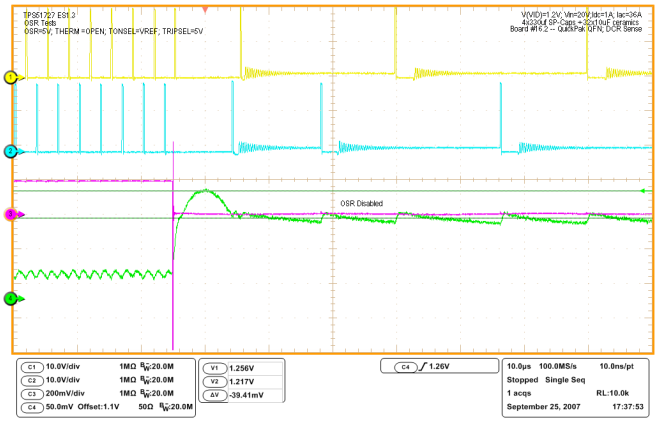


Figure 29. CIrcuit Performance Without Overshoot Reduction

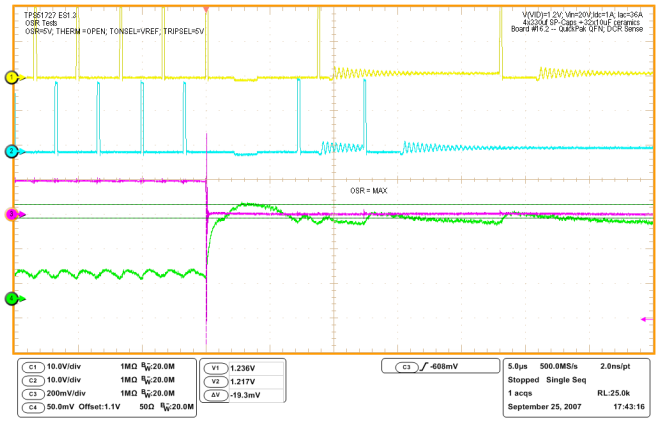


Figure 30. Transient Release Performance Improved with Overshoot Reduction

Implementation

OSR is implemented using a comparator between the DROOP and CMP nodes in Figure 1. To implement OSR, simply terminate the OSRSEL pin to the desired voltage to set the threshold voltage for the comparator. The settings are:

- GND = Minimum voltage (Maximum reduction)
- VREF = Medium voltage
- +3.3V = Maximum voltage
- 5V = OSR off

Use the highest setting that provides the desired level of overshoot reduction to eliminate the possibility of false OSR operation.

Light Load Power Saving Features

The TPS51727 has several power saving features to provide excellent efficiency over a very large load range. One is the PCNT pin. This pin has a low voltage I/O level which can work with logic signals from 1V to 3.6V. A LO on this pin puts the converter into single phase mode, thus eliminating the quiescent power of phase two when high power is not needed.

In addition, the TPS51727 has an automatic pulse skipping "skip" mode. Regardless of the state of the logic inputs, the converter senses negative inductor current flow and prevents it by shutting off the bottom MOSFET(s). This saves power by eliminating recirculating current. When the bottom MOSFET shuts off, the converter enters discontinuous mode, and the switching frequency decreases, thus reducing switching losses as well.

The SLP signal is used to enter a low-power state where unnecessary circuitry is powered down to save quiescent current for the lightest load conditions

MOSFET Drivers

The TPS51727 incorporates a pair of strong, high-performance gate drives with adaptive cross-conduction protection. The driver uses the state of the DRVLx and LLx pins to be sure the top or bottom MOSFET is off before turning the other on. Fast logic and high drive currents (up to 8 A typical!) quickly charge and discharge MOSFET gates to minimize dead-time to increase efficiency. The top gate driver also includes an internal P-N junction bootstrap diode, decreasing the size and cost of the external circuitry. For maximum efficiency, this diode can be bypassed externally by connecting Schottky diodes from V5IN (anode) to VBSTx (cathode).

Voltage Slewing

The TPS51727 ramps the internal DAC up and down to perform all voltage transitions. The timing is independent of switching frequency, as well as output resistive and capacitive loading. It is set by a resistor from the ISLEW pin to AGND (R_{SLEW}). All voltage transitions have a single slew rate.

$$R_{SLEW} = \frac{K_{SLEW} \times V_{SLEW}}{SR} \quad (3)$$

where

- $K_{SLEW} = 1.25 \times 10^9$
- $V_{SLEW} = 1.25$ V
- SR is the desired slew rate in units of mV/µs

V_{SLEW} is equal to the slew reference, $V_{SLEWREF}$ when R_{SLEW} is tied to GND. Connecting R_{SLEW} to VREF disables over-voltage protection (OVP) and changes V_{SLEW} in Equation 3 to 0.45 V ($V_{VREF} – V_{SLEWREF}$).

The soft start time to the voltage defined by the VID code at power-up is shown in Equation 4.

$$t_{SS} = \frac{V_{VID}}{SR} (s) \quad (4)$$

Soft Stop Control with Low Impedance Output Termination

The voltage slewing capability is also used to slowly slew the voltage down for a soft-stop without undershoot. The soft-stop rate equals the soft-start rate. As long as V5IN is available and EN toggles low, the TPS51727 slews from the current VID to 0.3 V. At this point, all DRVxx signals are held LO and an internal transistor connected from VFB to AGND turns on to keep V_{OUT} from floating up as a result of stray leakage currents.

Protection Features

The TPS51727 features full protection of the converter power chain as well as the system electronics.

Input Undervoltage Protection (UVLO)

The TPS51727 continuously monitors the voltage on the V5FILT pin to ensure the value is high enough to bias the devices properly and provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.4 V and has a nominal 200 mV of hysteresis. This function is not latched, therefore removing and restoring 5-V power to the device resets it. The power input (V_{BAT}) does not include a UVLO function, so the circuit runs with power inputs down to approximately 3 × V_{OUT}.

Power Good Signals

The TPS51727 has an open-drain power good pin, PGOOD. The high threshold is nominally VDAC +200 mV; the low threshold is nominally VDAC –300 mV. PGOOD goes inactive as soon as the EN pin is pulled low or an undervoltage condition on VOUT is detected. It is masked during DAC transitions to prevent false triggering during voltage slewing. When overvoltage protection is turned off, PGOOD continues to indicate an overvoltage condition.

Output Overvoltage Protection (OVP)

In addition to the power good function described above, the TPS51727 has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when V_{OUT} is greater than 200 mV greater than V_{DAC}. In this case, the converter sets PGOOD signal inactive, performs the soft-stop sequence, and then latches OFF. The converter remains in this state until the device is reset by cycling either V5IN or EN. However, because of the dynamic nature of the processor systems, the +200mV OVP threshold is “blanked” much of the time. In order to provide protection to the processor 100% of the time, there is a second OVP level fixed at 1.7 V which is always active. If the fixed OVP condition is detected, PGOOD is forced inactive and the DRVLx signals are driven HI. The converter remains in this state until either V5IN or EN are cycled. OVP is disabled when the R_{SLEW} is terminated to VREF instead of GND. In this case, change the value of R_{SLEW} as described in the *Voltage Slewing* section above.

Ouptut Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described below. If V_{OUT} drops below the low PGOOD threshold for 80 µs, then the converter enters soft-stop mode and latches OFF at the completion of soft stop.

Current Protection

Two types of current protection are provided in the TPS51727.

- Overcurrent protection (OCP)
- Negative overcurrent protection

Overcurrent Protection (OCP)

The TPS51727 uses a *valley* current limiting scheme, so the OCP set point is the OCP limit minus half of the ripple current. Current limiting occurs on a phase-by-phase and pulse-by-pulse basis. If the sensed current value is above the OCP setting, the converter holds off the next ON pulse until the current ramp drops below the OCP limit. Refer to the *Electrical Characteristics* table to choose the appropriate TRIPSEL value.

In OCP, the voltage droops until the UVP limit is reached. Then, the converter sets PGOOD signal inactive, performs the soft-stop sequence, and then latches OFF. The converter remains in this state until the device is reset.

Negative Overcurrent Protection

The negative OCP circuit acts when the converter is sinking current. The converter continues to act in a *valley* mode, so to have a similar negative DC limit, the absolute value of the negative OCP set point is typically 50% higher than the positive OCP set point.

Thermal Protection

Two types of thermal protection are provided in the TPS51727

- Thermal flag open drain ouptut signal ($\overline{\text{THAL}}$)
- Thermal shutdown

Thermal Flag Open Drain Ouptut Signal $\overline{\text{THAL}}$

The $\overline{\text{THAL}}$ signal is an open-drain signal that is used to protect the V_{OUT} power chain. To use $\overline{\text{THAL}}$, place an NTC thermistor at the hottest area of the PC board and connect it to the THRM pin. THRM sources a precise 60-µA current, and $\overline{\text{THAL}}$ goes LO when the voltage on THRM reaches 0.72 V. Therefore, the NTC thermistor needs to be 11.7 kΩ at the trip level. A series or parallel resistor can be used to trim the resistance to the desired value at the trip level.

$\overline{\text{THAL}}$ causes the processor to draw less current. The TPS51727 continues to operate normally.

Thermal Shutdown

The TPS51727 includes an internal temperature sensor. When the temperature reaches a nominal 160°C, the device shuts down until the temperature cools approximately 10°C and the EN pin or 5-V power is recycled.

Power Monitor

The TPS51727 includes a power monitor function. The power monitor puts out an analog voltage proportional to the output power on the PMON pin.

$$V_{PWRMON} = K_{PWR} \times V_{DAC} \times \sum V_{CS} \quad (5)$$

In Equation 5 K_{PWR} is given in the *Electrical Characteristics* table and Σ V_{CS} is the sum of the voltages at the inputs to the current sense amplifiers.

Power Sequencing

The TPS51727 is not sensitive to power sequencing if the EN pin comes up after all other voltages have settled. If EN is tied to 3.3 V without being controlled by a logic signal, 5 V must come up first. The VID lines must be valid within 10 µs of the time when EN goes high.

VID TABLE

Table 3. VID TABLE

EN	VID					VDAC (V) –3% Offset
	4	3	2	1	0	
1	0	0	0	0	0	1.250
1	0	0	0	0	1	1.225
1	0	0	0	1	0	1.200
1	0	0	0	1	1	1.175
1	0	0	1	0	0	1.150
1	0	0	1	0	1	1.125
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.075
1	0	1	0	0	0	1.050
1	0	1	0	0	1	1.025
1	0	1	0	1	0	1.000
1	0	1	0	1	1	0.975
1	0	1	1	0	0	0.950
1	0	1	1	0	1	0.925
1	0	1	1	1	0	0.900
1	0	1	1	1	1	0.875
1	1	0	0	0	0	0.850
1	1	0	0	0	1	0.825
1	1	0	0	1	0	0.800
1	1	0	0	1	1	0.775
1	1	0	1	0	0	0.750
1	1	0	1	0	1	0.725
1	1	0	1	1	0	0.700
1	1	0	1	1	1	0.675
1	1	1	0	0	0	0.650
1	1	1	0	0	1	0.625
1	1	1	0	1	0	0.600
1	1	1	0	1	1	0.575
1	1	1	1	0	0	0.550
1	1	1	1	0	1	0.525
1	1	1	1	1	0	0.500
1	1	1	1	1	1	0.400
0	X	X	X	X	X	0.000

APPLICATION INFORMATION

Design Procedure

The following section describes a very simple design procedure for the TPS51727, as a high-performance dual phase power controller.

Choosing Initial Parameters

Step One

Determine the output requirements. For the purposes of this document, we use the following parameters for the design procedure.

The processor requirements provide the following key parameters.

- $V_{OUT(max)}$ = 1.05 V
- R_{OUT} = -1.0 mΩ
- I_{MAX} = 40 A
- I_{DYN} = 30 A
- Slew rate = 5.0 mV/µs (minimum)

The TPS51727 architecture is designed to work with a load line defined by R_{OUT}. The output voltage drops by an accurately defined amount as the output current increases. The minimum supported load-line is –1.0mΩ.

Step Two

Determine system parameters. The input voltage range and operating frequency are of primary interest. For example:

1. $V_{IN(max)}$ = 15 V
2. $V_{IN(min)}$ = 8 V
3. *f* = 300 kHz

Step Three

Determine current sensing method. The TPS51727 supports both resistor sensing and inductor DCR sensing. Inductor DCR sensing is chosen. For resistor sensing, substitute the resistor value (1 mΩ recommended for a 40-A application) for RCS in the subsequent equations and skip Step Four.

Step Four

Determine inductor value and choose inductor. Smaller values of inductor have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 30% to 50% of the maximum current per phase. In this case, use 40%.

$$I_{P-P} = \frac{40\,A}{2\,phases} \times 0.4 = 8.0\,A \tag{6}$$

At *f* = 300 kHz, with a 15-V input and a 1.05-V output:

$$L_{MAX} = \frac{V \times dT}{I_{P-P}} \tag{8}$$

where

- $V = V_{IN(max)} - V_{OUT(max)}$

$$dT = \frac{V_{OUT(max)}}{f \times V_{IN(max)}} \tag{7}$$

L_{MAX} = 0.406 µH

To allow for inductor tolerances, 0.36 µH is chosen. The inductor must not saturate during peak loading conditions.

$$I_{SAT} = \left(\frac{I_{MAX}}{N_{PHASE}} + \frac{I_{P-P}}{2} \right) \times 1.5 = 36\,A \quad (9)$$

The factor of 1.5 allows for current sensing and current limiting tolerances. The chosen inductor should have the following characteristics:.

1. Create an inductance vs. current curve that is as flat as possible. Inductor DCR sensing is based on the idea L/DCR is approximately a constant through the current range of interest.
2. Either high saturation or “soft saturation”.
3. Low DCR for improved efficiency, but at least 0.7 mΩ for proper signal levels.
4. DCR tolerance as low as possible for load-line accuracy.

   For this application, a 0.36-µH, 1.2-mΩ inductor is chosen

Step Five

Design the thermal compensation network. In most designs, NTC thermistors are used to compensate thermal variations in the resistance of the inductor winding. This winding is generally copper, and so has a resistance coefficient of 3900 PPM/C. NTC thermistors, on the other hand, have very non-linear characteristics and need two or three resistors to linearize them over the range of interest. The typical DCR circuit is shown in Figure 31.

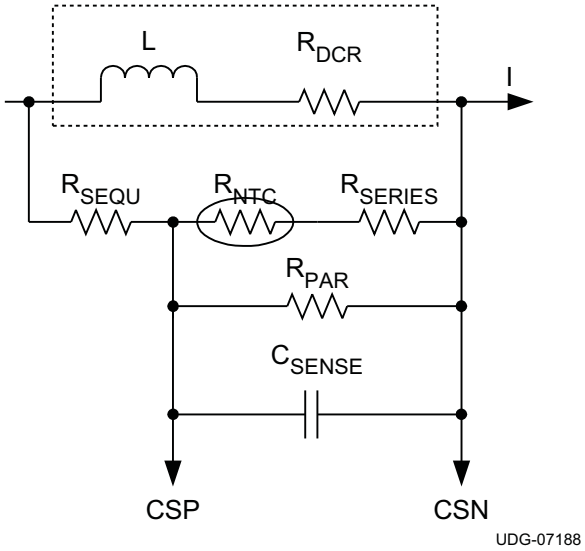


Figure 31. Typical DCR Sensing Circuit

In this circuit, good performance is obtained when:

$$\frac{L}{R_{DCR}} = C_{SENSE} \times R_{EQ} \quad (10)$$

In Equation 10, all of the parameters are defined in Figure 26 except R_{EQ}, which is the series/parallel combination of the other four discrete resistors. C_{SENSE} should be a capacitor type which is stable over temperature; use X7R or better dielectric (C0G preferred).

Since calculating these values by hand is difficult, TI has a spreadsheet using the Excel "Solver" function available to calculate them. Please contact your local TI representative to get a copy of the spreadsheet.

In the reference design, the following values are input to the spreadsheet::

- L
- R_{DCR}
- Load Line (R_{OUT})
- Thermistor R25 and "b" value

The spreadsheet then calculates R_{SEQU}, R_{SERIES}, R_{PAR}, and C_{SENSE}. In this case, the nearest standard values are:

- R_{SEQU} = 24.9 kΩ
- R_{SERIES} = 43.2 kΩ
- R_{PAR} = 165 kΩ
- C_{SENSE} =18 nF

Note the effective divider ratio for the inductor DCR. The effective current sense resistance, $R_{CS(eff)}$ is shown in Equation 11.

$$R_{CS(eff)} = R_{DCR} \times \left(\frac{R_{P\_N}}{R_{SEQU} + R_{P\_N}} \right) \tag{11}$$

Step Six

Determine the output capacitor configuration. This depends on the transient specification of the load. If R_{OUT} is high enough, the transient specification can be met within the DC load-line. A successful design includes a combination of bulk and ceramic capacitance totaling at least 1200 µF.

Step Seven

Set the load line. The load line is set by the droop resistor knowing R_{OUT} and $R_{CS(eff)}$.

$$R_{DROOP} = \frac{R_{CS(eff)} \times A_{CS}}{G_M \times R_{OUT}} \tag{12}$$

R_{DROOP} = 11.0 kΩ

Step Eight

Calculate the droop capacitance. From Equation 13 .

$$C_{DROOP} = \frac{R_{OUT} \times I_{DYN} \times G_M \times L}{R_{CS} \times A_{CS} \times D_{MAX} \times V(L)} - 30\,pF = 50\,pF \tag{13}$$

The next smaller standard value, 47 pF, is chosen.

Step Nine

Calculate R_{SLEW}. R_{SLEW} sets the rate for all transitions including:

1. Start-up slew rate
2. Shutdown slew rate
3. VID change slew rate (+ or –)

$$R_{SLEW} = \frac{K_{SLEW} \times V_{SLEW}}{SR} \tag{14}$$

Here, the OVP is enabled, so R_{SLEW} is terminated to GND. K_{SLEW} = 1.25 × 10^9 and V_{SLEW} = 1.25 V. For a slew rate (SR) of 5.0 mV/µs, R_{SLEW} = 312.5 kΩ.

Step Ten

Calculate $\overline{\text{THAL}}$ components. The THRM pin puts out a nominal 60-µA current. The trip voltage is 0.75 V. Therefore, the resistance at the trip point needs to be 0.75 V / 61 µA = 12.3 kΩ. For a trip temperature of 85°C, the recommended 150 kΩ NTC thermistor is 10.3 kΩ. To move the trip point to the correct resistance, we add a series resistance of 2.0 kΩ. Depending on the thermistors selection and desired trip point, adding a parallel resistance to obtain the correct resistance at the trip point is also possible. In order to keep the sensing as accurate as possible in both cases, the contribution of the fixed resistance at the trip point should be as small as possible. If $\overline{\text{THAL}}$ is not used, leave both $\overline{\text{THAL}}$ and THRM open.

Step Eleven

Select decoupling and peripheral components.

For TPS51727 peripheral capacitors, use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always OK.

- V5IN decoupling ≥ 2.2µF, ≥ 10V
- V5FILT decoupling ≥ 1µF≥10V
- VREF decoupling 0.22µF to 1µF, ≥ 4V
- Bootstrap capacitors ≥ 0.22µF, ≥ 10V
- Bootstrap diodes (optional) 30-V Schottky diode, BAT-54 or better
- PMON filter, 10 kΩ, 5% resistor / 10 nF 20% capacitor
- Pull-up resistors. Use a 10-kΩ, 5% resistor, or as system requirements dictate.

For power chain and other component selection, see Table 1.

Layout Guidelines

The TPS51727 has fully differential current and voltage feedback. As a result, no special layout considerations are required. However, all high-performance multi-phase power converters, like the , require a certain level of care in layout.

Schematic Review

Because the voltage and current feedback signals are fully differential it is a good idea to double check their polarity.

- CSP1/CSN1
- CSP2/CSN2
- VFB/GFB

Specific Guidelines

Separate Noisy Driver Interface Lines from Sensitive Analog Interface Lines

The TPS51727 makes this as easy as possible, as the two sets of pins are on opposite sides of the device. In addition, the CPU interface signals are grouped on the top and bottom sides of the device. This arrangement is shown in Figure 32.

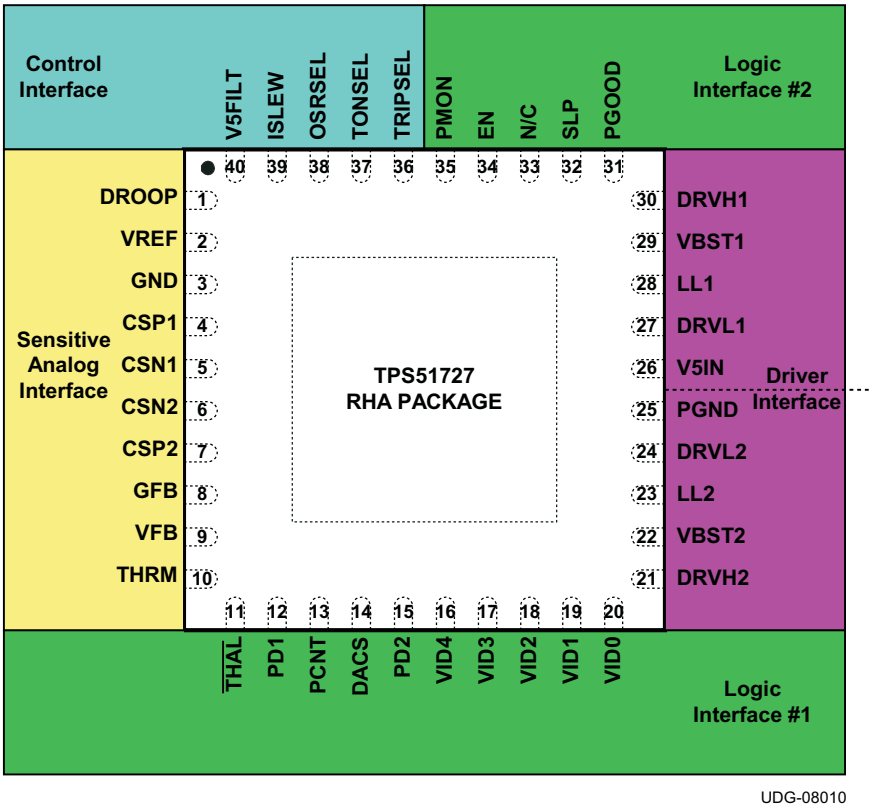


Figure 32. Device Layout by Pin Function

Given the physical layout of most systems, the current feedback (CSPx, CSNx) may have to pass near the power chain. Clean current feedback is required for good load-line, current sharing, and current limiting performance of the TPS51727. This requires the designer take the following precautions.

- Make a Kelvin connection to the pads of the resistor or inductor used for current sensing. See Figure 33 for a layout example.
- Lay out the current feedback signals as a differential pair to the device.
- Lay out the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane.
- Design the compensation capacitor for DCR sensing (C_{SENSE}) as close to the CS pins as possible.
- Design R_{PAR} next to C_{SENSE}.
- Design any noise filtering capacitors directly under the TPS51727 and connect to the CS pins with the shortest trace length possible.
- The ISLEW pin is susceptible to high frequency noise. Design the trace lengths to the slew resistor as short as possible and surround the pin and resistor with a guard ring of a quiet trace (analog ground is preferred).

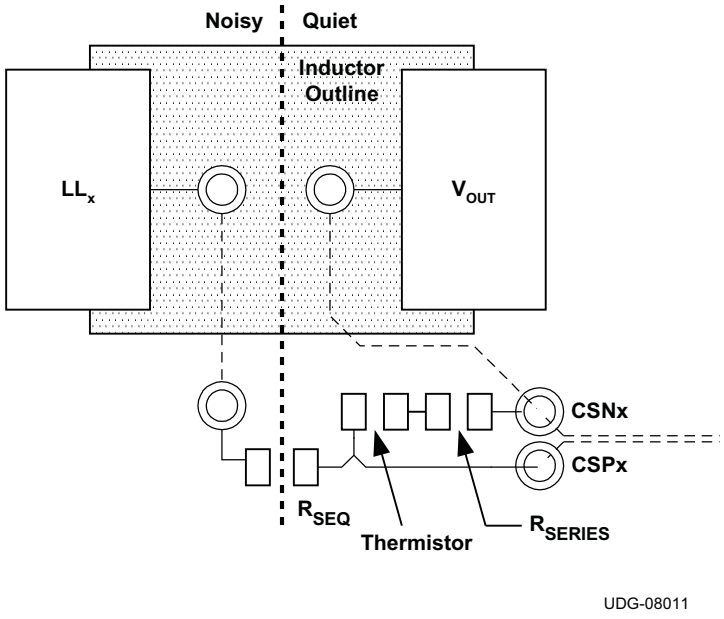


Figure 33. Make Kelvin Connections to the Inductor for DCR Sensing

- Ensure that all vias in the CSPx and CSNx traces are isolated from all other signals
- Lay out the dotted signal traces in internal planes
- If possible, change the name of the CSNx trace to prevent unintended connections to the V_{OUT} plane
- Design CSPx and CSNx as a differential pair in a quiet layer
- Design the capacittor as near to the device pins as possible

Minimize High Current Loops

Figure 34 shows the primary current loops in each phase, numbered in order of importance. The most important loop to minimize the area of is Loop 1, the path from the input capacitor through the high and low-side MOSFETs, and back to the capacitor through ground.

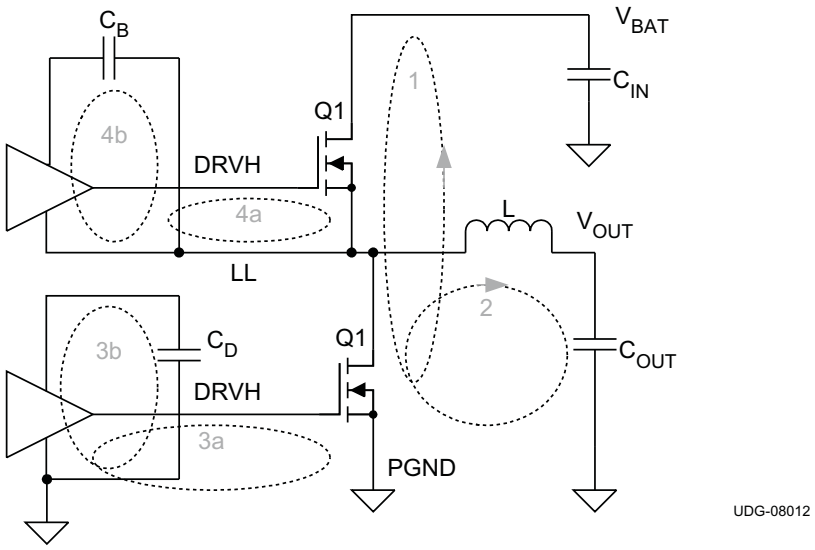


Figure 34. Major Current Loops Requiring Minimization

Loop 2 is from the inductor through the output capacitor, ground and Q2. The layout of the low-side gate drive (Loops 3a and 3b) is important. The guidelines for gate drive layout are:

- Make the low side gate drive as short as possible (1 inch or less preferred).
- Make the DRVL width to length ratio of 1:10, wider (1:5) if possible
- If changing layers is necessary, use at least two vias

A sample breakout of the driver side of the device is shown in Figure 35.

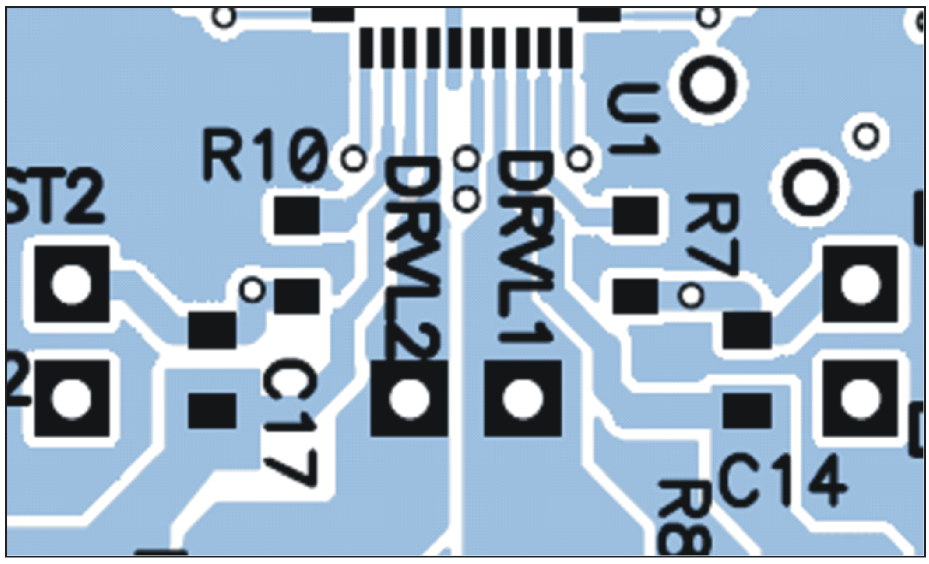


Figure 35. Recommended Gate Drive Section Breakout

Power Chain Symmetry

The TPS51727 does not require special care in the layout of the power chain components, because independent isolated current feedback is provided. Make every effort to lay out the phases in a symmetrical manner. The current feedback from each phase must be free of noise and have the same effective current sense resistance.

Place Analog Components as Close to the Device as Possible

Place components close to the device in the following order.

1. CS pin noise filtering components
2. DROOP pin compensation component
3. Decoupling capacitor
4. ISLEW resistor (R_{SLEW})

Grounding Recommendations

The TPS51727 has separate analog and power grounds, and a thermal pad. The normal procedure for connecting these is:

1. Connect the thermal pad to PGND.
2. Tie the thermal pad to the system ground plane with at least 4 small vias or one large via.
3. GND can be connected to any quiet space. A quiet space is defined as a spot where no power supply switching currents are likely to flow. This applies to all switching converters on the same board. Use a single point connection to the point, and pour a GND island around the analog components.
4. Make sure the bottom MOSFET source connection and the decoupling capacitors have plenty of vias.

Decoupling Recommendations

- Decouple V5 to PGND with at least a 2.2-µF ceramic capacitor. This fits best on the opposite side of the device.
- Use double vias to connect to the device.
- Decouple V5FILT with 1-µF to AGND with leads as short as possible.
- Decouple VREF to AGND with 0.22-µF, with short leads as short as possible.

Conductor Widths

- Maximize the widths of power, ground and drive signal connections.
- For conductors in the power path, be sure there is adequate trace width for the amount of current flowing through the traces.
- Make sure there are sufficient vias for connections between layers.
- Use a minimum of 1 via per ampere of current

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51727RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 100	TPS 51727	Samples
TPS51727RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 100	TPS 51727	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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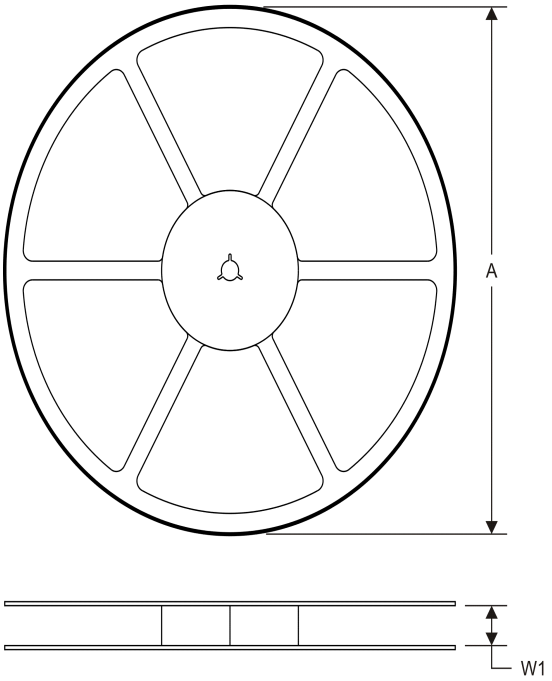
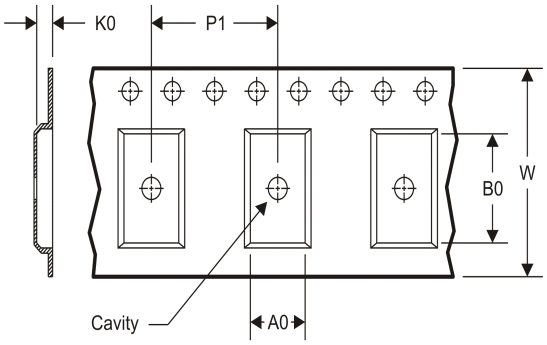
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



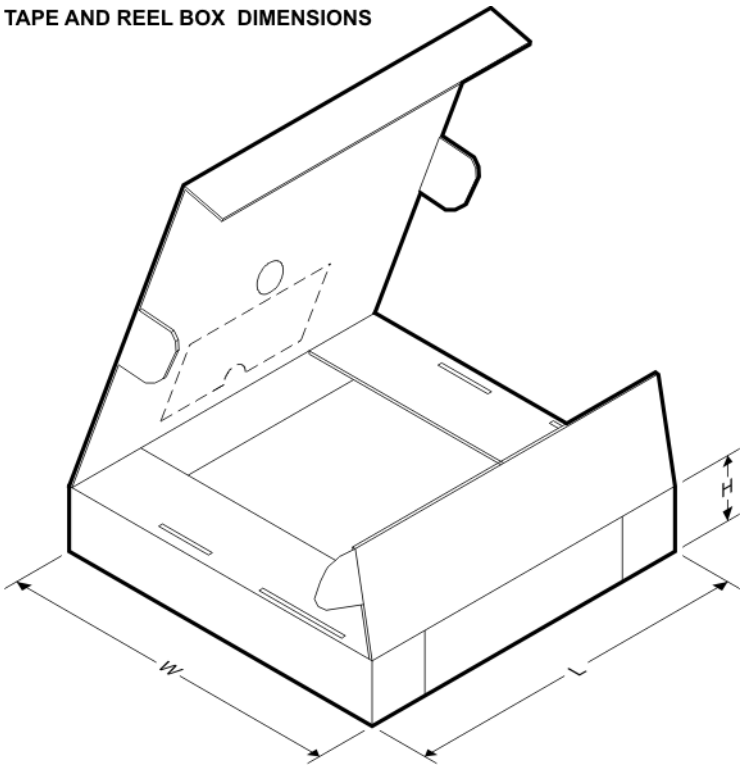
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51727RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS51727RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

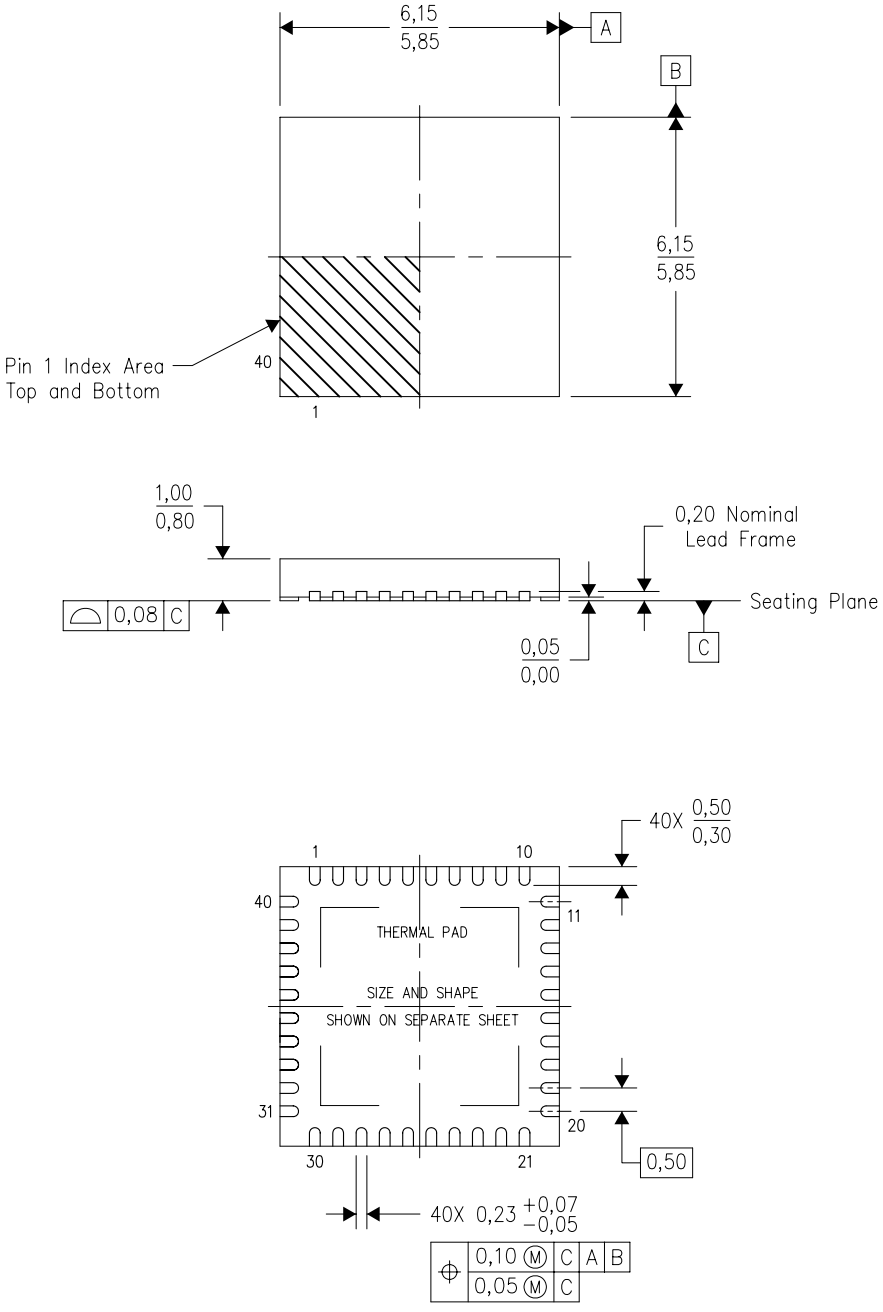
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51727RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS51727RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

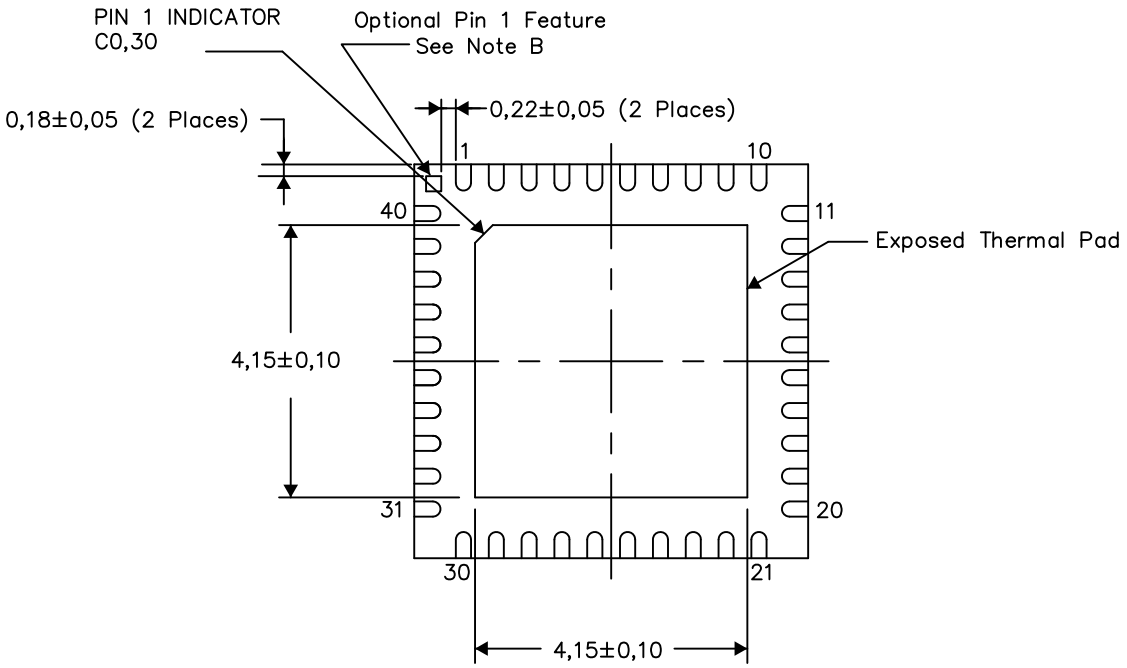
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

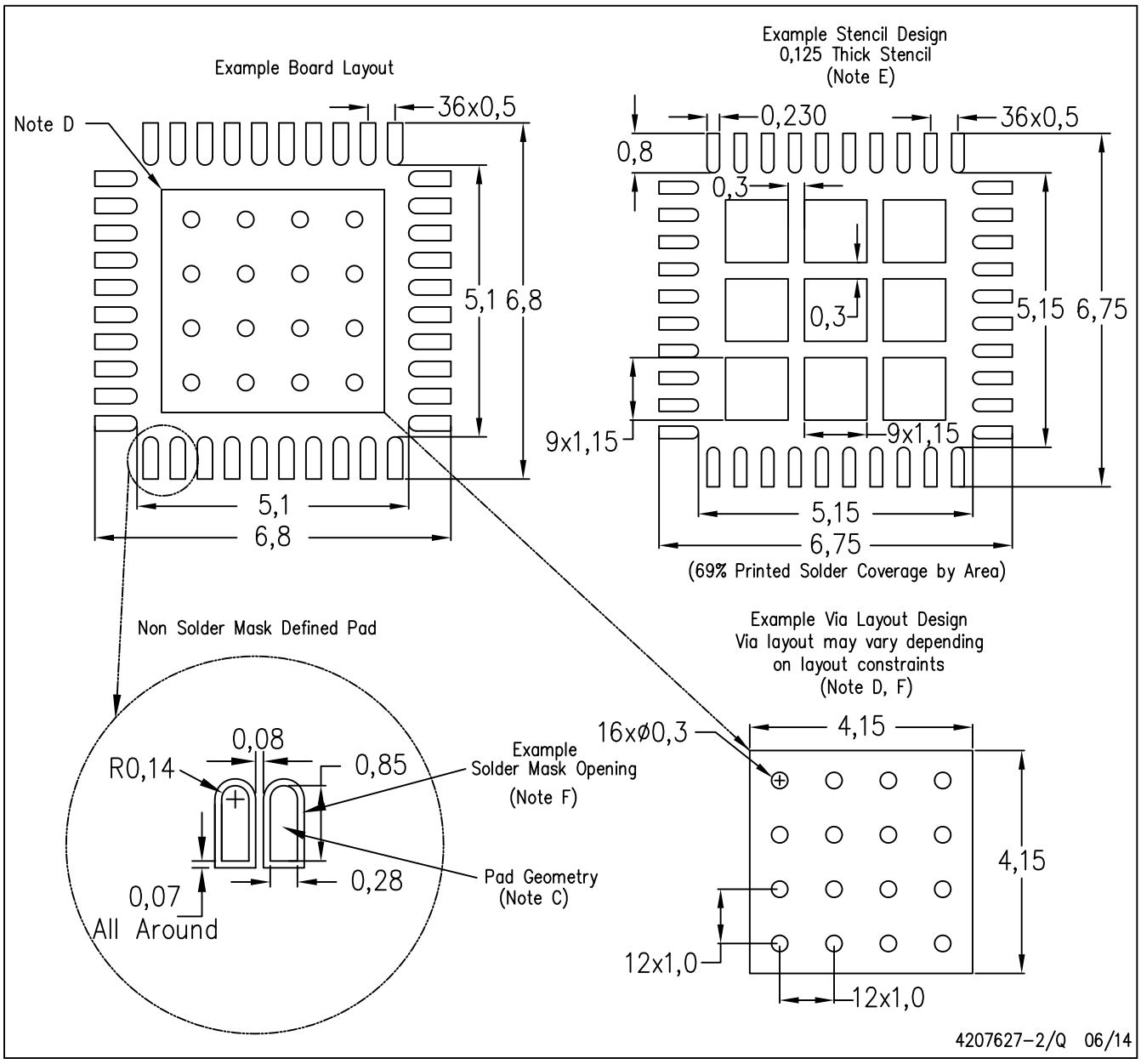
Exposed Thermal Pad Dimensions

4206355–2/W 06/14

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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