4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

Check for Samples: TS3DV421

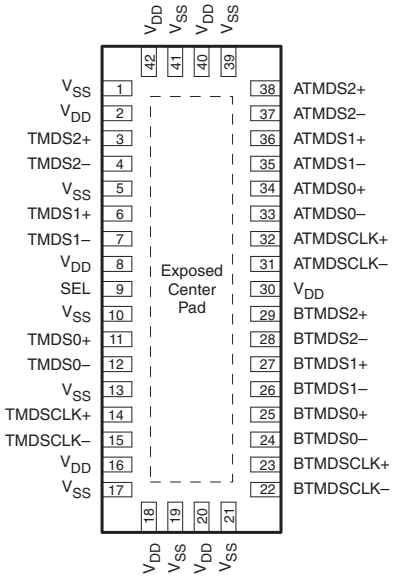
FEATURES

- **Compatible With HDMI v1.3 DVI 1.0 High-Speed Digital Interface**
  - **Wide Bandwidth of Over 3.8 Gbps**
  - **Serial Data Stream at 10× Pixel Clock Rate**
  - **Supports All Video Formats up to 1080p and SXGA (1280 × 1024 at 75 Hz)**
  - **High Bandwidth of 4.95 Gbps (Single Link)**
  - **HDCP Compatible**
- **Low Crosstalk (X_{TALK} = –50 dB Typ at 1.65 Gbps)**
- **Off Isolation (O_{IRR} = –50 dB Typ at 1.65 Gbps)**
- **Low Bit-to-Bit Skew ($t_{sk(o)}$ = 0.1 ns Max)**
- **Low and Flat ON-State Resistance (r_{ON} = 12.5 Ω Max, $r_{ON(flat)}$ = 0.5 Ω Typ)**
- **Low Input/Output Capacitance (C_{ON} = 4.5 pF Max)**
- **Enables Application-Specific Operating Voltage Selection**
  - **V_{DD} Operating Range From 1.5 V to 2.1 V When V_{SS} = GND**
  - **V_{DD} Operating Range From 3.0 V to 3.6 V When V_{SS} = 1.5 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **For DisplayPort Applications: V_{DD} = 1.8 V , V_{SS} = GND**
- **For HDMI /DVI Applications: V_{DD} = 3.3 V , V_{SS} = 1.5 V**

APPLICATIONS

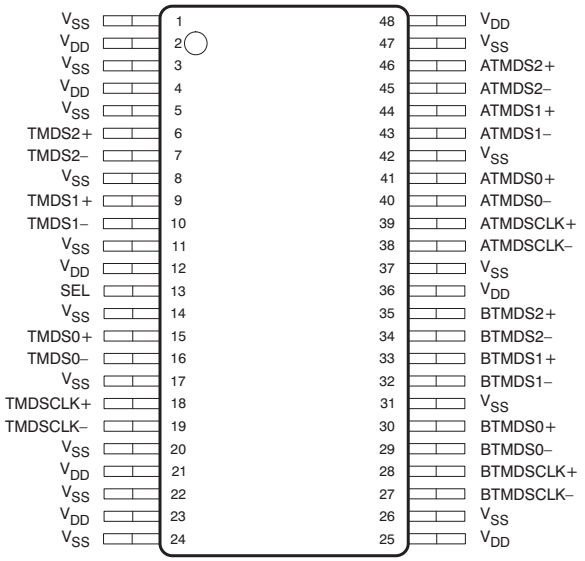
- **DVI/HDMI Signal Switching**
- **Differential DVI, HDMI Signal Multiplexing for Audio/Video Receivers and High-Definition Televisions (HDTVs)**

RUA PACKAGE
(TOP VIEW)



For RUA, the exposed center pad must be connected to V_{SS} or electronically open. For this part to be used in HDMI/TMDS applications, V_{SS} can be elevated to 1.5 V. See Figure 1.

DGV PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS3DV421 is a 4-channel differential 2:1 multiplexer/demultiplexer digital video switch controlled with one select input (SEL). SEL controls the data path of the multiplexer/demultiplexer and can be connected to any GPIO in the system, using an external voltage divider system. The device provides high bandwidth necessary for DVI and HDMI applications. This device expands the high-speed physical link interface from a single HDMI port to two HDMI ports (A or B port). The unselected channel is set to a high-impedance state.

The most common application for the TS3DV421 is in the sink application. In this case, there are two sources (i.e., DVD, set-top box, or game console) that must be routed to one HDMI receiver. The TS3DV421 can route the signals where one HDMI receiver (in a DLP, LCD TV, PDP, or other high-definition display) can be expanded to three ports.

The HDMI application calls for a 100-Ω differential impedance between the differential lines (TMDSn+ and TMDSn–). Additionally, because the TS3DV421 is a high-bandwidth, low-r_{ON} pass transistor-type switch, a properly designed board retains a 100-Ω differential impedance through the switch. The unselected port is in the high-impedance mode, such that the receiver receives information from only one source. HDCP encryption is passed through the switch for the HDMI receiver to decode.

Table 1. ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RUA	Tape and reel	TS3DV421RUAR	SD421
	TVSOP – DGV	Tape and reel	TS3DV421DGVR	SD421

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TYPICAL APPLICATION

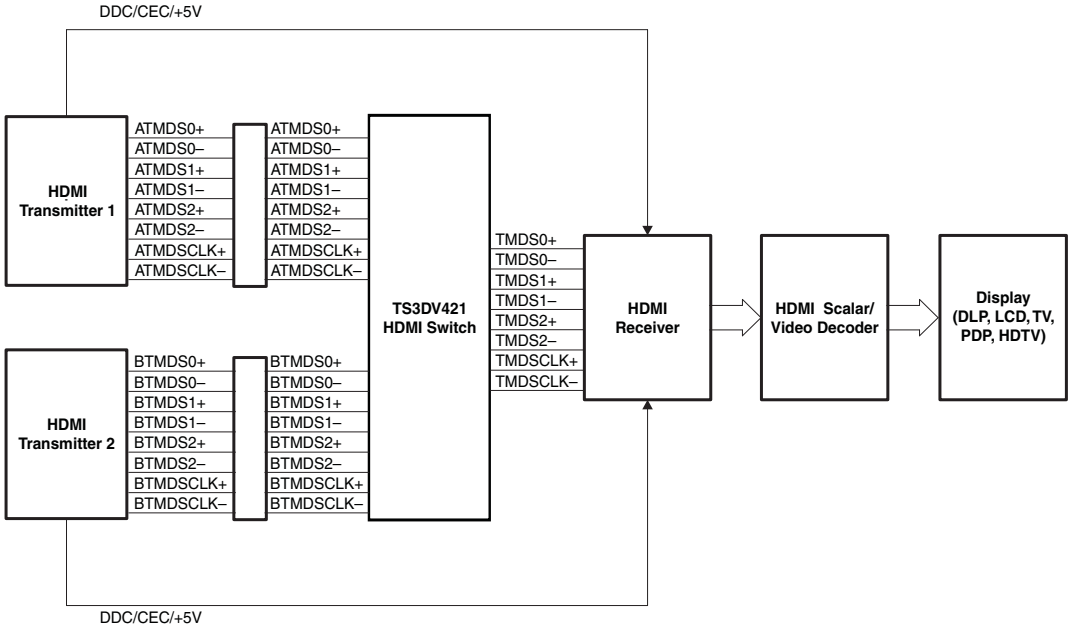
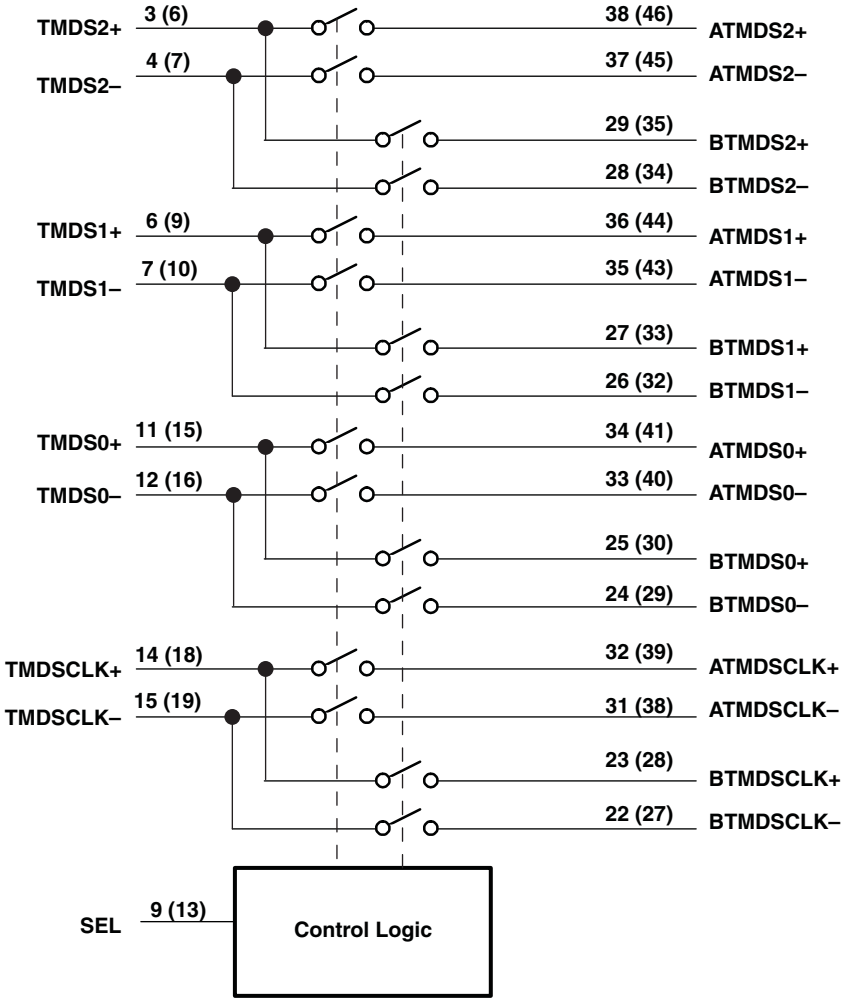


Table 2. FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn– = ATMDSn– TMDSCLK+ = ATMDSCLK+ TMDSCLK– = ATMDSCLK– BTMDSn+ = High impedance BTMDSn– = High impedance BTMDSCLK+ = High impedance BTMDSCLK– = High impedance	TMDSn+ TMDSn– TMDSCLK+ TMDSCLK–
H	TMDSn+ = BTMDSn+ TMDSn– = BTMDSn– TMDSCLK+ = BTMDSCLK+ TMDSCLK– = BTMDSCLK– ATMDSn+ = High impedance ATMDSn– = High impedance ATMDSCLK+ = High impedance ATMDSCLK– = High impedance	TMDSn+ TMDSn– TMDSCLK+ TMDSCLK–

FUNCTIONAL DIAGRAM



A. TVSOP package pin identification in parenthesis.

TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	QFN (RUA)	TVSOP (DGV)		
ATMDS0–	33	40	I/O	Port A, channel 0, TMDS negative signal
ATMDS0+	34	41	I/O	Port A, channel 0, TMDS positive signal
ATMDS1–	35	43	I/O	Port A, channel 1, TMDS negative signal
ATMDS1+	36	44	I/O	Port A, channel 1, TMDS positive signal
ATMDS2–	37	45	I/O	Port A, channel 2, TMDS negative signal
ATMDS2+	38	46	I/O	Port A, channel 2, TMDS positive signal
ATMDSCLK–	31	38	I/O	Port A TMDS negative clock
ATMDSCLK+	32	39	I/O	Port A TMDS positive clock
BTMDS0–	24	29	I/O	Port B, channel 0, TMDS negative signal
BTMDS0+	25	30	I/O	Port B, channel 0, TMDS positive signal
BTMDS1–	26	32	I/O	Port B, channel 1, TMDS negative signal
BTMDS1+	27	33	I/O	Port B, channel 1, TMDS positive signal
BTMDS2–	28	34	I/O	Port B, channel 2, TMDS negative signal
BTMDS2+	29	35	I/O	Port B, channel 2, TMDS positive signal
BTMDSCLK–	22	27	I/O	Port B TMDS negative clock
BTMDSCLK+	23	28	I/O	Port B TMDS positive clock
SEL	9	13	I	Select pin to choose between port A or port B. Referenced to V_{SS}
TMDS0–	12	16	I/O	TMDS channel 0 negative signal
TMDS0+	11	15	I/O	TMDS channel 0 positive signal
TMDS1–	7	10	I/O	TMDS channel 1 negative signal
TMDS1+	6	9	I/O	TMDS channel 1 positive signal
TMDS2–	4	7	I/O	TMDS channel 2 negative signal
TMDS2+	3	6	I/O	TMDS channel 2 positive signal
TMDSCLK–	15	19	I/O	TMDS negative clock
TMDSCLK+	14	18	I/O	TMDS positive clock
V_{DD}	2, 8, 16, 18, 20, 30, 40, 42	2, 4, 12, 21, 23, 25, 36, 48	Power	Positive power supply voltage
V_{SS}	1, 5, 10, 13, 17, 19, 21, 39, 41	1, 3, 5, 8, 14, 17, 20, 22, 24, 26, 31, 37, 42, 47	Power	Negative power supply voltage

ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted), - All voltages are with respect to V_{SS}

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	2.5	V
V_{IN}	Control input voltage range(2)		–0.5	2.5	V
$V_{I/O}$	Switch I/O voltage range(2) (3)		–0.5	2.5	V
I_{IK}	Control input clamp current	$V_{IN} < V_{SS}$		50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < V_{SS}$		50	mA
$I_{I/O}$	ON-state switch current(4)			100	mA
I_{DD}	Continuous current through V_{DD}			100	mA
I_{SS}	Continuous current through V_{SS}			100	mA
θ_{JA}	Package thermal impedance(5)	DGV package		58.0	°C/W
		RUA package		51.2	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(4) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	V_{SS} = GND	1.5	1.8	2.1	V
		V_{SS} = 1.5 V	3	3.3	3.6	
V_{IH}	High-level input voltage	3 V < V_{DD} < 3.6 V, V_{SS} = 1.5 V	0.65(V_{DD} – V_{SS}) + V_{SS}			V
V_{IL}	Low-level input voltage	1.5 V < V_{DD} < 2.1 V, V_{SS} = 0 V			0.35(V_{DD} – V_{SS}) + V_{SS}	V
V_{IO}	Switch input/output voltage		0		V_{DD}	V
T_A	Operating free-air temperature		0		85	°C

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY(1)

V_{DD} = 1.5 V to 2.1 V, V_{SS} = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 2.1 V,	I_{IN} = –18 mA				–0.7	–1.2	V
I_{IH}	SEL	V_{DD} = 2.1 V,	V_{IN} = V_{DD}					±1	µA
I_{IL}	SEL	V_{DD} = 2.1 V,	V_{IN} = V_{SS}					±1	µA
I_{off}		V_{DD} = 0,	V_O = 0 to 2.1 V,	V_I = 0				1	µA
I_{CC}		V_{DD} = 2.1 V,	$I_{I/O}$ = 0,	Switch ON or OFF			230	450	µA
C_{IN}	SEL	f = 1 MHz,	V_{IN} = 0				0.7	1	pF
C_{OFF}	B port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		1	1.5	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		4	4.5	pF
r_{on}		V_{DD} = 1.8 V,	V_{SS} ≤ V_I ≤ V_{DD},	I_O = –40 mA			12.5	20	Ω
$r_{on(flat)}$ (3)		V_{DD} = 1.8 V,	V_I = 1.65 V to 1.8 V	I_O = –40 mA			0.5		Ω
Δr_{on} (4)		V_{DD} = 1.8 V,	V_{SS} ≤ V_I ≤ V_{DD},	I_O = –40 mA			–0.1	0.2	Ω
Dynamic									
X_{TALK}		R_L = 50 Ω,	f = 825 MHz	See Figure 7			–50		dB
O_{IRR}		R_L = 50 Ω,	f = 825 MHz	See Figure 8			–50		dB
BW				See Figure 6			1.9		GHz
Max data rate				See Figure 6			3.8		Gbps

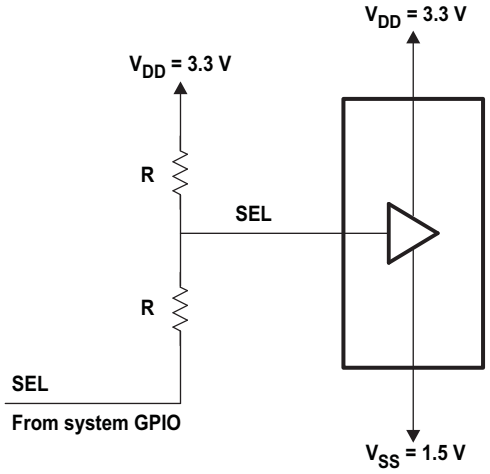
(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from centerports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 1.5 V to 2.1 V, V_{SS} = 0 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd} (2)	TMDSn or xTMDSn	xTMDSn or TMDSn		0.25		ns
t_{PZH}, t_{PZL}	SEL	TMDSn or xTMDSn	0.5		9	ns
t_{PHZ}, t_{PLZ}	SEL	TMDSn or xTMDSn	0.5		5	ns
$t_{sk(o)}$ (3)	TMDSn or xTMDSn	xTMDSn or TMDSn		0.06		ns
$t_{sk(p)}$ (4)				0.06	0.1	ns

(1) All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port to any other port
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$



This example circuit shows connecting control inputs to GPIOs of an application using V_{SS} = 1.5 V, which allows the device to pass TMDS signal levels

Figure 1. Example Voltage Divider Circuit

TYPICAL CHARACTERISTICS

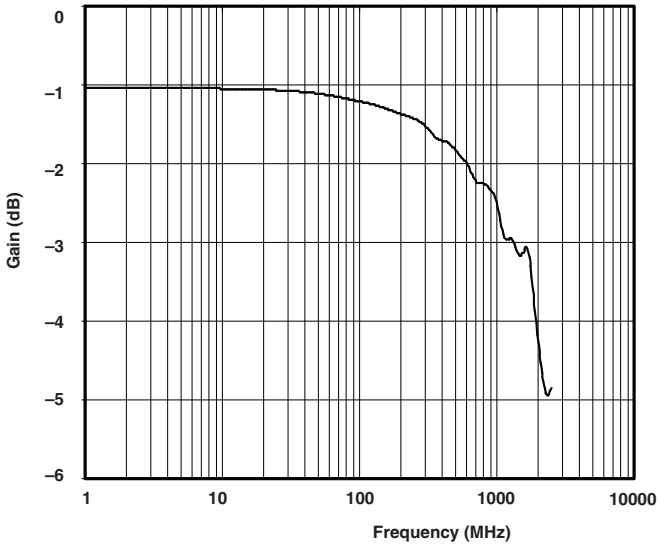


Figure 2. Insertion Loss

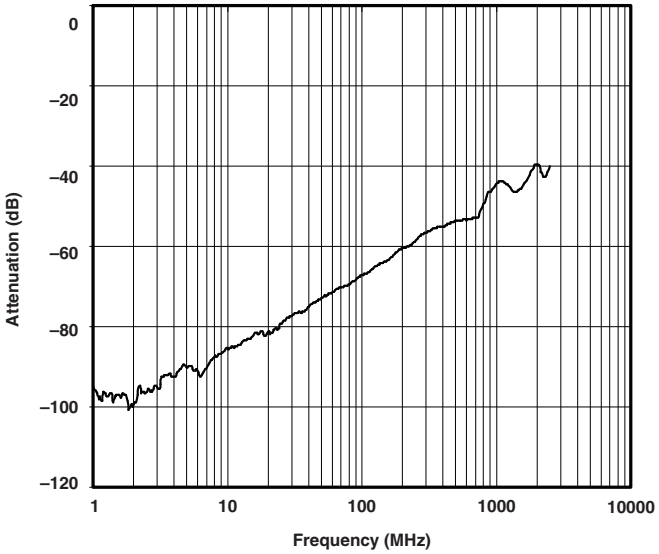


Figure 3. Crosstalk

TYPICAL CHARACTERISTICS (continued)

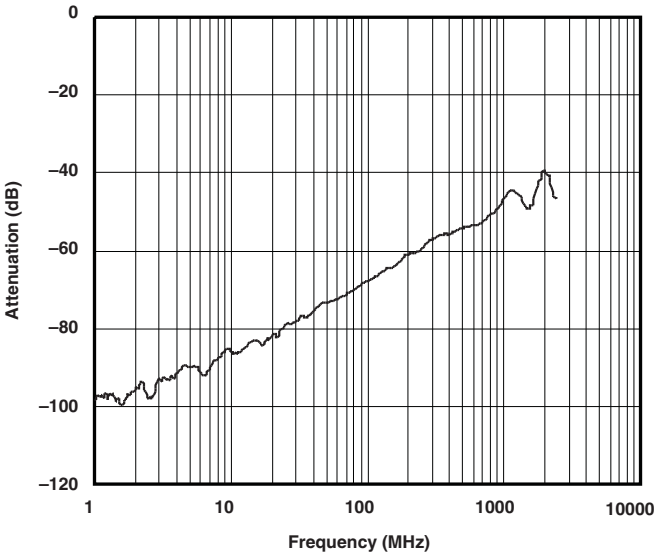


Figure 4. Off Isolation vs Frequency

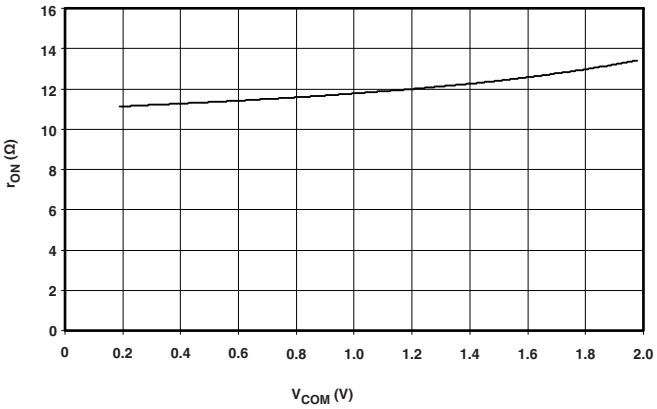


Figure 5. r_{ON} vs V_{COM}

PARAMETER MEASUREMENT INFORMATION

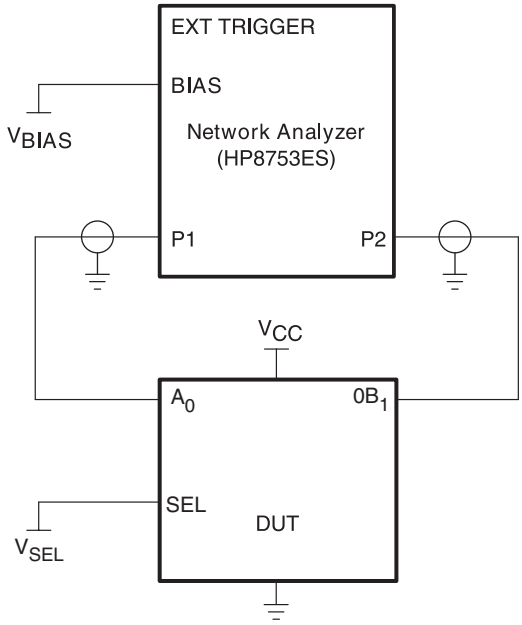


Figure 6. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

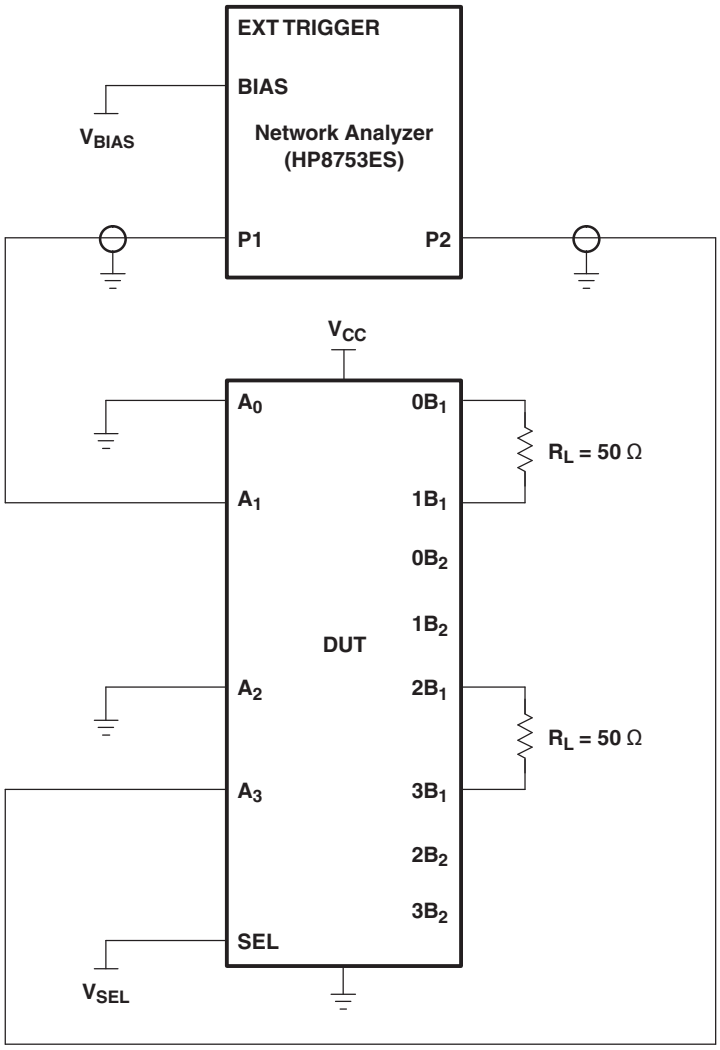


Figure 7. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $1B_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

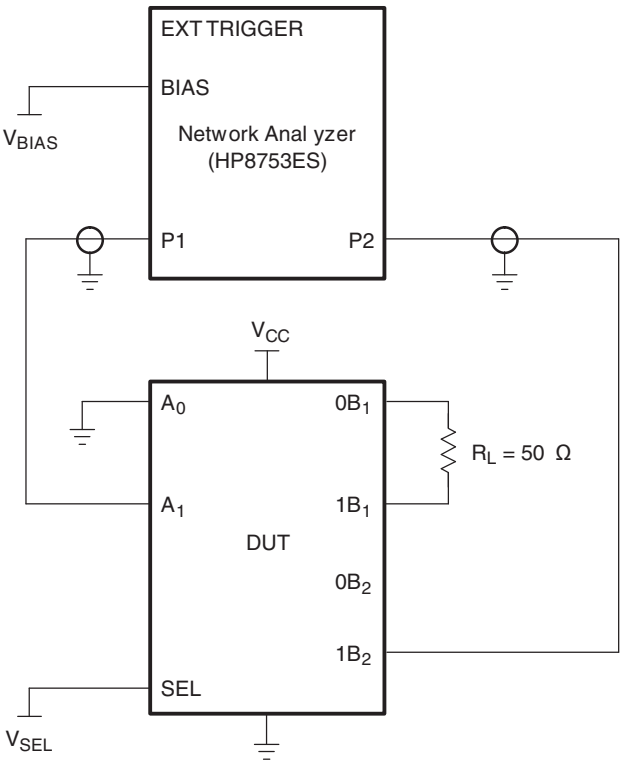


Figure 8. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $0B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2

P1 = 0 dBM

APPLICATION INFORMATION

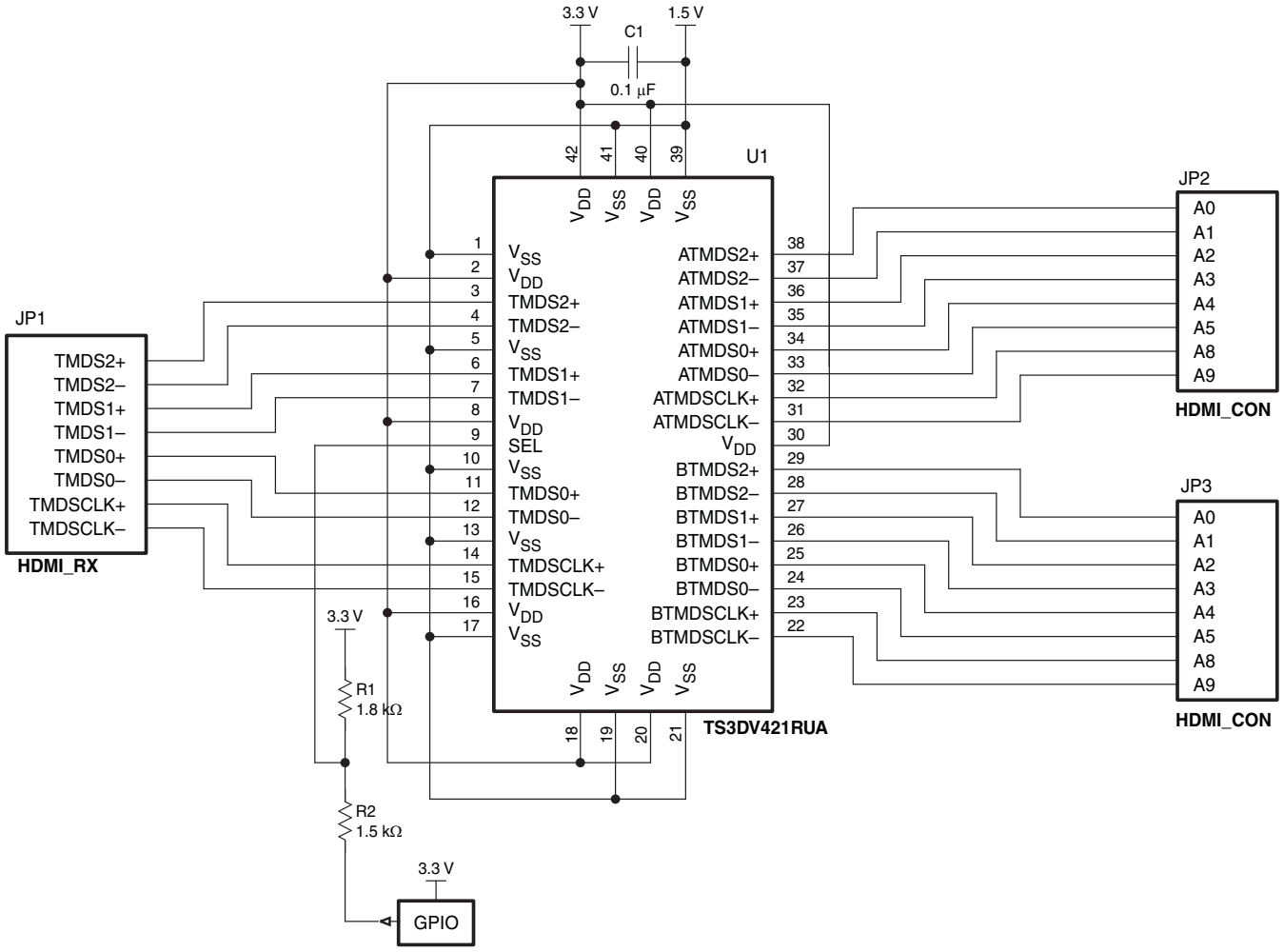


Figure 9. Reference Circuit for HDMI Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV421DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD421	Samples
TS3DV421RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	SD421	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

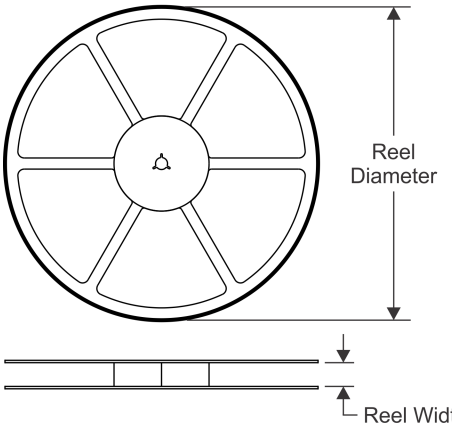
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

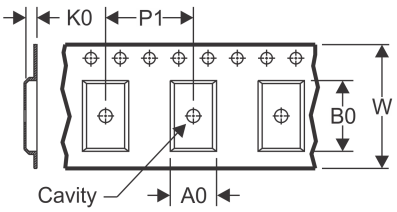
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

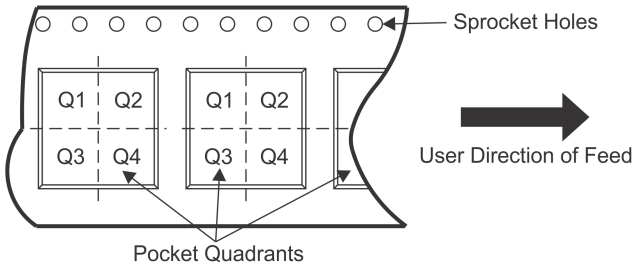


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

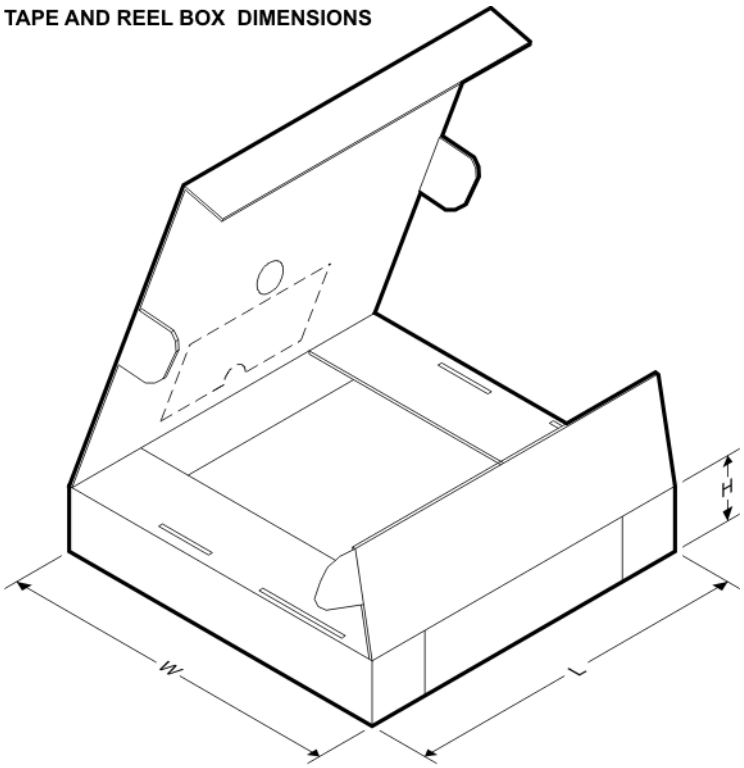
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV421DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
TS3DV421RUAR	WQFN	RUA	42	3000	330.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

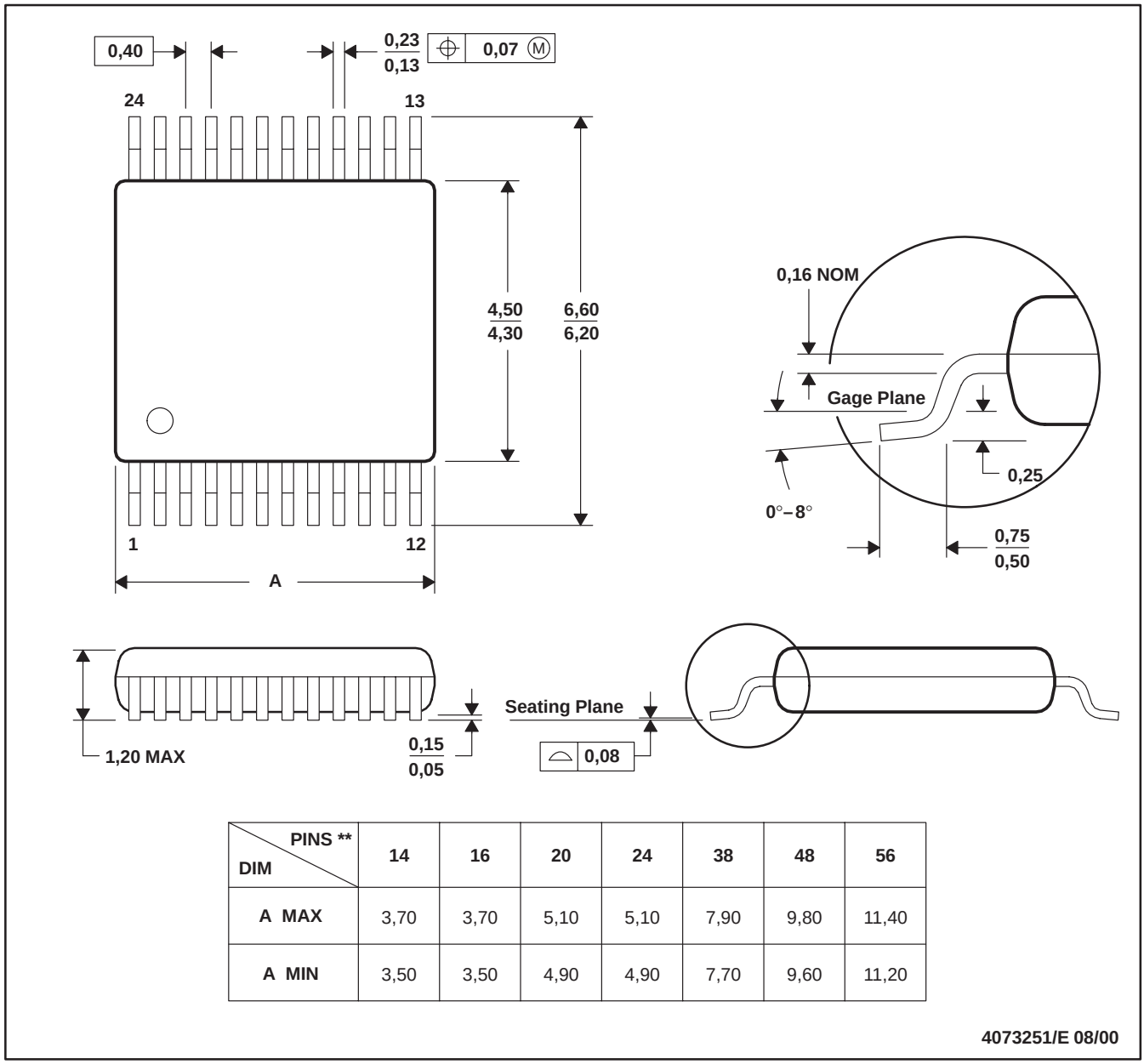


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV421DGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
TS3DV421RUAR	WQFN	RUA	42	3000	346.0	346.0	35.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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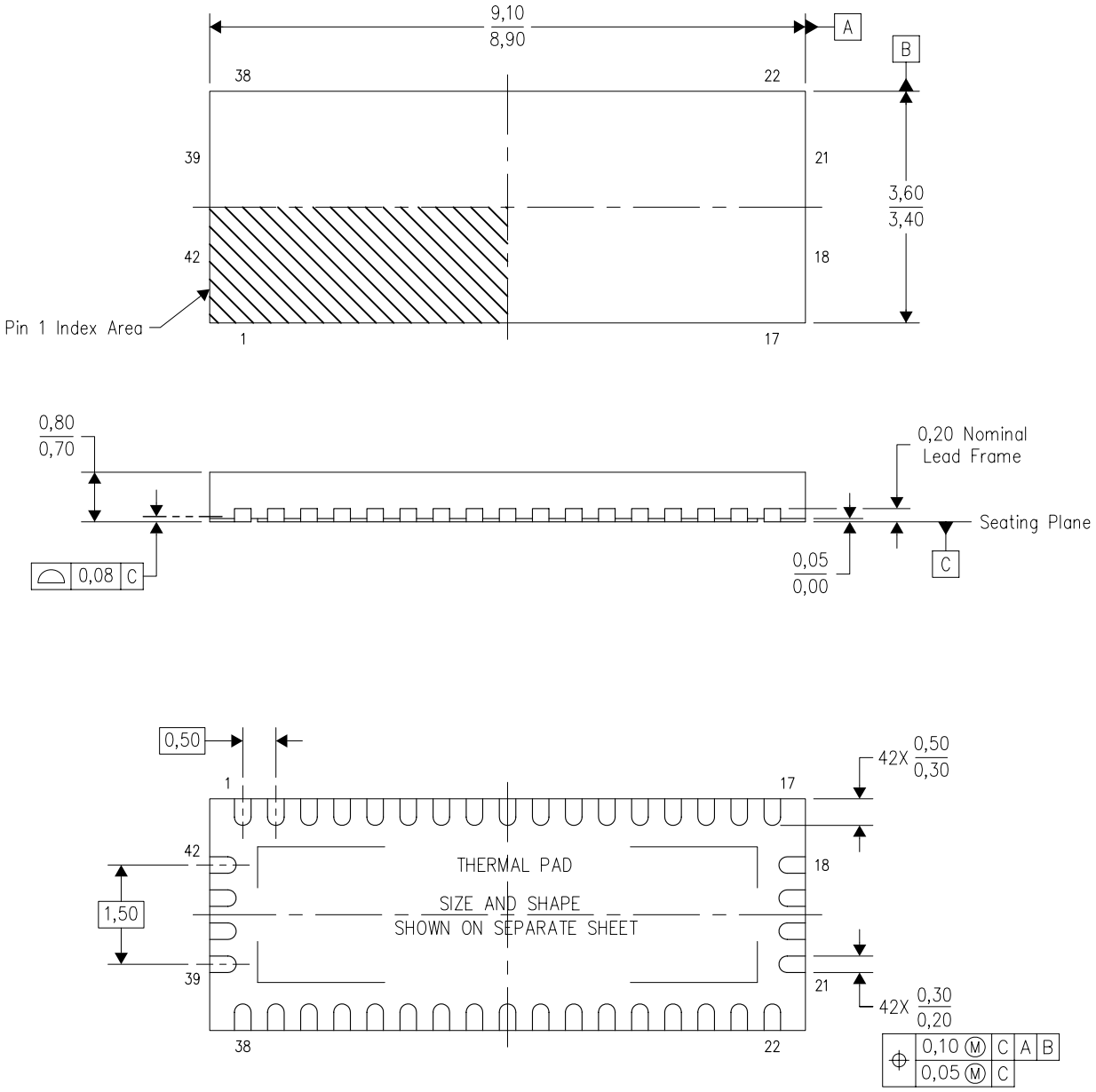
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

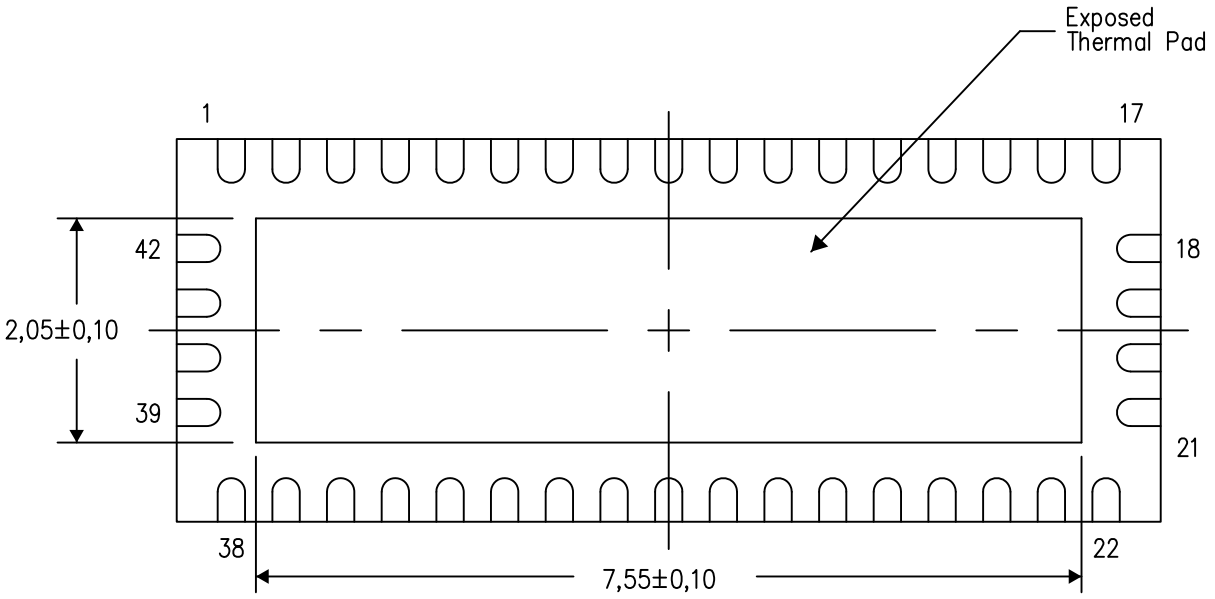
RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



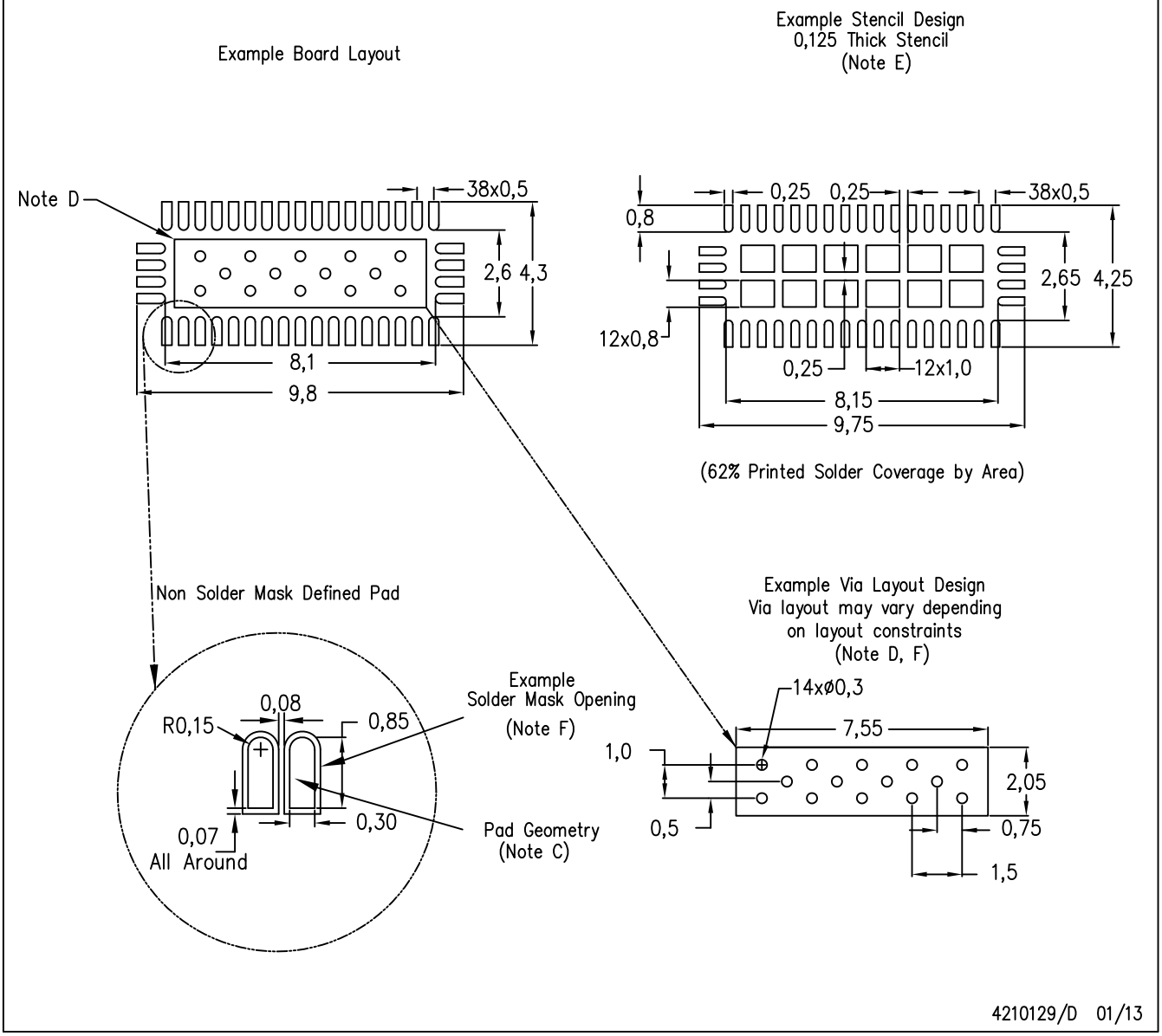
Bottom View

Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE: All linear dimensions are in millimeters

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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