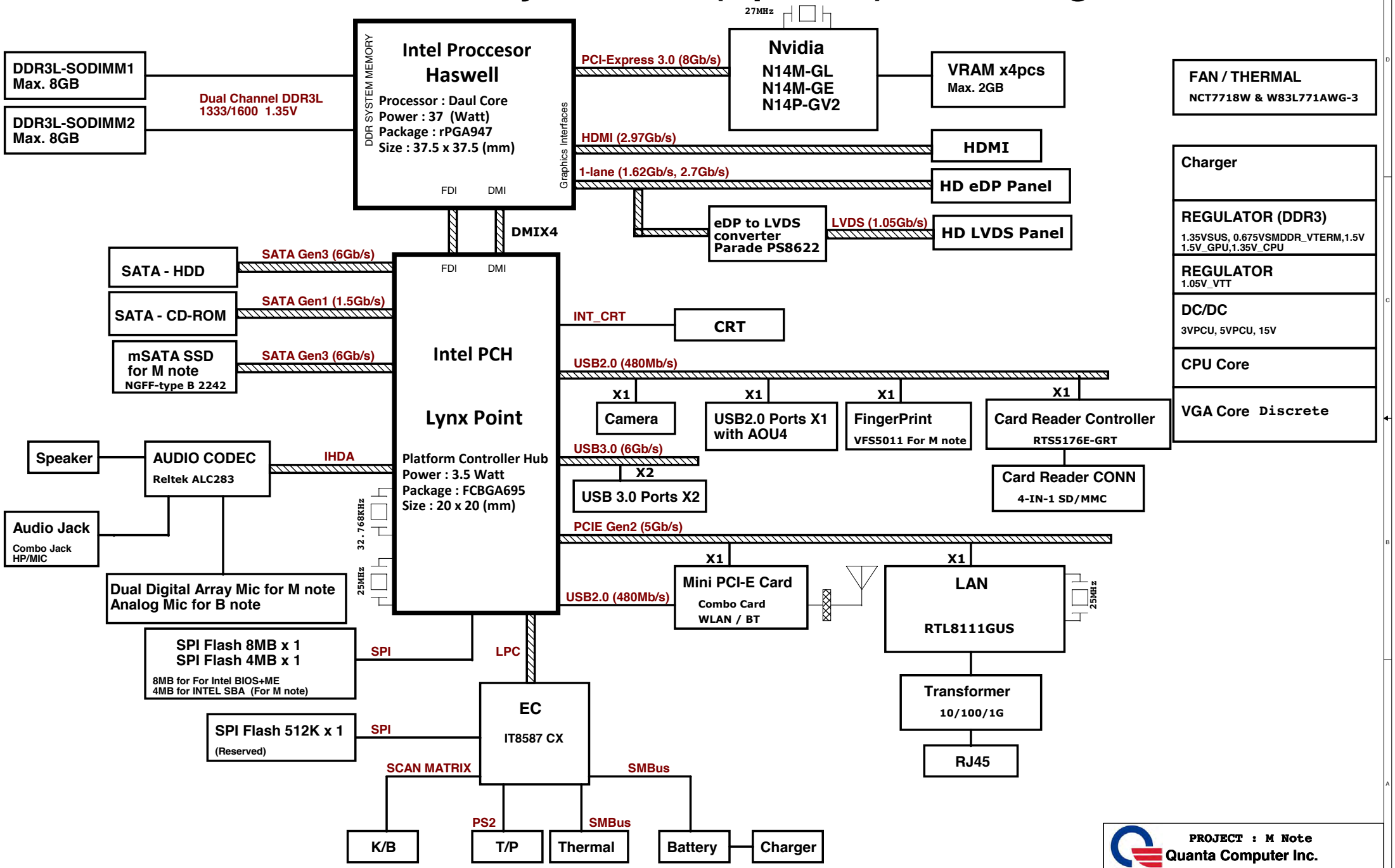
M/B Note Intel Shark Bay Platform (Optimus) Block Diagram



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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Haswell Processor (DMI,PEG,FDI)

Haswell Processor (CLK,MISC,JTAG)

02

+3V (6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

U21A

DMI_TXN0 (6) D21 DMI_RX#[0]
DMI_TXN1 (6) C21 DMI_RX#[1]
DMI_TXN2 (6) B21 DMI_RX#[2]
DMI_TXN3 (6) A21 DMI_RX#[3]

DMI_TXP0 (6) D20 DMI_RX[0]
DMI_TXP1 (6) C20 DMI_RX[1]
DMI_TXP2 (6) B20 DMI_RX[2]
DMI_TXP3 (6) A20 DMI_RX[3]

DMI_RXN0 (6) D18 DMI_TX#[0]
DMI_RXN1 (6) C17 DMI_TX#[1]
DMI_RXN2 (6) B17 DMI_TX#[2]
DMI_RXN3 (6) A17 DMI_TX#[3]

DMI_RXP0 (6) D17 DMI_TX[0]
DMI_RXP1 (6) C18 DMI_TX[1]
DMI_RXP2 (6) B18 DMI_TX[2]
DMI_RXP3 (6) A18 DMI_TX[3]

DMI

FDI_TXN0 (6) P33 FDI_TX#[0]
FDI_TXN1 (6) N32 FDI_TX#[1]
FDI_TXP0 (6) R33 FDI_TX[0]
FDI_TXP1 (6) P32 FDI_TX[1]

FDI_INT (6) J29 FDI_INT
FDI_CSYNC (6) H29 FDI_CSYNC
R427 *0_4S

FDI

IN_D2# (22) T28 DDIB_TX#[0]
IN_D1# (22) T30 DDIB_TX#[1]
IN_D0# (22) U29 DDIB_TX#[2]
IN_CLK# (22) U31 DDIB_TX#[3]
IN_D2 (22) U28 DDIB_TX[0]
IN_D1 (22) U30 DDIB_TX[1]
IN_D0 (22) V29 DDIB_TX[2]
IN_CLK (22) V31 DDIB_TX[3]

Intel(R) DDI

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

DP Port for Docking

ExDPP0_N (37) P29 DDID_TX#[0]
ExDPP1_N (37) N28 DDID_TX#[1]
P31 DDID_TX#[2]
N30 DDID_TX#[3]
ExDPP0_P (37) R29 DDID_TX[0]
ExDPP1_P (37) P28 DDID_TX[1]
R31 DDID_TX[2]
P30 DDID_TX[3]

eDP_RCOMP E24
EDP_DISP_UTIL (6,19) R72 *0_4 INT_eDP_HPD_Q R27 eDP_HPD
EDP_AUXP (19) N27 eDP_AUX
EDP_AUXN (19) M27 eDP_AUX#
EDP_TXP0 (19) R35 eDP_TX[0]
EDP_TXN0 (19) P35 eDP_TX[1]
P34
N34 eDP_TX#[0]
eDP_TX#[1]

eDP

HSW_RPGA_EDS_PGA

PCI EXPRESS* - GRAPHICS

PEG_COMP
PEG_RCOMPO E23

PEG_RX#[0] M29 PEG_RXN0
PEG_RX#[1] K28 PEG_RXN1
PEG_RX#[2] M31 PEG_RXN2
PEG_RX#[3] L30 PEG_RXN3
PEG_RX#[4] M33 PEG_RXN4
PEG_RX#[5] L32 PEG_RXN5
PEG_RX#[6] M35 PEG_RXN6
PEG_RX#[7] L34 PEG_RXN7
PEG_RX#[8] E29
PEG_RX#[9] D28
PEG_RX#[10] E31
PEG_RX#[11] D30
PEG_RX#[12] E35
PEG_RX#[13] D34
PEG_RX#[14] E33
PEG_RX#[15] E32

PEG_RXN[0..7] (14)

PEG_RX[0] L29 PEG_RXP0
PEG_RX[1] L28 PEG_RXP1
PEG_RX[2] L31 PEG_RXP2
PEG_RX[3] K30 PEG_RXP3
PEG_RX[4] L33 PEG_RXP4
PEG_RX[5] K32 PEG_RXP5
PEG_RX[6] L35 PEG_RXP6
PEG_RX[7] K34 PEG_RXP7
PEG_RX[8] F29
PEG_RX[9] E28
PEG_RX[10] F31
PEG_RX[11] E30
PEG_RX[12] F35
PEG_RX[13] E34
PEG_RX[14] F33
PEG_RX[15] D32

PEG_RXP[0..7] (14)

PEG_TX#[0] H35 C_PEG_TX#0
PEG_TX#[1] H34 C_PEG_TX#1
PEG_TX#[2] J33 C_PEG_TX#2
PEG_TX#[3] H32 C_PEG_TX#3
PEG_TX#[4] J31 C_PEG_TX#4
PEG_TX#[5] G30 C_PEG_TX#5
PEG_TX#[6] C33 C_PEG_TX#6
PEG_TX#[7] B32 C_PEG_TX#7
PEG_TX#[8] B31
PEG_TX#[9] A30
PEG_TX#[10] B29
PEG_TX#[11] A28
PEG_TX#[12] B27
PEG_TX#[13] A26
PEG_TX#[14] B25
PEG_TX#[15] A24

PEG_TX[0] J35 C_PEG_TX0
PEG_TX[1] G34 C_PEG_TX1
PEG_TX[2] H33 C_PEG_TX2
PEG_TX[3] G32 C_PEG_TX3
PEG_TX[4] H31 C_PEG_TX4
PEG_TX[5] H30 C_PEG_TX5
PEG_TX[6] B33 C_PEG_TX6
PEG_TX[7] A32 C_PEG_TX7
PEG_TX[8] C31
PEG_TX[9] B30
PEG_TX[10] C29
PEG_TX[11] B28
PEG_TX[12] C27
PEG_TX[13] B26
PEG_TX[14] C25
PEG_TX[15] B24

(41) DDR_VR_PWRGD

H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

TP61 SKTOCC# AP32
TP60 TP_CATERR# AN32

HPECI Ra,Ca need placement close to EC.
Ra
(9,32) EC_PECI R476 43_4 H_PECI
Ca
C555 *47P/50V_4

4/30 CRB 1.0 Add
+VCCST AK31

PROCHOT# (50ohm)
Trace Length <11 inches
(32,39,42) H_PROCHOT# R142 56.2/F_4 H_PROCHOT#_R AM30
C254 Cb need placment near VR
Cb
47P/50V_4

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
(9) PM_THRMTRIP#R PM_THRMTRIP#_R AM35

Rb need placment near PCH
4/30 CRB 1.0 Add
+1.05V R145 *1K_4 Rb

PM_SYNC (50ohm) (6) PM_SYNC R483 *0_4S PM_SYNC_R AT28
Trace Length: 1~11.25 inches
C203 *0.1U/10V_4

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
(9) H_PWRGOOD R117 *0_4/S H_PWRGOOD_R AL34
R114 10K_4

PM_DRAM_PWRGD_R AC10

CPU RESET#

(9) CPU_PLTRST#R
(8,14,23,27,28,30,34) PLTRST# R150 *750/F_4 CPU_PLTRST#R AT26

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

C249 *330P/50V_4
R141 *1.5K/F_4

U21B

SKTOCC# MISC
CATERR#
PECI
FC_AK31
PROCHOT#
THERMTRIP#
THERMAL
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
PWR MANAGEMENT
RESET#

HSW_RPGA_EDS_PGA

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

CLOCKS

BCLK E26 CLK_CPU_BCLKP → CLK_CPU_BCLKP (8)
BCLK# D26 CLK_CPU_BCLKN → CLK_CPU_BCLKN (8)
SSC_DPLL_REF_CLK E27 CLK_DPLL_SSCLKP → CLK_DPLL_SSCLKP (8)
SSC_DPLL_REF_CLK# F27 CLK_DPLL_SSCLKN → CLK_DPLL_SSCLKN (8)
DPLL_REF_CLK H28 CLK_DPLL_NSCCLKP → CLK_DPLL_NSCCLKP (8)
DPLL_REF_CLK# G28 CLK_DPLL_NSCCLKN → CLK_DPLL_NSCCLKN (8)

DDR3 MISC

SM_DRAMRST# AN3 CPU_DRAMRST#

SM_RCOMP[0] AP3 SM_RCOMP_0 R113 100/F_4
SM_RCOMP[1] AR3 SM_RCOMP_1 R153 75/F_4
SM_RCOMP[2] AP2 SM_RCOMP_2 R158 100/F_4

SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,

JTAG & BPM

CPU XDP

PRDY# AR29 XDP_PRDY# TP22
PREQ# AT29 XDP_PREQ# TP67
TCK AM34 XDP_TCLK TP11
TMS AN33 XDP_TMS TP15
TRST# AM33 XDP_TRST# TP12
TDI AM31 XDP_TDI_R TP18
TDO AL33 XDP_TDO TP14
DBR# AP33 XDP_DBRST# XDP_DBRST# (6)
R462 *1K_4 +3V

BPM#[0] AR30 XDP_BPM0 TP24
BPM#[1] AN31 XDP_BPM1 TP62
BPM#[2] AN29 XDP_BPM2 TP23
BPM#[3] AP31 XDP_BPM3 TP13
BPM#[4] AP30 XDP_BPM4 TP16
BPM#[5] AN28 XDP_BPM5 TP20
BPM#[6] AP29 XDP_BPM6 TP19
BPM#[7] AP28 XDP_BPM7 TP25

SM_DRAMPWROK Processor Input.

To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

+3VS5
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
R146 100K_4
R138 100K_4
C255 0.1U/10V_4
+1.35VSUS
DG 498556 -> 1.8K
R143 1.8K/F_4
U8
R135 *0_4S
74AHC1G09GW
PM_DRAM_PWRGD_C
R136 *0_4S PM_DRAM_PWRGD_R
R148 *0_4
PM_DRAM_PWRGD (6)
C260 0.047U/10V_4
D16 *RB500V-40
R154 3.3K_4
C259 *0.047U/10V_4
DG 498556 -> 3.3K
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches

DDR3 DRAM RESET

DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches

+1.35VSUS R144 *1K_4
(12,13) DDR3_DRAMRST# R149 *0_4S CPU_DRAMRST#
C256 *0.1U/10V_4

+3VS5 (6,7,9,10,15,17,20,23,24,25,28,32,37,40,44,47,53)
+1.35VSUS (4,12,13,38,41,49)
+1.05V (4,9,10,35,43,48,49,53)
+VCCIO_OUT (4,42)
+VCCIOA_OUT (4)

4/30 CRB V1.0 -> 10K

+VCCIO_OUT
R101 10K_4
INT_eDP_HPD_Q
Q25 2N7002BK
R63 100K_4
EDP_HPD (19)

PEG x8 disable (UMA only remove)

(14) PEG_TXP[0..7]

C_PEG_TX0 C458 0.22U/10V_4 PEG_TXP0
C_PEG_TX1 C460 0.22U/10V_4 PEG_TXP1
C_PEG_TX2 C462 0.22U/10V_4 PEG_TXP2
C_PEG_TX3 C464 0.22U/10V_4 PEG_TXP3
C_PEG_TX4 C466 0.22U/10V_4 PEG_TXP4
C_PEG_TX5 C468 0.22U/10V_4 PEG_TXP5
C_PEG_TX6 C472 0.22U/10V_4 PEG_TXP6
C_PEG_TX7 C477 0.22U/10V_4 PEG_TXP7

0.22uF AC coupling Caps for PCIE GEN1/2/3

(14) PEG_TXN[0..7]

C_PEG_TX#0 C459 0.22U/10V_4 PEG_TXN0
C_PEG_TX#1 C461 0.22U/10V_4 PEG_TXN1
C_PEG_TX#2 C463 0.22U/10V_4 PEG_TXN2
C_PEG_TX#3 C465 0.22U/10V_4 PEG_TXN3
C_PEG_TX#4 C467 0.22U/10V_4 PEG_TXN4
C_PEG_TX#5 C470 0.22U/10V_4 PEG_TXN5
C_PEG_TX#6 C476 0.22U/10V_4 PEG_TXN6
C_PEG_TX#7 C480 0.22U/10V_4 PEG_TXN7

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

+VCCIOA_OUT R37 24.9/F_4 eDP_RCOMP

eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

+VCCIOA_OUT R42 24.9/F_4 PEG_COMP

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Processor pull-up (CPU)

H_PROCHOT# R152 62_4 +VCCIO_OUT
CLK_DPLL_SSCLKP R34 *10K_4
CLK_DPLL_SSCLKN R35 *10K_4

XDP_TDO R128 51_4 +1.05V
XDP_TMS R131 *51_4
XDP_TDI_R R133 *51_4
XDP_PREQ# R485 *51_4
XDP_TCLK R119 51_4
XDP_TRST# R122 51_4

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HAS 1/4 (PCIE&DMI&FDI)	1A

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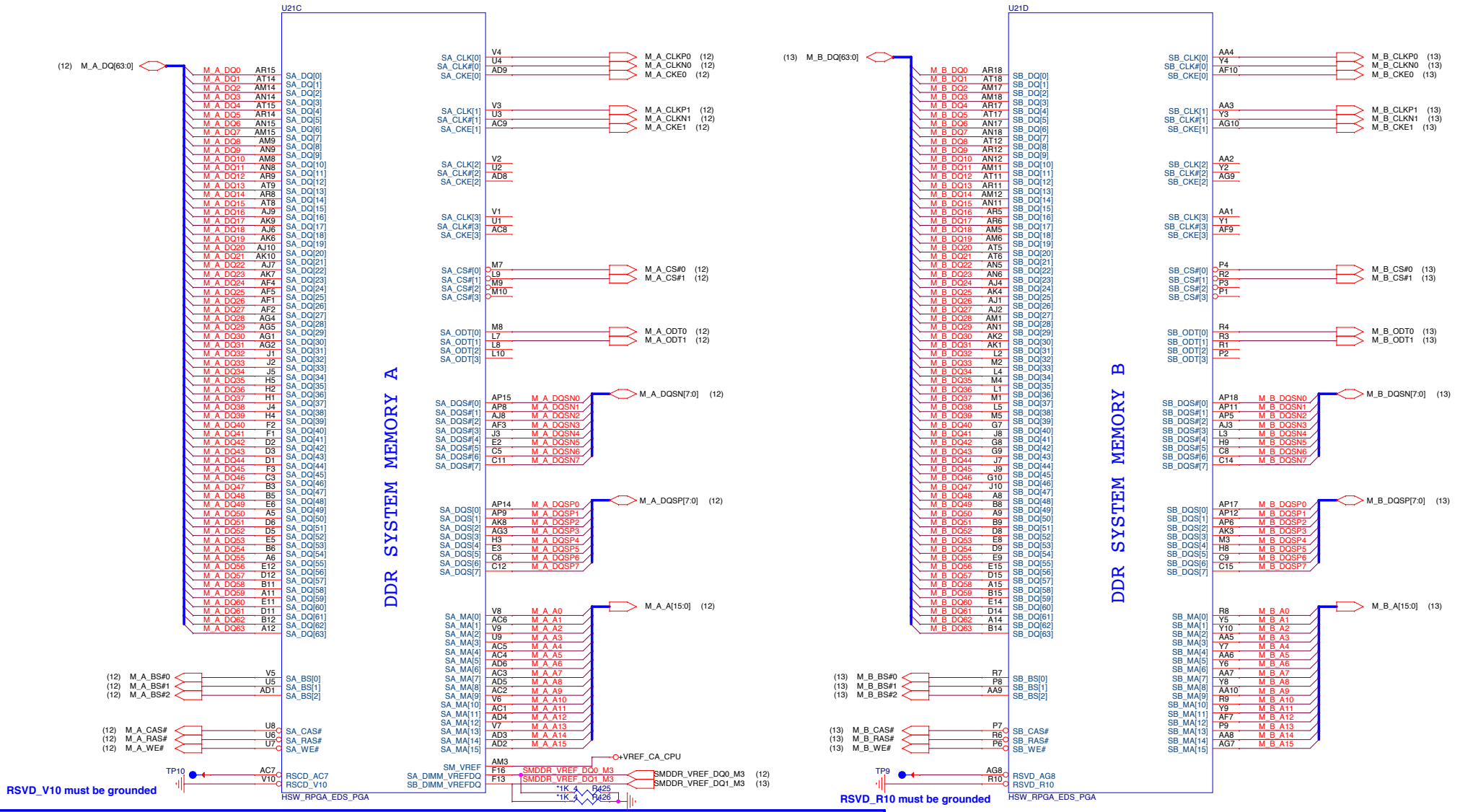
Haswell Processor (DDR3)



CPU SM_VREF

PROJECT :	M Note
Quanta Computer Inc.	
Size: Custom	Document Number: HAS 2/4 (DDR3 I/F) Rev: 1A
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Haswell Processor (POWER)

04

POWER

+VCCIN 95A

+VCC_CORE

U21F

+1.35VSUS 4.2A

180mil

+1.35VSUS

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

HSW_RPGA_EDS_PGA

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

CPU rPGA Socket P/N

Vender	Used	P/N
LTS	V	DGG^7000001
FOX		DGG^9000058

+1.35VSUS (2,12,13,38,41,49)
+VCC_CORE (42,49)
+1.05V (2,9,10,35,43,48,49,53)
+VCCIO_OUT (2,42)
+VCCIO_PCH (10)
+VCCIOA_OUT (2)

CRB 1.0 add

+1.05V R456 *0_8 +VCCST

C547 *22U/6.3VS_8 C549 *22U/6.3VS_8

Power Test Propose

+1.05V R41 150/F_4 PWR_DEBUG_R R40 *10K_4

+1.05V R503 *0_8 +VCCIO_OUT C558 *4.7U/6.3V_6

+1.05V R422 *0_6S +VCCIO_PCH C457 *4.7U/6.3V_6 CRB 1.0 stuff

DG 498550

Haswell PWR_DEBUG requires a 150-Ohm pull-up resistor to PCH 1.05-V VCC Core when routed to XDP

CPU VDDQ

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

SVID CLK

VR_SVID_CLK — VR_SVID_CLK (42)

SVID DATA

+VCCIO_OUT R140 130/F_4

Place PU resistor close to CPU

VR_SVID_DATA — VR_SVID_DATA (42)

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

SVID ALERT

+VCCIO_OUT C559 0.1U/10V_4 R147 75/F_4 H_CPU_SVIDALRT# R139 43_4 VR_SVID_ALERT# (42)

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

PROJECT : M Note

Quanta Computer Inc.

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Custom	HAS 3/4 (POWER)	1A

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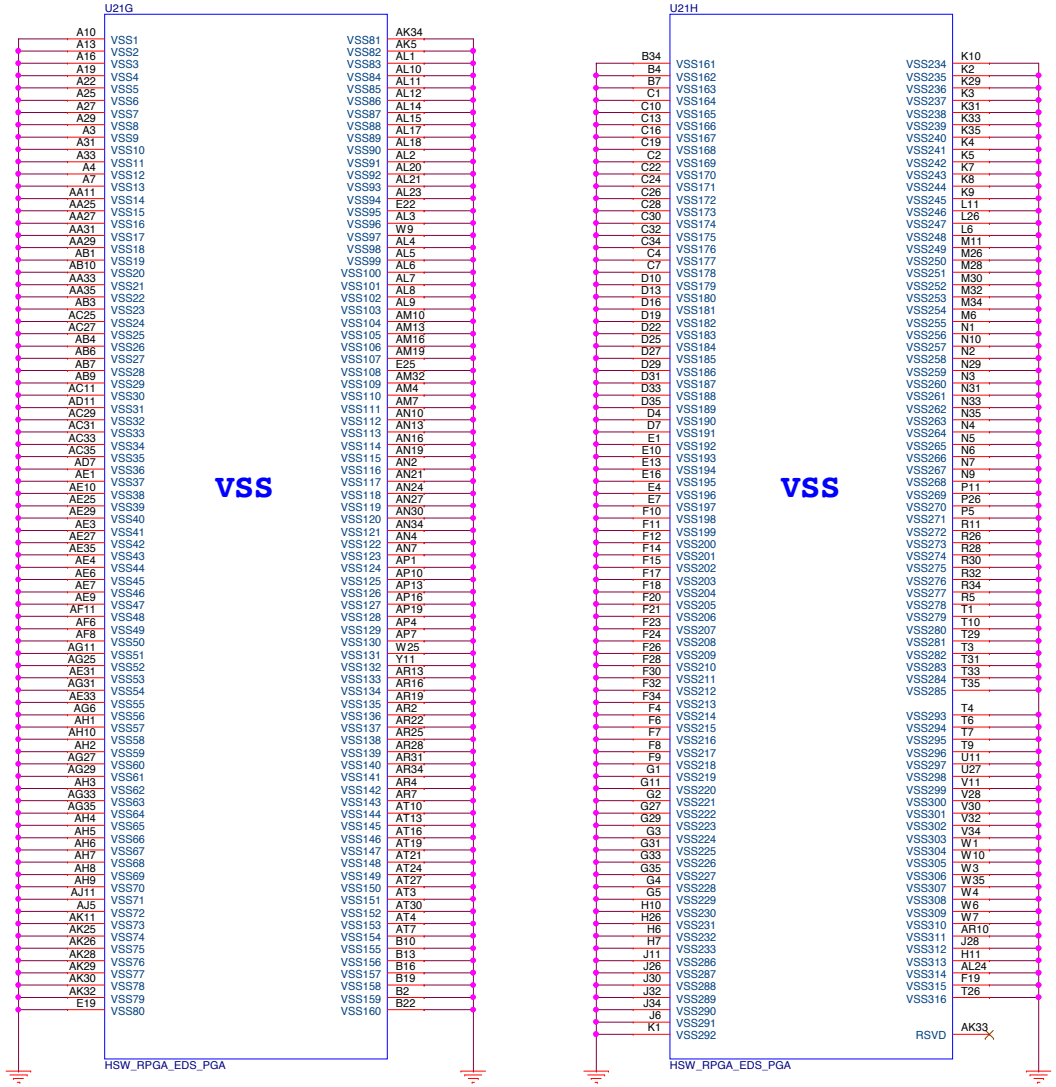
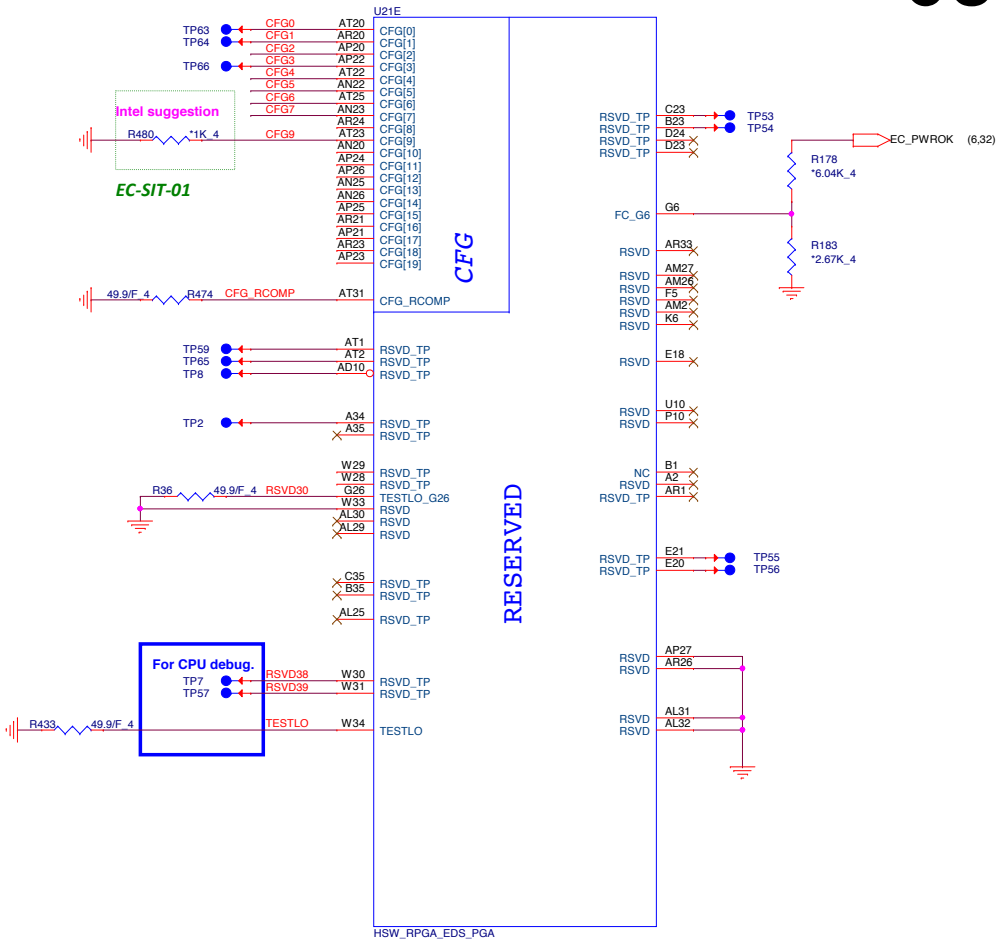
Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG3 R481 *1K_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG2 R468 *1K_4
CFG4 R482 1K_4
CFG7 R478 *1K_4
CFG5 R479 1K_4
CFG6 R477 *1K_4

PROJECT : M Note
Quanta Computer Inc.

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05

Lynx Point (DMI,FDI,PM)

U40C

+3V_RTC (7,10,24,32,35)
+3VS5 (2,7,9,10,15,17,20,23,24,25,28,32,37,40,44,47,53)
+3V_DEEP_SUS (7,8,9,10,53)
+3V (2,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)
+1.5V (7,8,10,19,24,28,46,48,49)

DMI0RXN DMI1RXN DMI2RXN DMI3RXN
DMI0RXP DMI1RXP DMI2RXP DMI3RXP
DMI0TXN DMI1TXN DMI2TXN DMI3TXN
DMI0TXP DMI1TXP DMI2TXP DMI3TXP
DMI_IREF DMI_IRCOMP

DMI

FDI_RXN0 FDI_RXN1 FDI_RXP0 FDI_RXP1
FDI_TXN0 FDI_TXN1 FDI_TXP0 FDI_TXP1
FDI_CSYNC
FDI_INT
FDI_IREF R620 *0_4S +1.5V
FDI_RCOMP R625 7.5K/F_4

FDI

RSMRST# C586 *0.1U/10V_4

EC-SIT-14

+1.5V R646 *0_4S DMI_IREF
R645 7.5K/F_4 DMI_COMP

TP12 TP7

for DS3
SUSWARN# *0_4 R243
(32) SUSACK#EC *0_4S R250 SUSACK#

(2) XDP_DBRST#
SYS_PWROK R281 *0_4S SYS_PWROK_R
EC-DV-04 EC_PWROK_R
(53) APWROK R201 0_4 APWROK_R
(2) PM_DRAM_PWRGD
(32) RSMRST#

for DS3
(32) SUSWARN#EC R564 *0_4S SUSWARN#
(32) SIO_PWRBTN# R569 *0_4S DNBSWON#_R
for DS3
(17,32) AC_PRESENT R202 *0_4S AC_PRESENT_R

PM_BATLOW# RI#
TP40 TP21

SYS_PWROK_R C318 *0.1U/10V_4
Reserve for power on sequence

System Power Management

SUSACK# SYS_RESET# SYS_PWROK PWROK APWROK DRAMPWROK RSMRST# SUSWARN#/SUSPWRDNACK/GPIO30 (SUS) PWRBTN# ACPRESENT / GPIO31(DSW) BATLOW# / GPIO72 (SUS) RI#

(+3VS5) (DSW)

DSWVRMEN DPWROK WAKE# CLKRUN# SUS_STAT# / GPIO61 (SUS) SUSCLK / GPIO62 (SUS) SLP_S5# / GPIO63 (SUS) SLP_S4# SLP_S3# SLP_A# SLP_SUS# PMSYNCH SLP_LAN# SLP_WLAN#/ GPIO29 (DSW)

(+3VS5) (DSW)

R214 330K_4 +3V_RTC
C8 DSWVREN
L13 DPWROK
R220 *0_4S for DS3 DPWROK_EC (32)
R204 *0_4 RSMRST#

K3 PCIE_WAKE# PCIE_WAKE# (23,28)
AN7 CLKRUN# CLKRUN# (32)
U7 SUS_STAT# SUS_STAT# (32)
Y6 PCH_SUSCLK_L PCH_SUSCLK_L (7)
Y7 R273 *0_4S SIO_SLP_S5# (32)
C6 R547 *0_4S SLP_S4# (32)
H1 R568 *0_4S SIO_SLP_S3# (32)
F3 R227 *0_4S PM_SLP_M# (32)
F1 R562 *0_4S SLP_SUS# (32)
AY3 PM_SYNC (2)
G5 SLP_LAN#
D2 WLAN_AOAC_ON WLAN_AOAC_ON (28)

5/16 for DS3

LPT_PCH_HM87_EDS/BGA

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance.

(31) CRT_B R266 150/F_4 T45 CRT_BLUE
(31) CRT_G R271 150/F_4 U44 CRT_GREEN
(31) CRT_R R274 150/F_4 V45 CRT_RED
(31) DDCCLK M43 CRT_DDC_CLK
(31) DDCDATA M45 CRT_DDC_DATA

DG V0.7 -> 33 ohm
SCH V0.7 -> 0 ohm
(31) HSYNC_COM R579 33_4 PCH_HSYNC_R N42 CRT_HSYNC
(31) VSYNC_COM R578 33_4 PCH_VSYNC_R N44 CRT_VSYNC

R269 649/F_4 DAC_IREF U40 DAC_IREF
U39 CRT_IRTN

DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS

Reserve from EMI request
CRT_B CRT_G CRT_R
EC6 *5.6P/16V_4 EC7 *5.6P/16V_4 EC8 *5.6P/16V_4

Lynx Point (DDI)

U40D

(19) INT_LVDS_BLON K36 EDP_BKLTEN
(19) INT_DISP_ON G36 EDP_VDD_EN
(2,19) INT_DPST_PWM N36 EDP_BKLTCTL

LVDS

CRT

Digital Display Interface

LPT_PCH_HM87_EDS/BGA

DDPB_CTRLCLK R40 SDVO_CLK (22)
DDPB_CTRLDATA R39 SDVO_DATA (22)
DDPB_AUXN H45 TP79
DDPB_AUXP H43 TP80
DDPB_HPD K40 HDMI_HPD_CON (22)

EC-DV-26

INT. HDMI

DDPC_CTRLCLK R35
DDPC_CTRLDATA R36
DDPC_AUXN K43
DDPC_AUXP K45
DDPC_HPD K38

EC-DV-26

DDPD_CTRLCLK N40
DDPD_CTRLDATA N38
R691 2.2K_4 TP81 TP82 +3V
DDPD_AUXN J42 ExDP_AUXN (37)
DDPD_AUXP J44 ExDP_AUXP (37)
DDPD_HPD H39 ExDP_HPD (37)

Cable Docking

PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)

PCH Pull-high/low(CLG)

+3V_DEEP_SUS for DS3

PM_RI# R572 10K_4
SLP_LAN# R549 10K_4
SUSACK# R247 *10K_4
SUSWARN# R565 *10K_4
PM_DRAM_PWRGD R560 *10K_4
SUS_STAT# R267 *10K_4
WLAN_AOAC_ON R198 10K_4
PM_BATLOW# R223 8.2K_4
PCIE_WAKE# R571 1K_4
DNBSWON#_R R566 10K_4
AC_PRESENT_R R188 10K_4 +3VS5
R192 *100K_4
DPWROK R213 100K/F_4
CLKRUN# R293 8.2K_4 +3V
XDP_DBRST# R615 1K_4
R614 *1K_4
RSMRST# R206 10K_4
SYS_PWROK_R R280 10K_4
EC_PWROK_R R686 10K_4

EDS V0.7 -> BATLOW# is in SUS well
SCH V0.7 -> BATLOW# pull up to DS3 power
Follow CRB @1224

DG V0.7 say that PWRBTN# is internal pulled-up in PCH to 3.3 V DSW through a weak pull-up resistor (24 kΩ nominal)

10/16 add

12/02 add

EC-DV-04

SBA Support

APWROK_R R191 *0/J_4 EC_PWROK_R

	R	Status
Non-SBA	R191/Stuff,R201/Un-Stuff	
SBA	R191/Un-Stuff,R201/Stuff	

PCH_PWROK_OK(CLG)

EC-DV-04

+3VS5 C643 0.1U/10V_4
EC_PWROK_R 4 U49 TC7SH08FU 5 2 1 3 IMVP_PWRGD HWPG (19,30,32,39,40,41,43,46)
IMVP_PWRGD R186 *0_4
EC_PWROK R187 *0_4 EC_PWROK_R

Follow Intel schematic review suggestion

System PWR_OK(CLG)

EC-DV-04

+3VS5 C274 *0.1U/10V_4
(41) SYS_PWROK SYS_PWROK 4 U36 *TC7SH08FU 5 2 1 3 IMVP_PWRGD IMVP_PWRGD (42)
EC_PWROK EC_PWROK (5,32)
R185 *0_4S TP26

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

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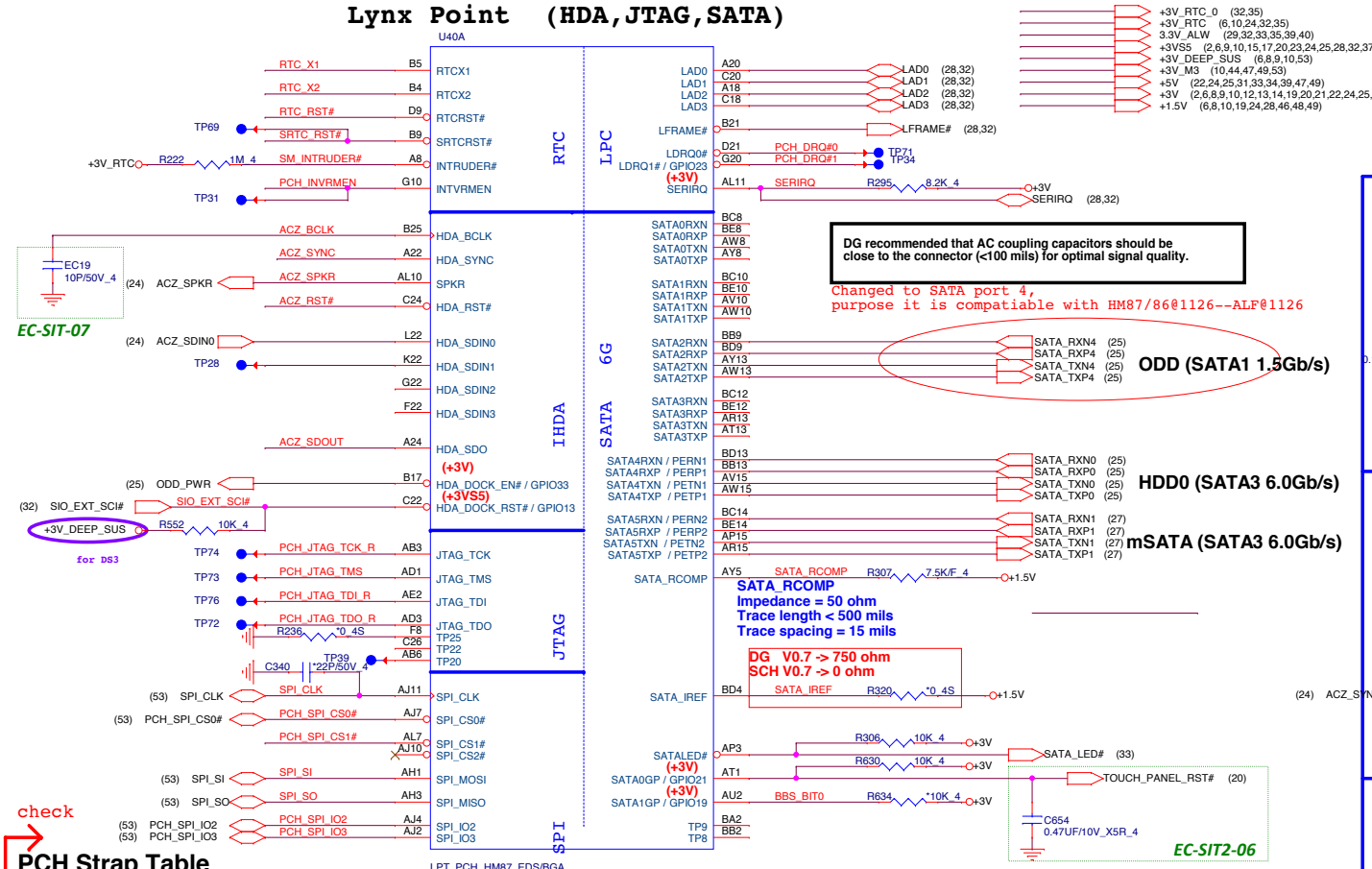
06

Lynx Point (HDA,JTAG,SATA)



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

Changed to SATA port 4, purpose it is compatiable with HM87/86@1126--ALF@1126

ODD (SATA1 1.5Gb/s)

HDD0 (SATA3 6.0Gb/s)

mSATA (SATA3 6.0Gb/s)

SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

DG V0.7 -> 750 ohm
SCH V0.7 -> 0 ohm

EC-SIT-07

check

PCH Strap Table

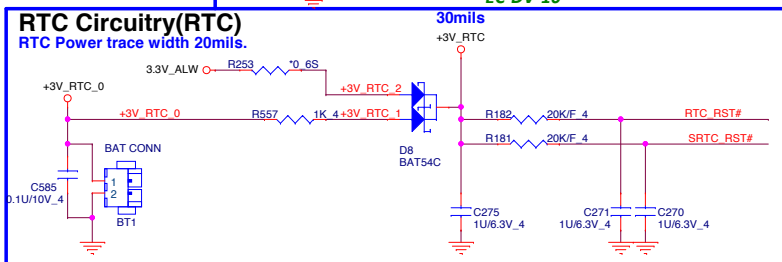
LPT_PCH_HM87_EDS/BGA

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R292 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R286 *1K_4 PCI_GNT3# (8)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R240 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# R633 *1K_4 BBS_BIT0 R550 *1K_4 BBS_BIT1 (8)
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R539 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	ACZ_SDOUT R551 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R583 *1K_4 BT_OFF# (9,28)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R577 *1K_4 PLL_ODVR_EN (9)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	SPI_SI R291 *1K_4 +3V
SUSCLK / GPIO62	On-die PLL Voltage Regulator	PWROK	0 = Disable 1 = Enable (Int PU)	(6) PCH_SUSCLK_L R256 *1K_4 R262 *1K_4 +3V

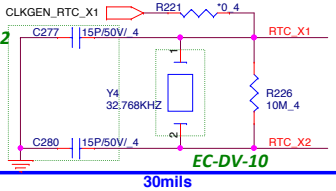
RTC Circuitry(RTC)

RTC Power trace width 20mils.

30mils

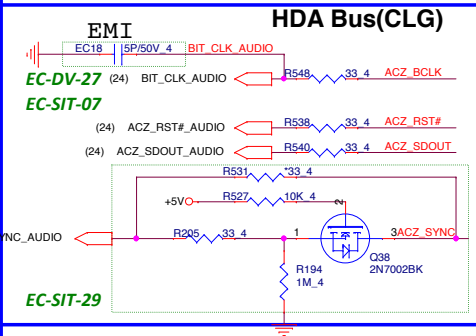


EC-DV-10



EC-SIT-32

HDA Bus(CLG)

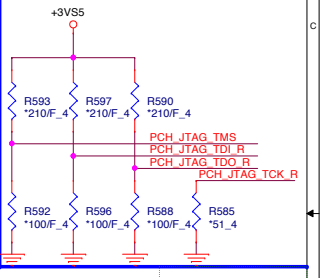


EC-DV-27

EC-SIT-07

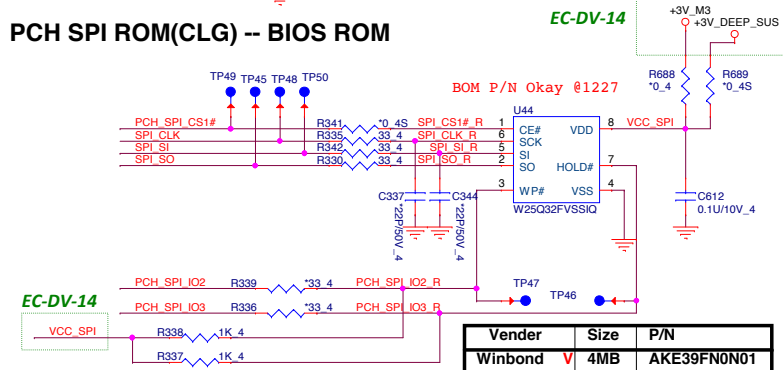
EC-SIT-29

PCH JTAG Debug(CLG)



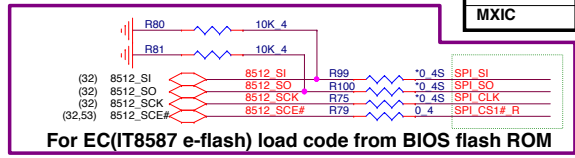
PCH SPI ROM(CLG) -- BIOS ROM

EC-DV-14



EC-DV-14

Vender	Size	P/N
Winbond V	4MB	AKE39FN0N01
MXIC	4MB	AKE39ZN0Z01



EC-DV-14

For EC(IT8587 e-flash) load code from BIOS flash ROM

BIOS = 4MB_CS1 ME = 8MB_CS0	R	Status
Un-SBA	R79	Un-Stuff
SBA	R79	Stuff

PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

GPIO50 DGPU_HOLD_RST#_R

PCIE Clock

SMBus/Pull-up(CLG)

Compatible with HM86

USB3.0 for Docking

Compatible with HM86

USB3.0

Right_USB

Left_USB_down EC-DV-11

Webcam

Fingerprint

Touch Screen (Option)

Cable Docking

Card Reader

Left_USB_up EC-DV-11

Bluetooth

Card reader changed to USB I/F

WLAN

LAN

GPU

check

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CRB 1.0 =>rename PCH_TP26

for DS3

EC-DV-03

SG : Rb ; UMA : Ra

Remove for UMA only.

CLOCK TERMINATION for FCIM

EC-SIT-28

EC-SIT-10

RF

EC-DV-28

EC-DV-28

New Adding @1219

PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A

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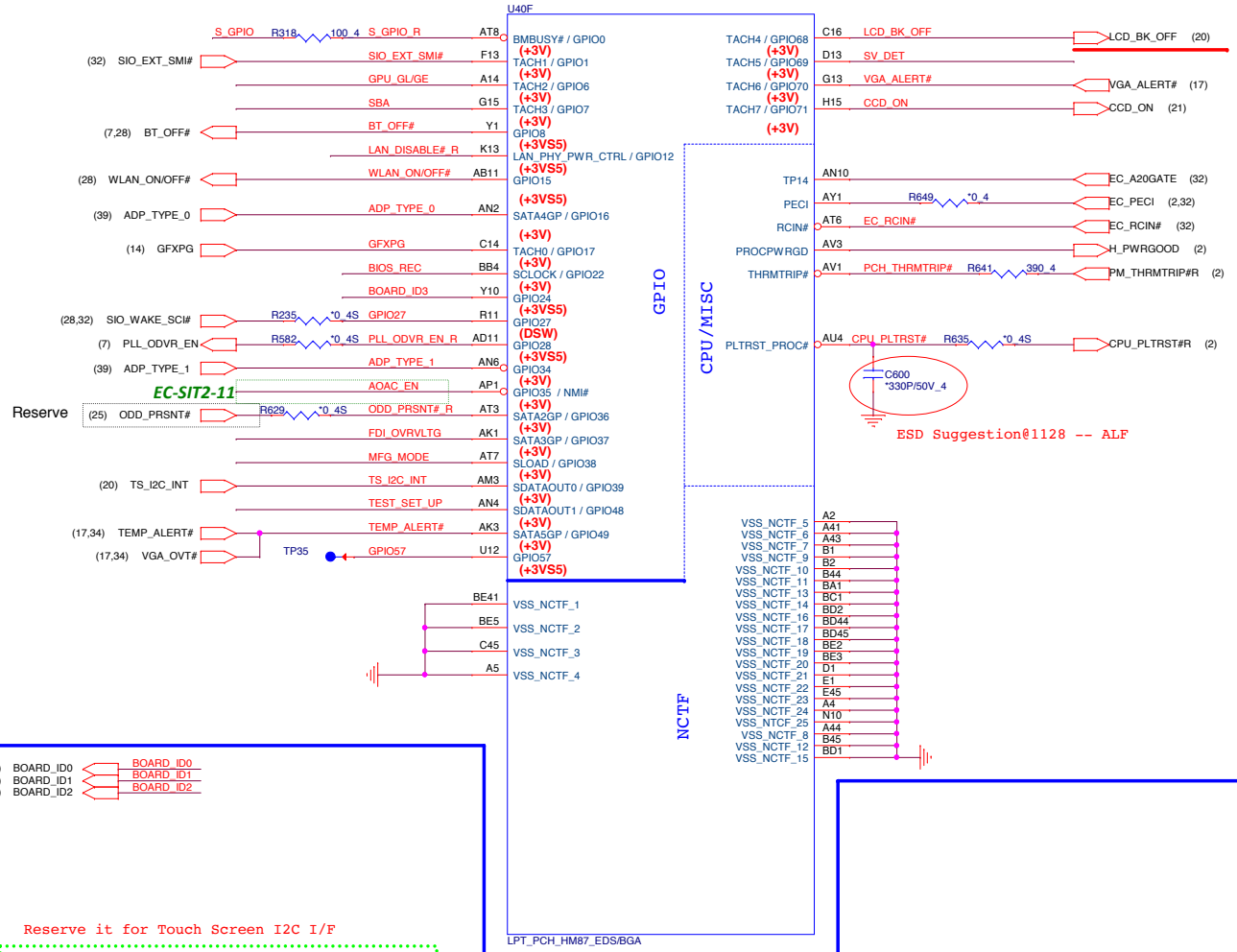
Lynx Point (GPIO,VSS_NCTF,RSVD)



Reserve

EC-SIT2-11

(28,32) SIO_WAKE_SCI# R235 *0_4S

(7) PLL_ODVR_EN R582 *0_4S

(25) ODD_PRSNT#

(39) ADP_TYPE_0

(39) ADP_TYPE_1

(14) GFXPG

(28) WLAN_ON/OFF#

(7,28) BT_OFF#

(32) SIO_EXT_SMI#

(20) TS_I2C_INT

(17,34) TEMP_ALERT#

(17,34) VGA_OVT# TP35

(8) BOARD_ID0
(8) BOARD_ID1
(8) BOARD_ID2

Reserve it for Touch Screen I2C I/F

R609 *10K_4 TS_I2C_INT R610 *10K_4 +3V
R219 *10K_4 CCD_ON R210 10K_4
R617 *10K_4 AOAC_EN R621 10K_4
R606 *10K_4 TEMP_ALERT# R607 10K_4
R532 *10K_4 LCD_BK_OFF R544 10K_4
R261 *10K_4 GPIO57 R255 *10K_4 +3V_DEEP_SUS

RD0 R586 *10K_4 BOARD_ID0 R589 10K_4 RU0
RD1 R283 *10K_4 BOARD_ID1 R284 10K_4 RU1
RD2 R575 10K_4 BOARD_ID2 R573 *10K_4 RU2
RD3 R278 *10K_4 BOARD_ID3 R275 10K_4 RU3

+3V_DEEP_SUS for DS3

EC-DV-35
EC-SIT-36
EC-SIT2-17

SharkBay BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO45	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO24	B = 0 / M = 1
SBA setting	GPIO6	
GPU GE/GL setting	GPIO7	GL=0 / GE=1
GPIO71	GPIO71	RESERVE
GPIO35	GPIO35	RESERVE
GPIO49	GPIO49	TEMP_ALERT#
GPIO68	GPIO68	RESERVE
GPIO69	GPIO69	RESERVE
GPIO39	GPIO39	RESERVE
GPIO70	GPIO70	RESERVE
AOAC_EN	GPIO35	for BM6/ AOAC Support AOAC=1/Non AOAC=0

BOARD_ID[3:0]	Model Name
	B Note
0000	A
0001	A2
0010	SIT
0011	SIT2
0100	
0101	
0110	
0111	
	M Note
1000	A
1001	A2
1010	SIT
1011	SIT2
1100	
1101	
1110	
1111	

+3VS5 (2,6,7,10,15,17,20,23,24,25,28,32,37,40,44,47,53)
+3V_DEEP_SUS (6,7,8,10,53)
+3V (2,6,7,8,10,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)
+1.05V (2,4,10,35,43,48,49,53)

PCH MISC PU /PD

EC_A20GATE R321 10K_4 +3V
EC_RCIN# R316 10K_4
PCH_THRMTRIP# R640 *1K_4 +1.05V

MFG-TEST

MFG_MODE R317 10K_4 +3V
R305 *0_4

Intel CRB

Swap GPIO

0 = SGPIO
1 = Default

S_GPIO R322 1K_4 +3V
R319 *0_4

Intel CRB for DS3

GPIO Pull-up/Pull-down(CLG) for DS3

+3V_DEEP_SUS

BT_OFF# R581 *10K_4

Reserve it for GPU's GPIO9 +3V

VGA_ALERT# R212 *10K_4
SIO_EXT_SMI# R196 10K_4
ADP_TYPE_0 R618 10K_4
ADP_TYPE_1 R300 10K_4
ODD_PRSNT#_R R627 10K_4
GFXPG R553 *10K_4

GFXPG R541 *10K_4 Rb

10/2 modify +3VS5
GPIO27 R234 10K_4
LAN_DISABLE#_R R239 10K_4

	Rb
UMA	Stuff
DIS	NC

+3V_DEEP_SUS
WLAN_ON/OFF# R580 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

R648 *0_4 BIOS_REC R647 10K_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

Intel CRB

BIOS_RESP

R626 *0_4 TEST_SET_UP R622 10K_4 +3V

SV_SET_UP
High = Strong (Default)

Intel CRB

SV Detect

0 = SV Detect
1 = Default

SV_DET
R554 *100K_4
R542 10K_4 +3V
EC-SIT-05

Intel CRB

B Note GPU GL/GE Select setting

	GL	GE
Stuff	Ra (Hi)	Rb (Lo)

Rb R533 10K_4 GPU_GL/GE R534 Ra *10K_4 +3V

SATA3GP/GPIO37 TLS Confidentiality PCH STRAPING

0 = TLS no confidentiality (Int PD)
1 = TLS with confidentiality

R601 *10K_4 FDI_OVRVLTG R602 1K_4 +3V

GPIO37	Low	N.A
	Hight	SBA

Intel CRB

GFX Present

Rb R567 *100K_4 DGPU_PRSNT# Ra R563 10K_4 +3V
DGPU_PRSNT# (8)

	DIS	UMA
Stuff	Ra	Rb
Level	Hi	Lo

for BM Note

SBA setting

	SBA	No-SBA
Stuff	Ra	Rb

Rb R209 *10K_4 SBA R218 10K_4 Ra +3V

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

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Lynx Point (POWER)

+3V_RTC (6,7,24,32,35)
+1.5V (6,7,8,19,24,28,46,48,49)
+1.05V (2,4,9,35,43,48,49,53)
+VCCIO_PCH (4)

+3VS5 (2,6,7,9,15,17,20,23,24,25,28,32,37,40,44,47,53)
+3V_DEEP_SUS (6,7,8,9,53)
+3V_M3 (7,44,47,49,53)
+3V (2,6,7,8,9,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

POWER

U40J

Clock and Miscellaneous

0.15A (20mils)
+1.05V, +VCCAXCK_VRM_R, +VCCAXCK_VRM
R639 *1/F_4, L31 *10uH/100MA_8, R631 *0_8S, C599 10U/6.3V_6
VCCVRM[5] ← AF34

+VCC_AXCK_DCB, +V1.05S_VCC_AXCK_DCB
R304 *0_6S, L11 *0_6S, C332 *10U/6.3V_6, C328 1U/6.3V_4
1.09A (40mils)
VCC[3] ← AP45

50mA (10mils)
+3V: R259 *0_4S, C289 1U/6.3V_4, +V3.3S_VCC_FLEX0 → M29 VCCCLK3_3[1]
+3V: R242 *0_4S, C288 1U/6.3V_4, +V3.3S_VCC_FLEX1 → L29 VCCCLK3_3[2]
+3V: R265 *0_4S, C298 1U/6.3V_4, +V3.3S_VCC_FLEX23 → L26 VCCCLK3_3[3]
M26 VCCCLK3_3[4]
+3V: R251 *0_4S, C296 1U/6.3V_4, +V3.3S_VCC_ASEPCI → U32 VCCCLK3_3[5]
V32 VCCCLK3_3[6]

+V1.05S_VCC_SSCFF
0.3A (20mils)
+1.05V: R277 *0_4S, C306 1U/6.3V_4 → Y32 VCCCLK[1]
+VCCCLKF135
+1.05V: R311 *0_4S, C333 1U/6.3V_4 → AD34 VCCCLK[2]
+V1.05S_VCC_SSCFF → AA30 VCCCLK[3], AA32 VCCCLK[4]
+V1.05S_VCCCLKF100
+1.05V: R287 *0_4S, C316 1U/6.3V_4 → AD35 VCCCLK[5]
+V1.05S_VCCSSCF100
+1.05V: R288 *0_4S, C320 1U/6.3V_4 → AG30 VCCCLK[6], AG32 VCCCLK[7]
+V1.05S_VCCCLKF100 → AD36 VCCCLK[8]
+V1.05S_VCCSSCF100 → AE30 VCCCLK[9], AE32 VCCCLK[10]

THERMAL

0.15A (20mils)
+1.5V: R309 *0_4S, +V1.5S_VCCATS → AW40 VCCVRM[6]
0.13A (20mils)
+3V: R312 *0_4S, +V3.3S_VCCPTS → AK30 VCC3_3[7], AK32 VCC3_3[8]
0.1U/10V_4 C324

CPU

+VCCIO_PCH: R340 *0_4S, +V1.05S_VCCPCPU
4mA (10mils)
C343 0.1U/10V_4, C342 0.1U/10V_4, C341 1U/6.3V_4
AJ12 V_PROC_IO[1], AJ14 V_PROC_IO[2]

RTC

for DS3
+3V_DEEP_SUS: R270 *0_4S, +VCCPRTCSUS_3P3 → K8 VCCSUS3_3[9]
1U/6.3V_4 C295
+3V_RTC → A6 VCCRTC
0.1U/10V_4 C281
0.1U/10V_4 C282
1U/6.3V_4 C278
0.1U/10V_4 C297 +VCCRTCEXT
0.261A (40mils)
P14 DCPRTC[1], P16 DCPRTC[2]

USB

0.26A (40mils)
R24 +V3.3A_VCCPUSB, R558 *0_6S, 0.1U/10V_4 C303 → +3V_DEEP_SUS
for DS3
VCCSUS3_3[3], VCCSUS3_3[4], VCCSUS3_3[5], VCCSUS3_3[6] ← R24, R26, R28, U26

+1.05V
VCCUSBPLL ← U35 +V1.05S_VCCAUSB, R245 *0_6S, 0.1U/10V_4 C286

VCC3_3[3] ← L24 +V3.3S_VCCAUBG, R264 *0_4S, 0.1U/10V_4 C291 +3V

VCCIO[11], VCCIO[12], VCCIO[13], VCCIO[14] ← U30, V28, V30, Y30 +V1.05S_VCCUSBCORE, R570 *0_8S, 1U/6.3V_4 C300 +1.05V
3.629A (160mils)

VSS ← M24

DCPSUS2 ← Y35 +V1.05M_VCCDUSBSUS, *1U/6.3V_4 C299
28mA (10mils)

GPIO/LPC

0.26A (40mils)
VCCSUS3_3[7], VCCSUS3_3[8] ← R20, R22 R258 *0_4S +3V_DEEP_SUS
15mA (10mils)
for DS3
VCCDSW3_3 ← A16 +VCCPDSW, R233 *0_4S +3VS5, C284 0.1U/10V_4

VCC3_3[4], VCC3_3[5], VCC3_3[6] ← AE14, AF12, AG14 +V3.3S_VCCPCORE, R343 *0_4S +3V, 0.01U/16V_4 C345

VCCIO[15] ← U36 +V1.05S_VCCAUX, R248 *0_4S +1.05V
DCPSST ← AA14 +VCCSST, 0.1U/10V_4 C314

FUSE

VCC[1], VCC[2] ← P18, P20 +V3.3S_VCCPFUSE, R211 *0_8S +3V, R223 *0_6 +1.05V, 1U/6.3V_4 C292

VCCASW[12], VCCASW[13] ← L17, R18 PCH_VCC_1_1_20, PCH_VCC_1_1_21, R301 *0_4S +1.05V_M3
EC-DV-01

PCH VRM Power
+1.05V_M3
+V1.05S_VCCAPLL_SATA3
VCCVRM[7] ← AN11 *10uH/100MA_8, L12, *0_8S, R331, *10U/6.3V_6, C336 +1.05V +1.5V
VCCIO[16] ← AK22 +V1.05S_VCC_EXP_16, R282 *0_6S +V1.05S_VCC_EXP
3.629A (160mils)

SATA

HDA

10mA (10mils)
+VCC_HDA_IO
VCCSUSHDA ← A26 R224 *0_4S +3V_DEEP_SUS
0.1U/10V_4 C276
for DS3

POWER

U40G

VCC CORE

1.29A (60mils)
+1.05V, R279 *0_6S, +V1.05S_PCH_VCC
1U/6.3V_4 C311, 1U/6.3V_4 C315, 1U/6.3V_4 C309, 10U/6.3V/X5R_6 C317
VCCCORE[1] AA24
VCCCORE[2] AA26
VCCCORE[3] AD20
VCCCORE[4] AD22
VCCCORE[5] AD24
VCCCORE[6] AD26
VCCCORE[7] AD28
VCCCORE[8] AE18
VCCCORE[9] AE20
VCCCORE[10] AE22
VCCCORE[11] AE24
VCCCORE[12] AE26
VCCCORE[13] AG18
VCCCORE[14] AG20
VCCCORE[15] AG22
VCCCORE[16] AG24
VCCCORE[17] Y26

12/03 For SBA
+1.05V_M3
0.67A (40mils)
*0_8S, R619, +V1.05M_VCCASW
C301 1U/6.3V_4, C304 1U/6.3V_4, C305 10U/6.3V_6
VCCASW[1] AA18
VCCASW[2] U18
VCCASW[3] U20
VCCASW[4] U22
VCCASW[5] U24
VCCASW[6] V18
VCCASW[7] V20
VCCASW[8] V24
VCCASW[9] Y18
VCCASW[10] Y20
VCCASW[11] Y22
VCCASW[12] V22

DCPSUSBYP ← 1U/6.3V_4 C308, R276 5.11/F_4 +PCH_VCCDSW, U14

VCCMPHY

3.629A (160mils) +V1.05S_VCC_EXP
VCCIO[1] AM18
VCCIO[2] AM20
VCCIO[3] AM22
VCCIO[4] AF22
VCCIO[5] AR22
VCCIO[6] AT22

0.261A (40mils)
+3V_DEEP_SUS, R313 *0_4S +3V_DEEP_SUS_R

VCCSUS3_3[1] AJ30
VCCSUS3_3[2] AJ32
0.098A (20mils)
*1U/6.3V_4 C329, *10U/6.3V_6 C330, +VCCA_USBSUS
DCPSUS3_3[1] AJ26
DCPSUS3_3[2] AJ28

PCH VRM Power
+1.05V, +1.5V, L14 *10uH/100mA_8, R346 *0_8S, *10U/6.3V_6 C348, +VCCAPLL_USB3
0.476A (30mils)
VCCVRM[1] AK26
VCCVRM[2] AK28

VCCIO[7] ← AK20 +V1.05S_VCC_EXP
*1U/6.3V_4 C302, +V1.05M_VCCSUS
DCPSUS1 ← Y12
98mA (15mils)

PCH VRM Power
+1.05V, +1.5V, L32 *1uH/25mA_6, R632 *0_8S, +V1.05S_VCCAPLL_FDI, *10U/6.3V_6 C602
0.179A (20mils)
VCCVRM[3] ← BB44

VCCIO[8] AN34
VCCIO[9] AN35
+V1.05S_VCC_EXP, R296 *0_6S
3.629A (160mils)

LPT_PCH_HM87_EDS/BGA

12/03 For SBA
Layout Notes:
R5477 close to Y12
R5478 close to Y35
+1.05V_M3
R308 *0_6 +V1.05M_VCCSUS — Y12 -- DCPSUS1
R294 *0_6 +V1.05M_VCCDUSBSUS — Y35 -- DCPSUS2

CRT

+VCCA_DAC_1_2, +1.5V
70mA (15 mils)
L30 BLM18PG181SN1D_1.5A_6
VCCADAC1_5 ← P45: C587 10U/6.3V_6, C589 0.1U/10V_4, C588 0.01U/16V_4
VSS ← P43
R584 *0_6, R587 *0_8 +1.5V_LDO

13mA (10mils)
VCCADACBG3_3 ← M31 +V3.3S_ADACBG, R530 *0_8S +3V, R529 *0_8 +3V_BG

HVCMOS

VCC3_3[1], VCC3_3[2] ← R30, R32 +V3.3S_VCC_GIO, R252 *0_4S +3V, 0.1U/10V_4 C293
133mA (20mils)

DMI / PCIE

PCH VRM Power
+V1.05S_VCCAPLL_EXP, +1.05V
VCCVRM[4] ← BE22 L13 *1uH/25mA_6, R344 *0_8S +1.5V, *10U/6.3V_6 C347
VCCIO[10] ← AK18 +V1.05S_VCC_EXP_10, R315 *0_8S +V1.05S_VCC_EXP
3.629A (160mils)

USB3

SPI

+V3.3M_VCCPSPI
EC-DV-14
+3V_DEEP_SUS
R690 *0_6S, +3V_M3
VCCSPI ← AD12 R272 *0_6, 1U/6.3V_4 C310
22mA (10mils)

If EC support embedded flash , SPI power must be used S5_ON power rail for EC load code.

FDI

LPT_PCH_HM87_EDS/BGA

If have power noise issue then stuff it.
+3V, +1.5V_LDO
U39 G9090-150T11U
VINVOUT, EN, GND NC
C596 *1U/6.3V_4

PCH VCCIO Power

+1.05V, +V1.05S_VCC_EXP
3.629A (160mils)
Near Pin AN34,AN35
C331 10U/6.3V_6, C326 1U/6.3V_4, C322 1U/6.3V_4, C312 1U/6.3V_4, C319 1U/6.3V_4, C325 1U/6.3V_4

PCH band gap Power

+3VS5, Q39 *ME2N7002D, +3V_BG
(47) MAINON_15V

PCH VCCSUS

+3V_DEEP_SUS
C584 0.1U/10V_4

PCH DS3 PWR

RESERVE IT

+3VS5, +3V_DEEP_SUS
R536 *0_8
C582 1U/6.3V_4
U38 AP2821KTR-G1
IN, IN, ON/OFF, OUT, GND
(32) SLP_SUS_ON_GPG2
EC-DV-15
R555 *100K/F_4

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Quanta Computer Inc.

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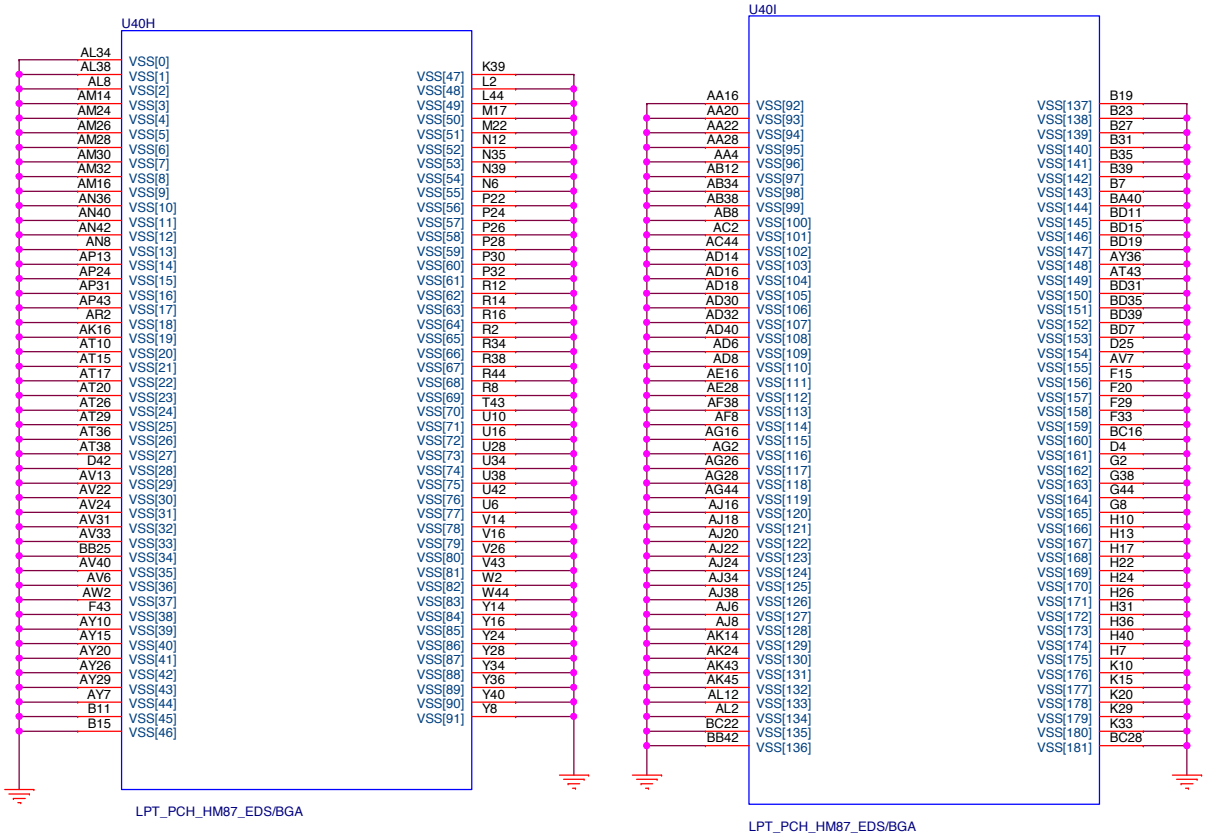
Lynx Point (GND)



PROJECT : M Note		
Quanta Computer Inc.		
Size: B	Document Number: PCH 6/6 (GND)	Rev: 1A
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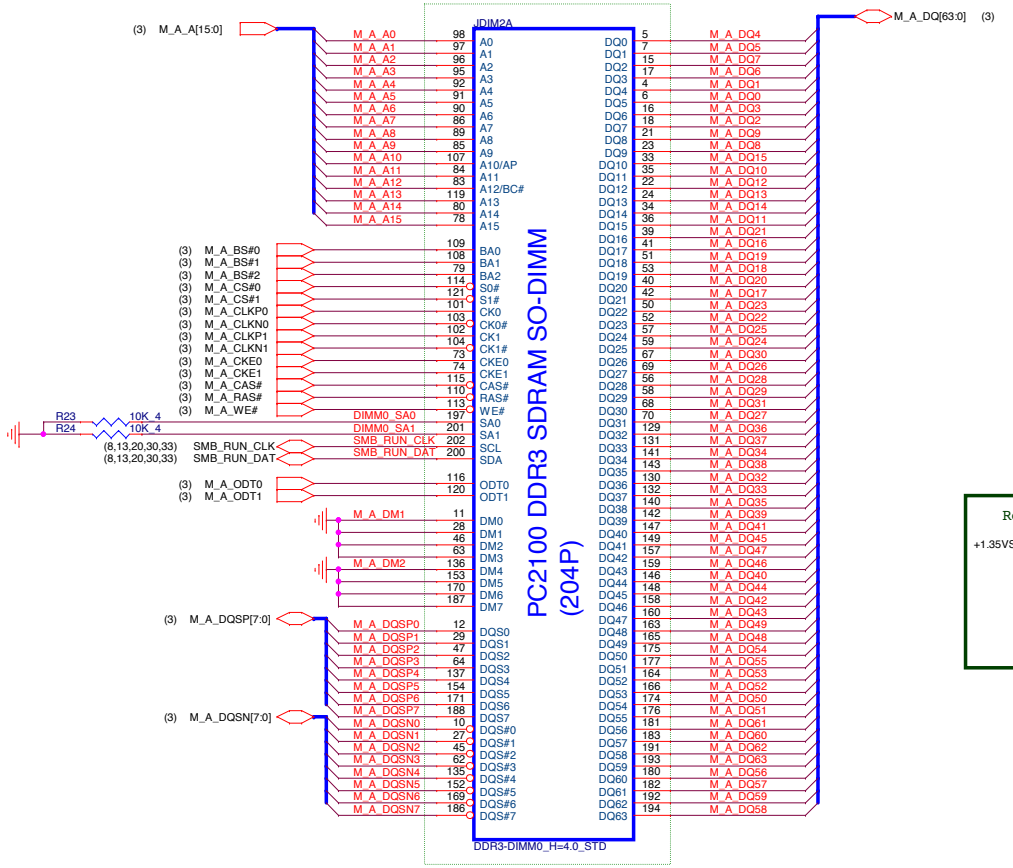

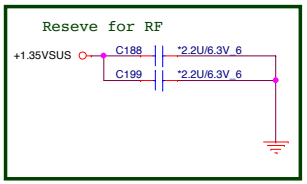

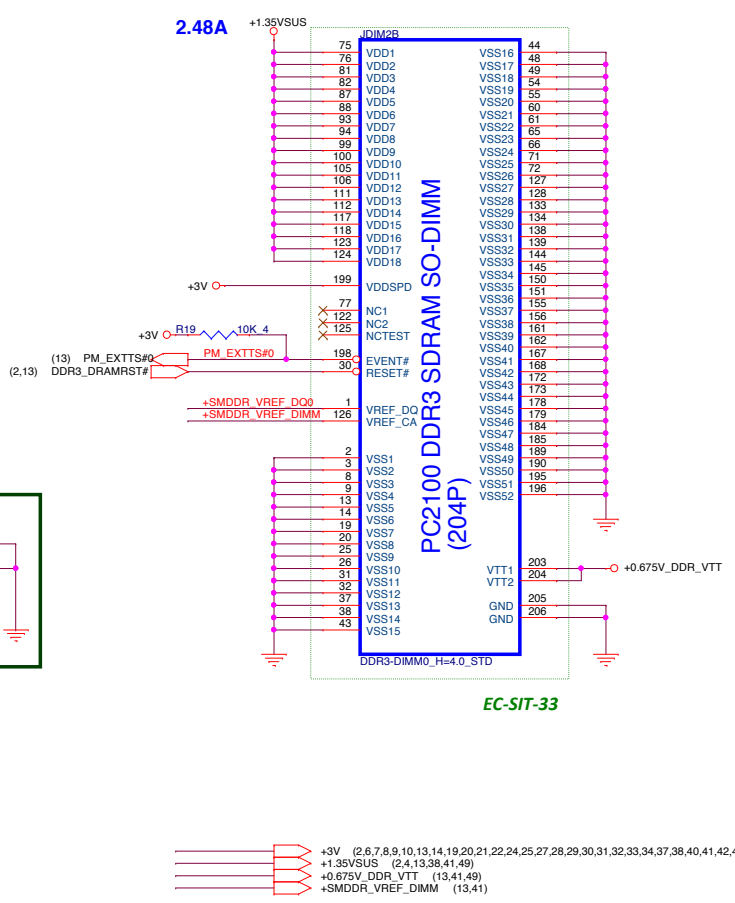

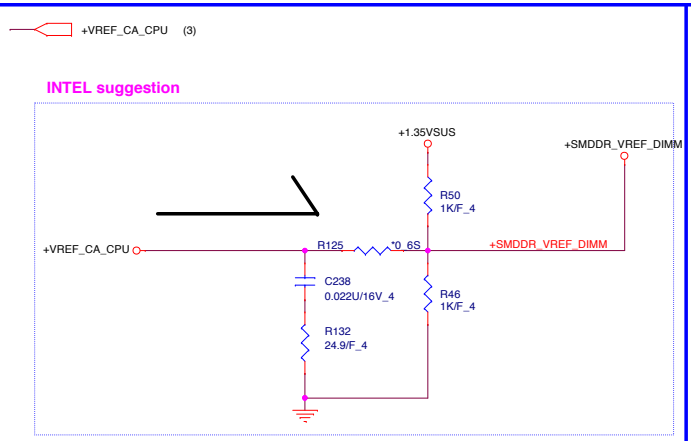

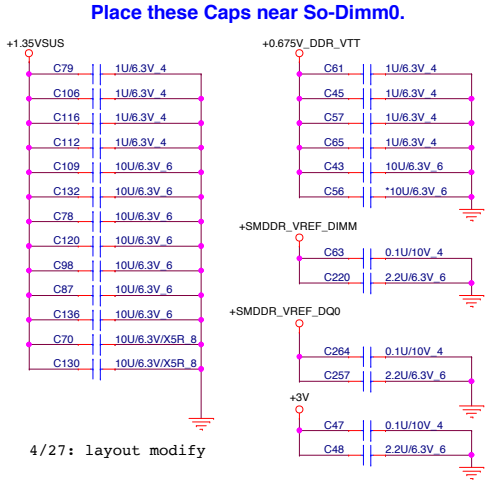

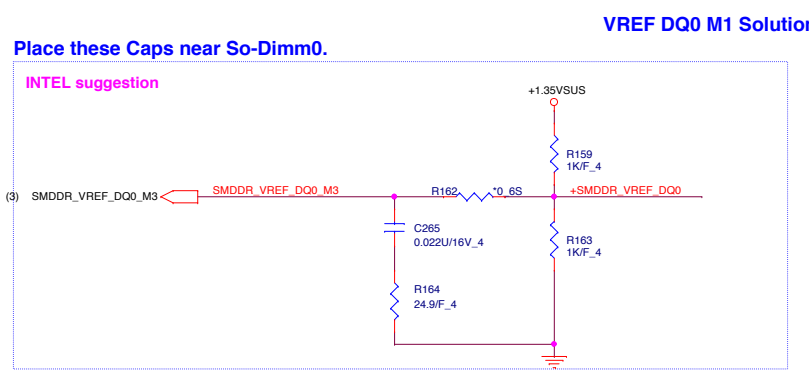

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (4.0H)	1A

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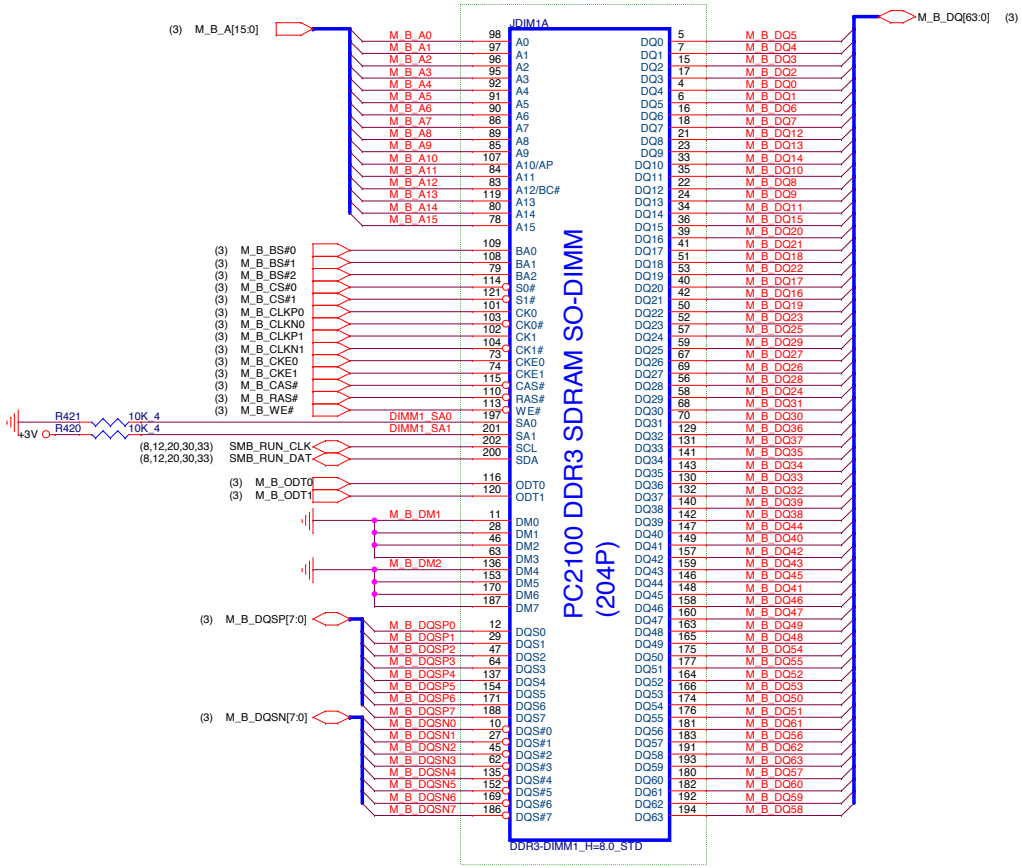
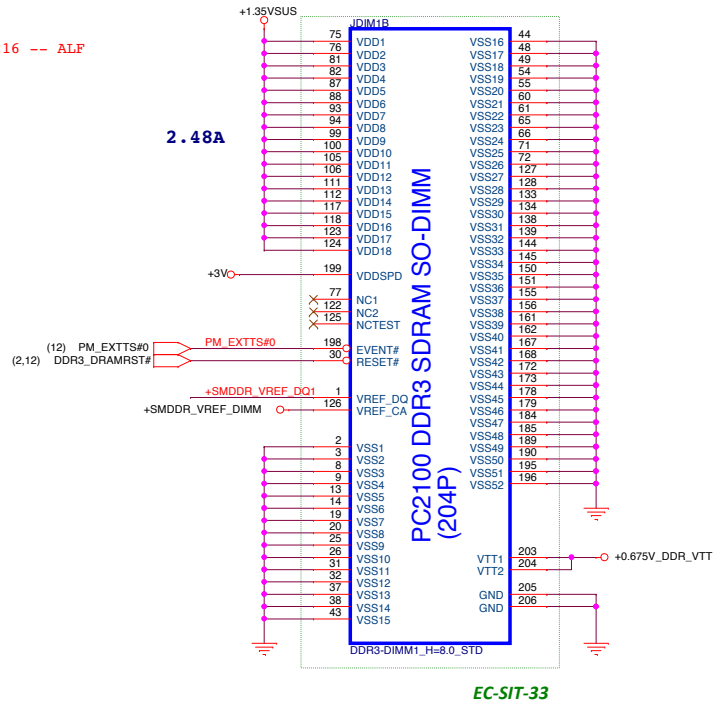


EC-SIT-33

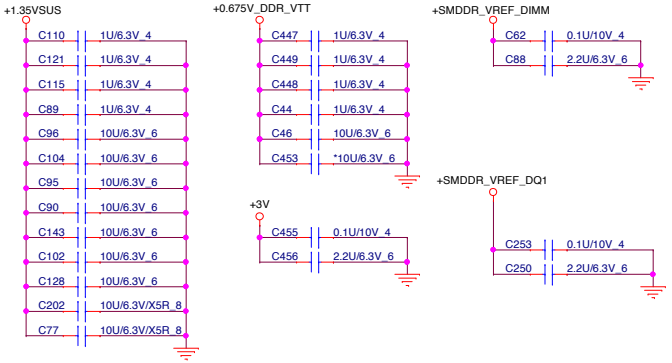
Footprint & P/N = okay @1216 -- ALF



EC-SIT-33

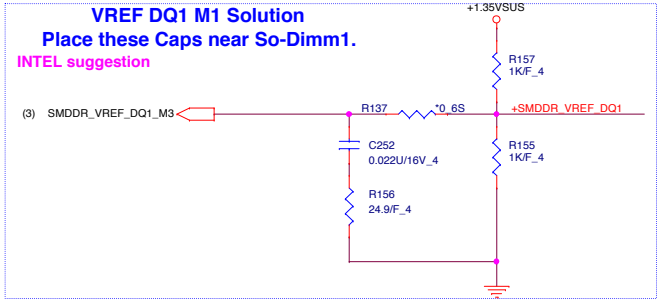
+3V (2,6,7,8,9,10,12,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,4
+1.35VSUS (2,4,12,38,41,49)
+0.675V_DDR_VTT (12,41,49)
+SMDDR_VREF_DIMM (12,41)

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution
Place these Caps near So-Dimm1.

INTEL suggestion



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Quanta Computer Inc.		
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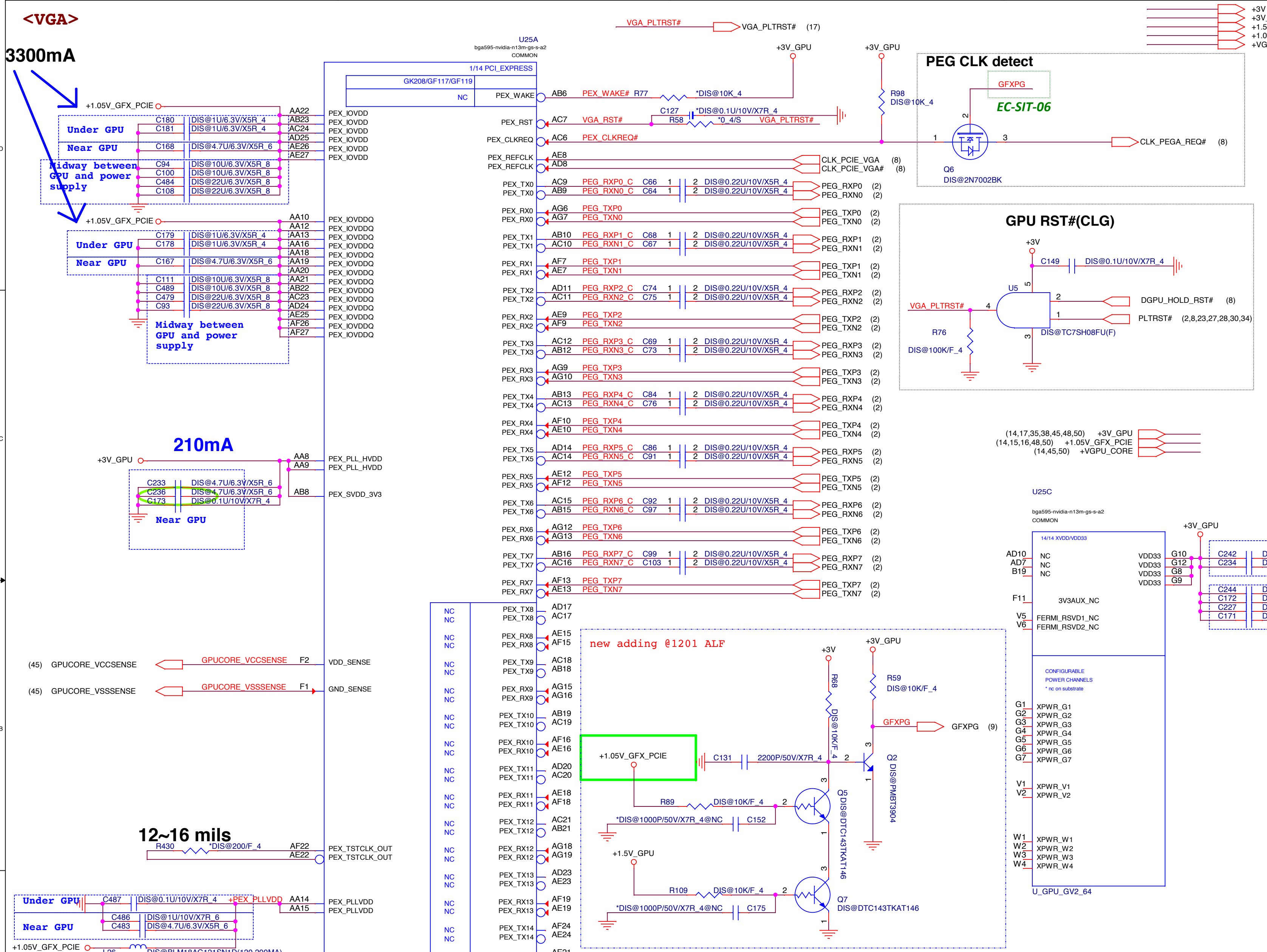
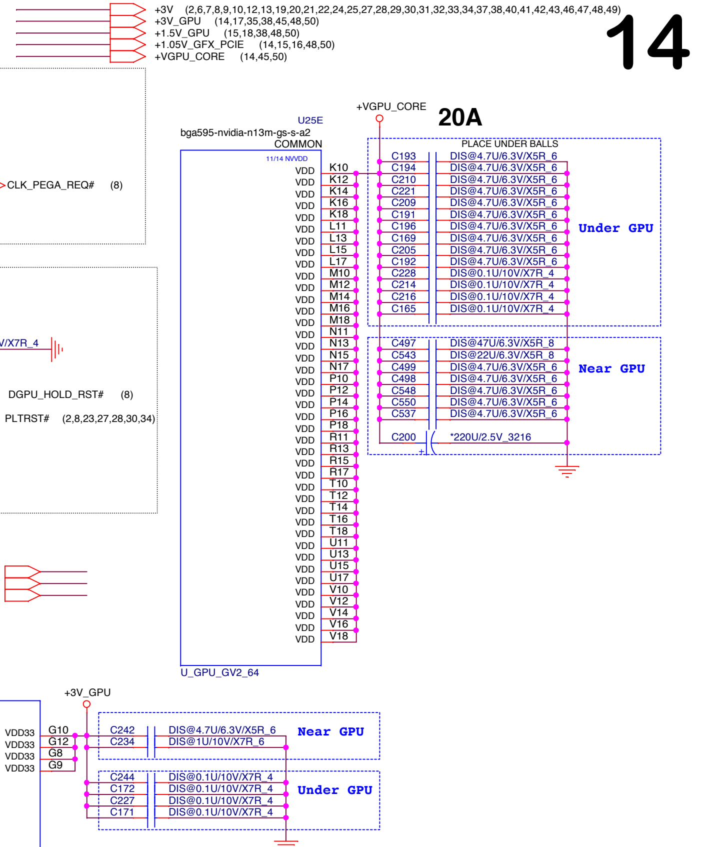
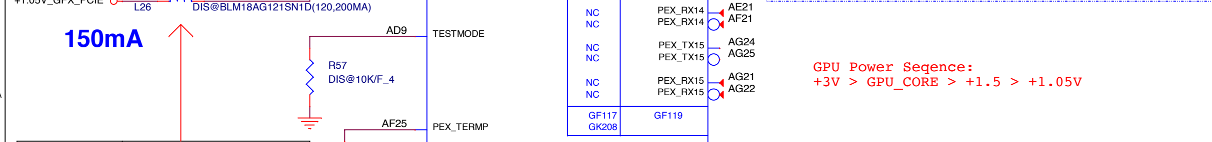
<VGA>

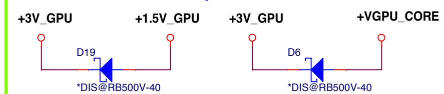






PEX_PLLVDD	120 ohm @100MHz bead
N14P-GV2	0 ohm
N14M-GE	Stuff
N14M-GL	Stuff

For Power Down Sequence (Group C)



NV's Suggestion @1218 ALF

Group C	
N14P-GV2	Group C - Un-Stuff
N14M-GE	Group C - Stuff
N14M-GL	Group C - Stuff

Table 2. GPU Power Rails

GPU Power Rail	Nominal Value	Comments
NVVDD	GPU SKU Specific	GPU Core power rail
FBVDD[2]	1.35 V or 1.5 V	VRAM Core power for Frame Buffer components
FBVDDQ[2]	1.35 V or 1.5 V	VRAM I/O and GPUs Frame Buffer I/O power rail
IFPx_IOVDD[3]	1.05 V or 3.3V	Powers IFP blocks
IFPx_PLLVDD[3]	1.05 V or 3.3 V	Integrated Digital Display PLL Power Rails
PEX_IOVDD/Q	1.05 V	GPUs PCIE interface power rail
PEX_SVDD_3V3, PEX_PLL_HVDD	3.3 V	GPU PCIE PLL Power Rails
PEX_PLLVDD	1.05 V	GPU PCIE PLL Power Rails
FBx_PLL_AVDD	1.05 V or 3.3 V	Frame Buffer PLL Power Rail
FBx_DLL_AVDD (GB2-64 and GB4-128)	1.05 V	Frame Buffer PLL and DLL Power Rail
FBx_PLL_DLL_AVDD (GB2-192 and GB3-256)	1.05 V	Frame Buffer PLL and DLL Power Rail
PLLVDD, GPCPLL_AVDD LXS_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
VID_PLLVDD	1.05 V	Video Pixel Clock PLL Analog Power Rail
SP_PLLVDD	1.05 V	Core Clock PLL Analog Power Rail
DACx_VDD[1]	3.3 V	Powers the DAC interfaces
VDD33(NV3V3)[4]	3.3 V	Powers slower logic such as GPIOs, I2C, AUX channels and SLI

Notes: 1. The same power plane can be used for VDD33 and DACx_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays)
4. On GB3-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

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Quanta Computer Inc.		
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<VGA>

+5VS5 (19,26,29,37,38,40,41,42,43,45,46,47,48,49)
+3VS5 (2,6,7,9,10,17,20,23,24,25,28,32,37,40,44,47,53)
+1.5V_GPU (14,18,38,48,50)
+1.05V_GFX_PCIE (14,16,48,50)

GC6 feature for N14p-GV2

new adding @1201 ALF

2.16A

U25B bga595-nvidia-n13m-gs-s-a2 COMMON

FB_CLAMP R168 Ra 0_4 F3

for GC6 support

R127 DIS@10K/F_4 Rb

for GC6 @1218 ALF

GPIO0	For GC6 function
N14P-GV2	Ra - Stuff / Rb - Stuff
N14M-GE	Ra - Un-Stuff/Rb - Stuff
N14M-GL	Ra - Un-Stuff/Rb - Stuff

FB_CLAMP	NC
GF117/GK208	GF119

2/14 FBA

FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63

(18) FBA_CMD0 FBA_CMD0 C27 FBA_CMD0
C26 FBA_CMD1
(18) FBA_CMD2 FBA_CMD2 E24 FBA_CMD2
(18) FBA_CMD3 FBA_CMD3 F24 FBA_CMD3
(18) FBA_CMD4 FBA_CMD4 D27 FBA_CMD4
(18) FBA_CMD5 FBA_CMD5 D26 FBA_CMD5
(18) FBA_CMD6 FBA_CMD6 F25 FBA_CMD6
(18) FBA_CMD7 FBA_CMD7 F26 FBA_CMD7
(18) FBA_CMD8 FBA_CMD8 F23 FBA_CMD8
(18) FBA_CMD9 FBA_CMD9 G22 FBA_CMD9
(18) FBA_CMD10 FBA_CMD10 G23 FBA_CMD10
(18) FBA_CMD11 FBA_CMD11 G24 FBA_CMD11
(18) FBA_CMD12 FBA_CMD12 F27 FBA_CMD12
(18) FBA_CMD13 FBA_CMD13 G25 FBA_CMD13
(18) FBA_CMD14 FBA_CMD14 G27 FBA_CMD14
(18) FBA_CMD15 FBA_CMD15 G26 FBA_CMD15
(18) FBA_CMD16 FBA_CMD16 M24 FBA_CMD16
M23 FBA_CMD17
(18) FBA_CMD18 FBA_CMD18 K24 FBA_CMD18
(18) FBA_CMD19 FBA_CMD19 K23 FBA_CMD19
(18) FBA_CMD20 FBA_CMD20 M27 FBA_CMD20
(18) FBA_CMD21 FBA_CMD21 M26 FBA_CMD21
(18) FBA_CMD22 FBA_CMD22 M25 FBA_CMD22
(18) FBA_CMD23 FBA_CMD23 K26 FBA_CMD23
(18) FBA_CMD24 FBA_CMD24 K22 FBA_CMD24
(18) FBA_CMD25 FBA_CMD25 J23 FBA_CMD25
(18) FBA_CMD26 FBA_CMD26 J25 FBA_CMD26
(18) FBA_CMD27 FBA_CMD27 J24 FBA_CMD27
(18) FBA_CMD28 FBA_CMD28 K27 FBA_CMD28
(18) FBA_CMD29 FBA_CMD29 K25 FBA_CMD29
(18) FBA_CMD30 FBA_CMD30 J27 FBA_CMD30
J26 FBA_CMD31

For debug only 10mA

+1.5V_GPU R134 *DIS@60.4/F_4 FBA_DEBUG0 F22 FBA_DEBUG0
R126 *DIS@60.4/F_4 FBA_DEBUG1 J22 FBA_DEBUG1

(18) VMA_CLK0 VMA_CLK0 D24 FBA_CLK0
(18) VMA_CLK0# VMA_CLK0# D25 FBA_CLK0
(18) VMA_CLK1 VMA_CLK1 N22 FBA_CLK1
(18) VMA_CLK1# VMA_CLK1# M22 FBA_CLK1

D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67

+1.05V_GFX_PCIE

Near GPU 15mils width 200mA

L29 DIS@BLM18PG300SN1D_1A_6 FB_PLLAVDD F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22

30ohm/100MHz
ESR=0.01ohm

FB_DLLAVDD	FB_PLLAVDD
GF119/GK208	GF117

Under GPU
C241 DIS@0.1U/10V/X7R_4
C564 DIS@0.1U/10V/X7R_4
C232 DIS@0.1U/10V/X7R_4

Near GPU
C571 DIS@22U/6.3V/X5R_8

FB_VREF_PROBE D23 +FB_VREF1 TP21

U_GPU_GV2_64

Q37 DIS@2N7002BK
(32,48) FB_CLAMP FB_CLAMP 3 1 FB_CLAMP_MON (17)
2
C575 *DIS@10U/6.3V/X5R_6
+5VS5
R528 DIS@10K/F_4
EC-SIT2-08
3
5 Q35A DIS@2N7002BKS 4
C580 *DIS@10U/6.3V/X5R_6
+3VS5
R526 DIS@10K/F_4
6
(32,45,48) GFXON 2 1 Q35B DIS@2N7002BKS

(Group B)

NV's Suggestion @1218 ALF

GC6 -- Group B	
N14P-GV2	Group B - Stuff
N14M-GE	Group B - Un-Stuff
N14M-GL	Group B - Un-Stuff

U25D bga595-nvidia-n13m-gs-s-a2 COMMON 12/14 FBVDDQ

FBVDDQ B26
FBVDDQ C25
FBVDDQ E23
FBVDDQ E26
FBVDDQ F14
FBVDDQ P21
FBVDDQ G13
FBVDDQ G14
FBVDDQ G15
FBVDDQ G16
FBVDDQ G18
FBVDDQ G19
FBVDDQ G20
FBVDDQ G21
FBVDDQ H24
FBVDDQ H26
FBVDDQ J21
FBVDDQ K21
FBVDDQ L22
FBVDDQ L24
FBVDDQ L26
FBVDDQ M21
FBVDDQ N21
FBVDDQ R21
FBVDDQ T21
FBVDDQ V21
FBVDDQ W21

+1.5V_GPU R519 DIS@40.2/F_4 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
R506 DIS@42.2/F_4 FB_CAL_PU_GND C24 FB_CAL_PU_GND
R513 DIS@51.1/F_4 FB_CAL_TERM_GND B25 FB_CALTERM_GND

U_GPU_GV2_64

(18) VMA_DQ[63..0] VMA_DQ[63..0]
(18) VMA_DM[7..0] VMA_DM[7..0]
(18) VMA_WDQS[7..0] VMA_WDQS[7..0]
(18) VMA_RDQS[7..0] VMA_RDQS[7..0]

FBA_CMD2 R487 DIS@10K/F_4
FBA_CMD3 R493 DIS@10K/F_4
FBA_CMD5 R120 DIS@10K/F_4
FBA_CMD18 R438 DIS@10K/F_4
FBA_CMD19 R441 DIS@10K/F_4

DDR3 Command Bit	Data[31..0]	Data[63..32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

+1.5V_GPU

Under GPU
C243 DIS@0.1U/10V/X7R_4
C231 DIS@0.1U/10V/X7R_4
C258 DIS@4.7U/6.3V/X5R_6
C198 DIS@1U/10V/X7R_6
C226 DIS@1U/10V/X7R_6
C170 DIS@4.7U/6.3V/X5R_6
C536 DIS@10U/6.3V/X5R_8
C542 DIS@22U/6.3V/X5R_8
Near GPU

U25F bga595-nvidia-n13m-gs-s-a2 COMMON 13/14 GND

M13 GND GND A2
M15 GND GND AB17
M17 GND GND AB20
N10 GND GND AB24
N12 GND GND AC2
N14 GND GND AC22
N16 GND GND AC26
N18 GND GND AC5
P11 GND GND AC8
P13 GND GND AD12
P15 GND GND AD13
P17 GND GND AE26
P2 GND GND AD15
P23 GND GND AD16
P26 GND GND AD18
P5 GND GND AD19
R10 GND GND AD21
R12 GND GND AD22
R14 GND GND AE11
R16 GND GND AE14
R18 GND GND AE17
T11 GND GND AE20
T13 GND GND AB11
T15 GND GND AF1
T17 GND GND AF11
U10 GND GND AF14
U12 GND GND AF17
U14 GND GND AF20
U16 GND GND AF23
U18 GND GND AF5
U2 GND GND AF8
U23 GND GND AG2
U26 GND GND AG26
U5 GND GND AB14
V11 GND GND B1
V13 GND GND B11
V15 GND GND B14
V17 GND GND B17
Y2 GND GND B20
Y23 GND GND B23
Y26 GND GND B27
Y5 GND GND B5
GND B8
GND E11
GND E14
GND E17
GND E2
GND E20
GND E22
GND E25
GND E5
GND E8
GND H2
GND H23
GND H25
GND H5
GND K11
GND K13
GND K15
GND K17
GND L10
GND L12
GND L14
GND L16
GND L18
GND L2
GND L23
GND L25
AA7 GND GND L5
AB7 GND GND M11

U_GPU_GV2_64

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GL (MEMORY/GND) 2/5	1A

Date: 星期六, 五月 25, 2013 Sheet 15 of 61

<VGA> <HDM> <CRT>

Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm

U25G
bga595-nvidia-n13m-gs-s-a2
COMMON

4/14 IFPAB

IFPAB

U_GPU_GV2_64

U25H
bga595-nvidia-n13m-gs-s-a2
COMMON

5/14 IFPC

IFPC

U_GPU_GV2_64

U25K
bga595-nvidia-n13m-gs-s-a2
COMMON

3/14 DACA

U_GPU_GV2_64

+1.05V_GFX_PCIE (14,15,48,50)

U25I
bga595-nvidia-n13m-gs-s-a2
COMMON

6/14 IFPD

IFPD

U_GPU_GV2_64

U25J
bga595-nvidia-n13m-gs-s-a2
COMMON

7/14 IFPEF

IFPE

IFPF

U_GPU_GV2_64

EC-DV-23	
VID_PLLVDD	R115
N14P-GV2	Stuff
N14M-GE	Un-Stuff
N14M-GL	Un-Stuff

+1.05V_GFX_PCIE

12~16mils

Near GPU

Under GPU

Under GPU Near GPU

U25M
bga595-nvidia-n13m-gs-s-a2
COMMON

9/14 XTAL_PLL

U_GPU_GV2_64

EC-DV-23

(35) GPU_XTAL27_IN

DIS@27MHz

Project : M Note		
Quanta Computer Inc.		
Size: Custom	Document Number: N14M-GL (DISPLAY) 3/5	Rev: 1A
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<VGA>

U25L
bga595-nvidia-n13m-gs-s-a2
COMMON

NV's Suggestion @1218 ALF

MULTI_STRAP_REF0_GND	
N14P-GV2	Ra - Stuff
N14M-GE	Ra - Un-Stuff
N14M-GL	Ra - Un-Stuff

U_GPU_GV2_64

U25N
bga595-nvidia-n13m-gs-s-a2
COMMON

for GC6 @1218 ALF

GPIO0	For GC6 function
N14P-GV2	Ra - Stuff / Rb - Stuff
N14M-GE	Ra - Un-Stuff/Rb - Stuff
N14M-GL	Ra - Un-Stuff/Rb - Stuff

for GC6 @1201 ALF

Reserve it for GPIO9 @1222 ALF

Del PSI control for 1 phase DEM Mode @ 1130

GC6 feature for N14P-GV2 (Group A)
Low Power State on Idle
new adding @1201 ALF
NV's Suggestion @1218 ALF

GC6 -- Group A	
N14P-GV2	Group A - Stuff
N14M-GE	Group A - Un-Stuff
N14M-GL	Group A - Un-Stuff

+3VS5 (2,6,7,9,10,15,20,23,24,25,28,32,37,40,44,47,53)
+3V_GPU (14,35,38,45,48,50)

DDR3 RAM CFG

GPU SKU	GPU	VRAM Vendor	Type		Config	VRAM P/N	Max Speed CL	D/C Mini	RAM_CFG	Strap 3	Strap 2	Strap 1	Strap 0
GF117	N14M-GE/GL	Micron	DDR3	1.5V/1.5V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1150	0x1	PD 10K	PD 10K	PD 10K	PU 10K
						MT41K256M16HA-107G:E	900Mhz						
		Samsung	DDR3	1.5V/1.5V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x5	PD 10K	PU 10K	PD 10K	PU 10K
						K4W2G1646E-BC11	900Mhz						
		Hynix	DDR3	1.5V/1.5V	128Mx16	H5TQ2G63DFR-N0C	1000Mhz	NA	0x6	PD 10K	PU 10K	PU 10K	PD 10K
						H5TQ2G63DFR-11C	900Mhz						
		Samsung	DDR3	1.5V/1.5V	256Mx16	K4W4G1646B-HC11	900Mhz	NA	0xB	PU 10K	PD 10K	PU 10K	PU 10K
		Micron	DDR3	1.5V/1.5V	256Mx16	MT41K256M16HA-107G:E	900Mhz	NA	0xD	PU 10K	PD 10K	PU 10K	PU 10K
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TQ4G63MFR-11C	900Mhz	NA	0x3	PD 10K	PD 10K	PU 10K	PU 10K
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TQ4G63AFR-11C	900Mhz	NA	0x4	PD 10K	PU 10K	PU 10K	PD 10K

GF117 SKU	
Item	N14M-GL-B-A2
Device ID	0x1140
Package	GB4-128
Internal P/N	GF117, 28nm
ROM_SI	10kohm pull down
ROM_SO	10kohm pull down
ROM_SCLK	10kohm pull down
Strap0	Refer to N14x_RAM_Straps table
Strap1	
Strap2	
Strap3	
Strap4	10kohm pull down
NVVDD Boot Voltage	0.9V

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14M-GL (GPIO/STRAPS) 4/5	1A

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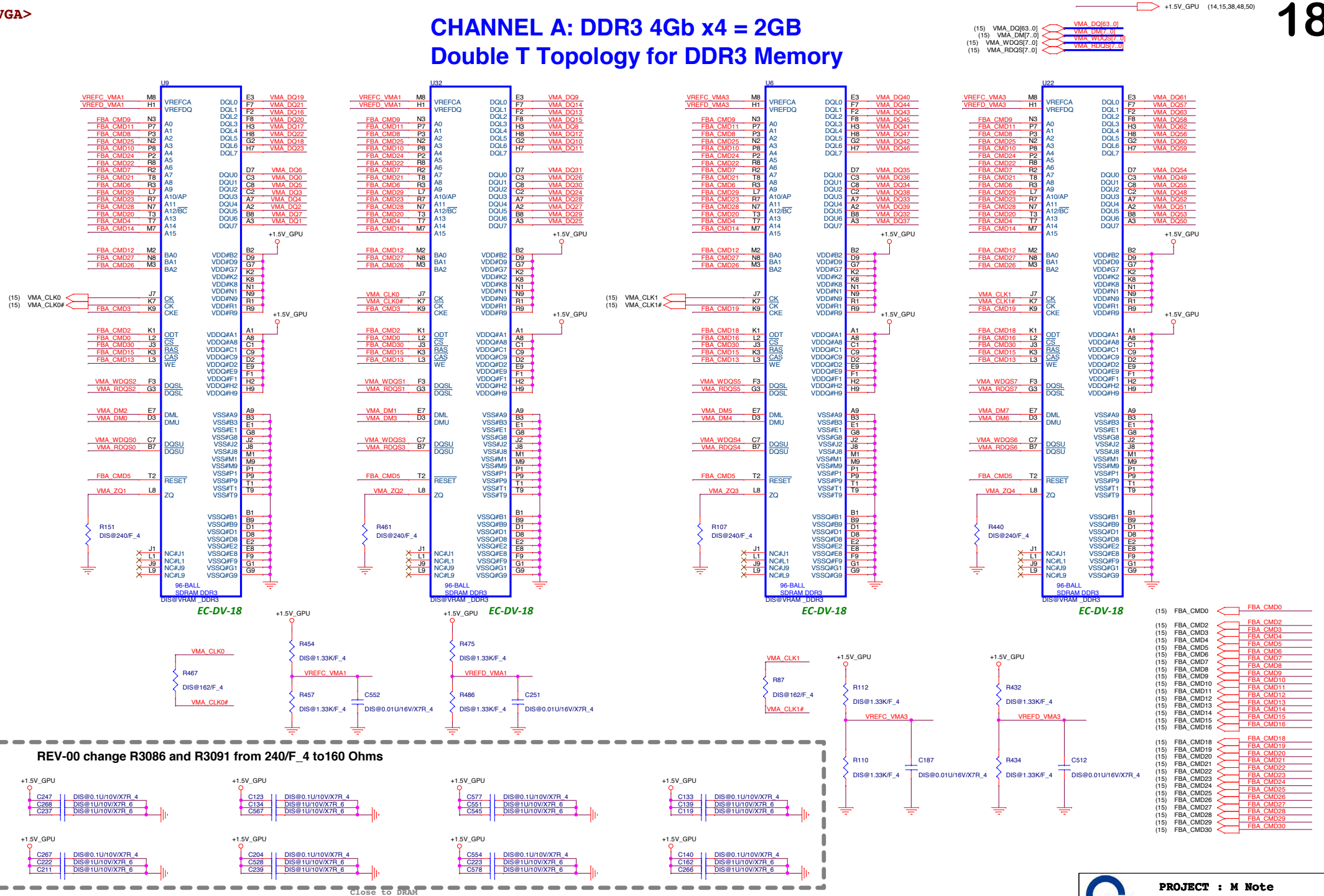
CHANNEL A: DDR3 4Gb x4 = 2GB
Double T Topology for DDR3 Memory

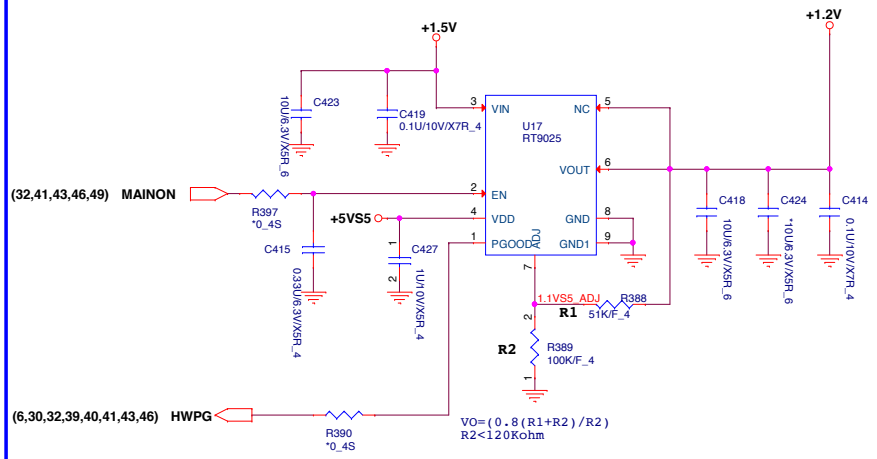


REV-00 change R3086 and R3091 from 240/F_4 to160 Ohms

+5VS5 (15,26,29,37,38,40,41,42,43,45,46,47,48,49)
+3V (2,6,7,8,9,10,12,13,14,20,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)
+1.5V (6,7,8,10,24,28,46,48,49)
+1.2V

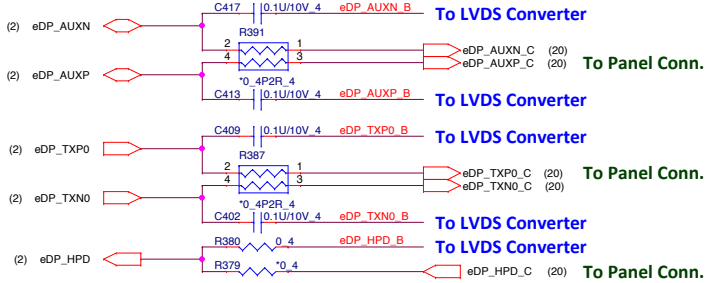
1.2V Power Source

1.2 V +/- 5%
TDC:0.3A(max)

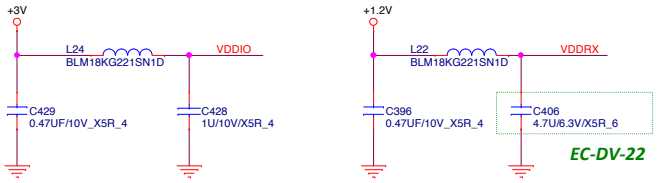


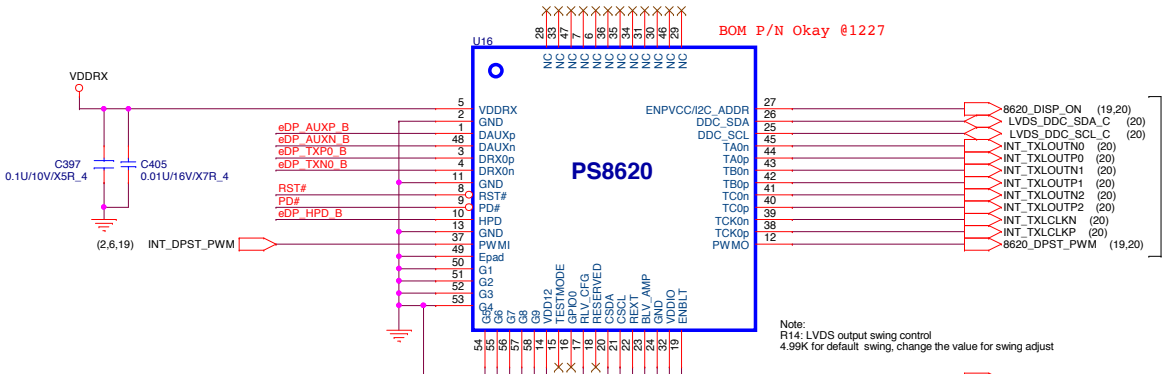
New Adding for eDP and LVDS Panel @1128 -- ALF

For BOM Control:
1. LVDS Panel : Stuff "To LVDS Converter. (Default)
2. eDP Panel : Stuff " To Panel Conn.

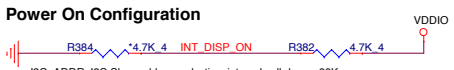


For eDP, Stuff

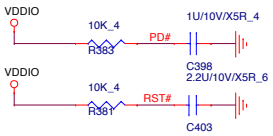


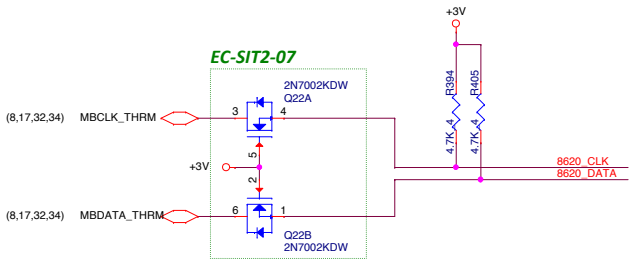


Power On Configuration



I2C_ADDR: I2C Slave address selection, internal pull-down ~80K
L: 0x10h~0x1Fh
H: 0x90h~0x9Fh





Switching Regulator Layout Guideline

1. Place the switching regulator inductor (L3) close to SW_OUT Pin (Pin13).
2. The SW_OUT output traces should be as wide as possible.
3. The GNDX pin (Pin14) should be connected to the main PCB ground plane, with the device GND pins of the PS8622 connected to separate GND island (GNDA) for the device. The GND island (GNDA) should be connected to the main GND plane (GND) with a single-point connection by use of a wide PCB trace.
4. Place the 4.7uF decoupling Capacitor (C4) for VDDIOX close to VDDIOX pin.
5. The GND of the 4.7uF capacitor (C4) for VDDIOX should be placed close to the GND of 4.7uF capacitor (C5) behind Inductor.
6. Place the bead (L2) for VDDIOX close to PS8622.

PROJECT : M Note			
Quanta Computer Inc.			
Size: Custom	Document Number: PS8620		Rev: 1A
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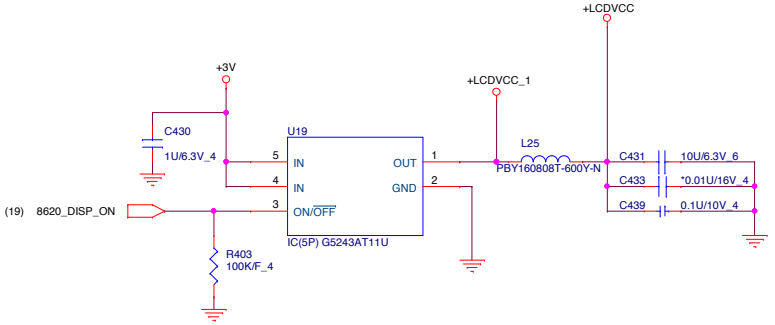
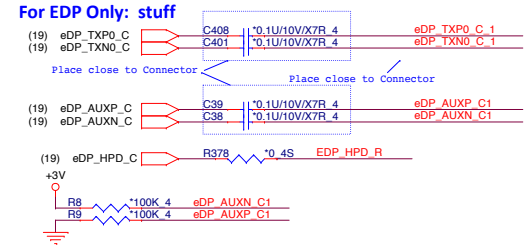
VIN (38,39,40,41,42,43,45,46,51)
+3VS5 (2,6,7,9,10,15,17,23,24,25,28,32,37,40,44,47,53)
+3V (2,6,7,8,9,10,12,13,14,19,21,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

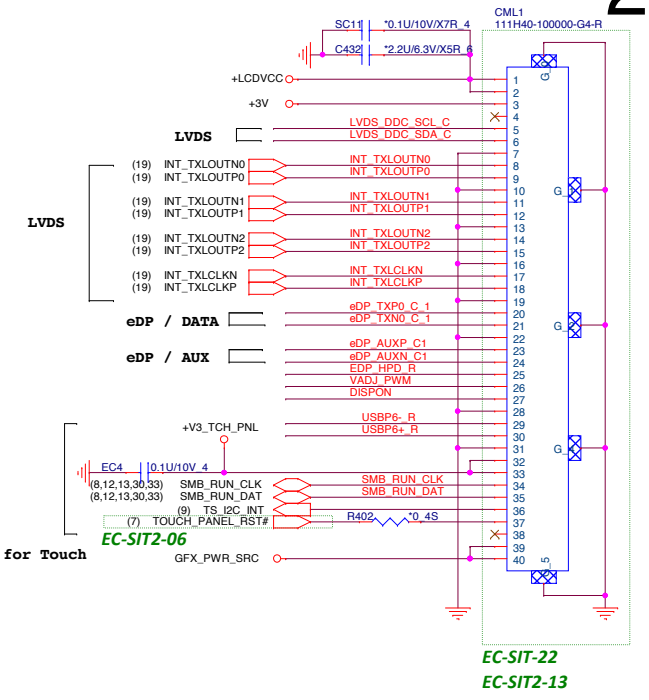
LCDVCC



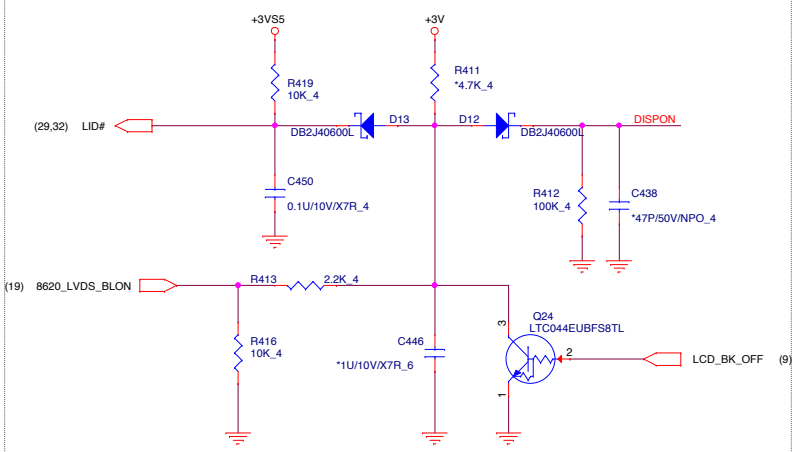
For LVDS only : stuff

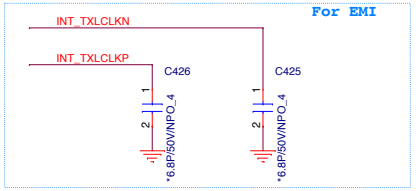
For EDP Only: stuff

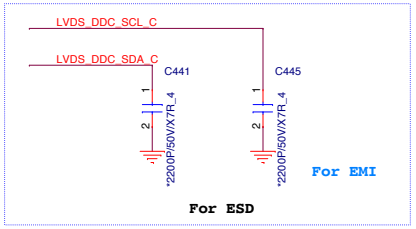




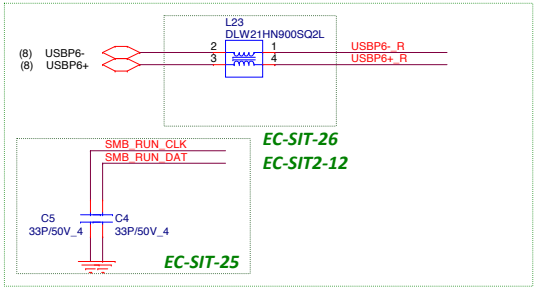
Back light







EC-DV-05
EC-SIT-21



Touch Panel VCC Control

+3V_TOUCH_PANEL
Max Current : 800mA

PROJECT : M Note
Quanta Computer Inc.

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Custom	LCD CONN / Touch Panel	1A
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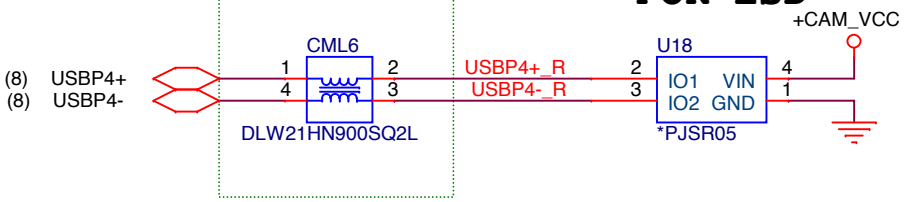
CAMERA CONN

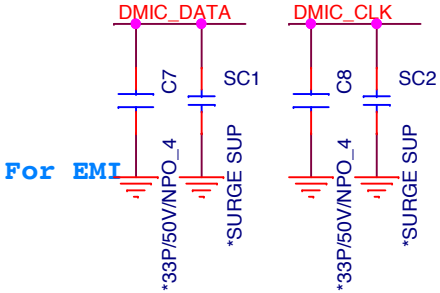
+3V (2,6,7,8,9,10,12,13,14,19,20,22,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

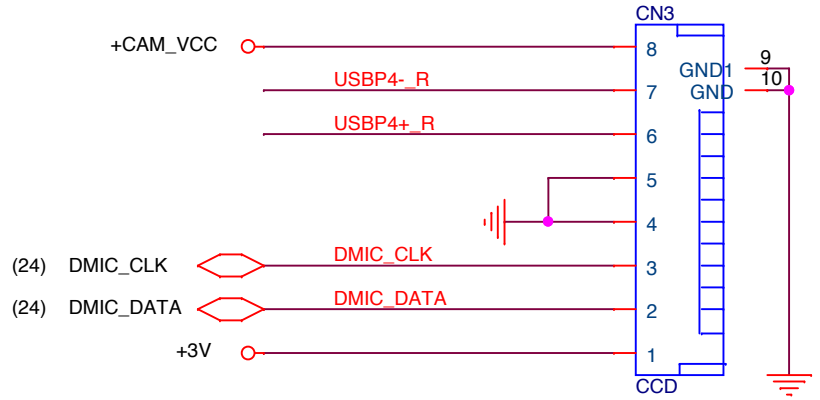
EC-SIT2-12

EC-SIT-24

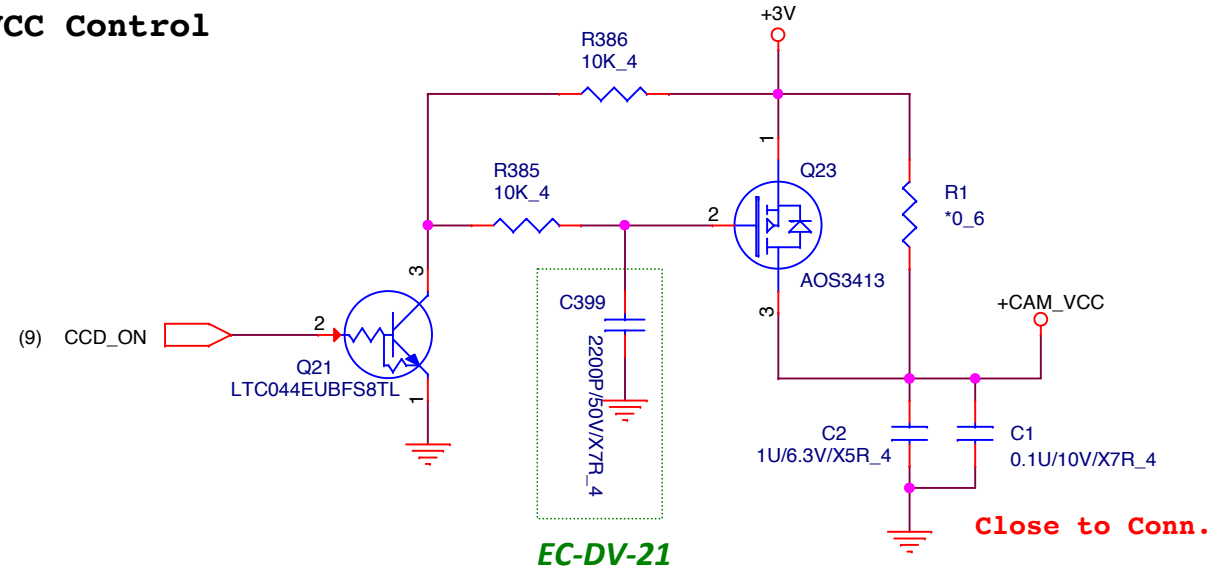
FOR ESD







CAMERA VCC Control



EC-DV-21

PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
A	CAMERA	1A
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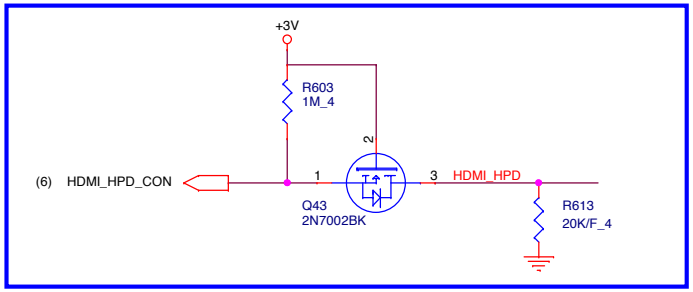
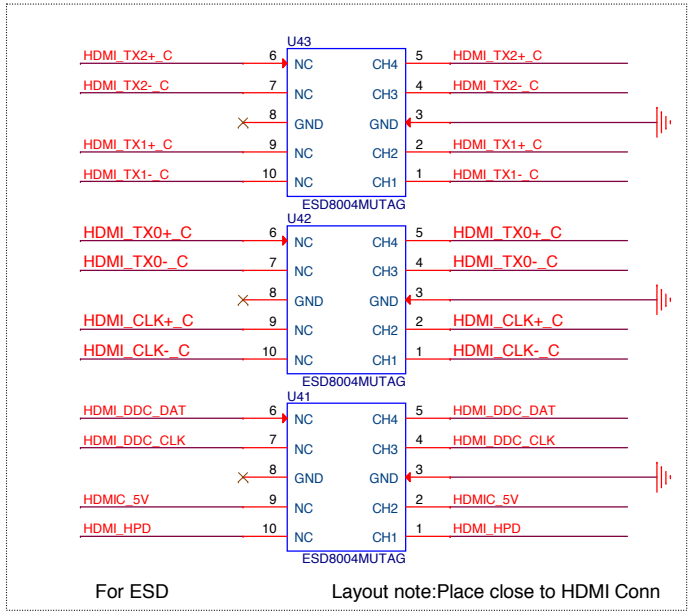
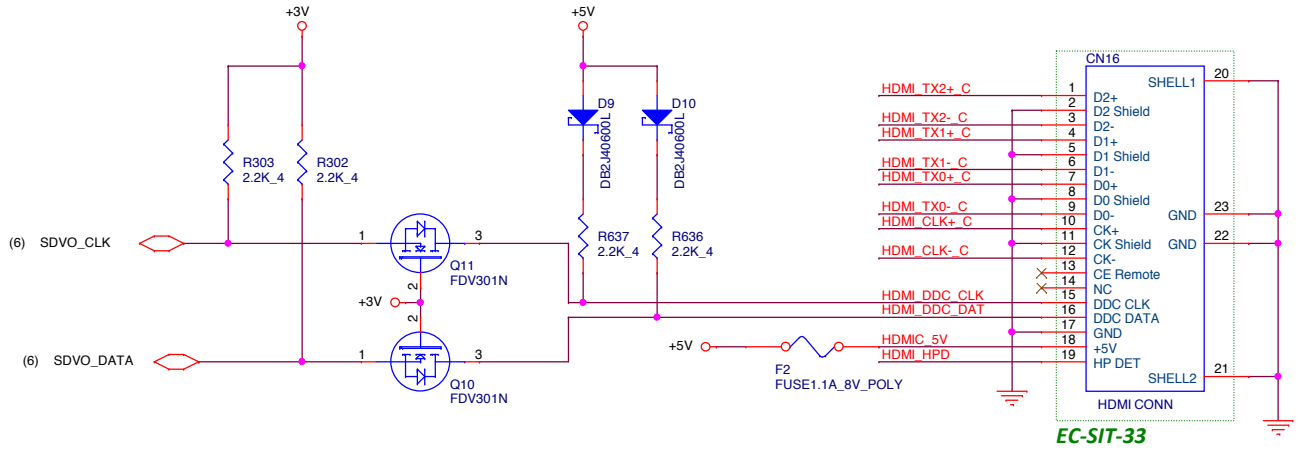
+5V (7,24,25,31,33,34,39,47,49)
+3V (2,6,7,8,9,10,12,13,14,19,20,21,24,25,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

close to HDMI conn

(2) IN_CLK# — IN_CLK# — C601 0.1U/10V_4 — HDMI_CLK-_C
(2) IN_CLK — IN_CLK — C603 0.1U/10V_4 — HDMI_CLK+_C
(2) IN_D0# — IN_D0# — C604 0.1U/10V_4 — HDMI_TX0-_C
(2) IN_D0 — IN_D0 — C605 0.1U/10V_4 — HDMI_TX0+_C
(2) IN_D1# — IN_D1# — C610 0.1U/10V_4 — HDMI_TX1-_C
(2) IN_D1 — IN_D1 — C611 0.1U/10V_4 — HDMI_TX1+_C
(2) IN_D2# — IN_D2# — C613 0.1U/10V_4 — HDMI_TX2-_C
(2) IN_D2 — IN_D2 — C614 0.1U/10V_4 — HDMI_TX2+_C

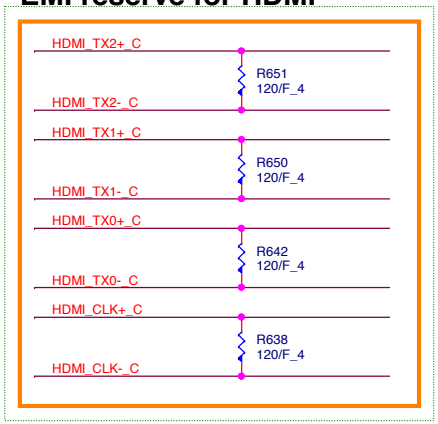




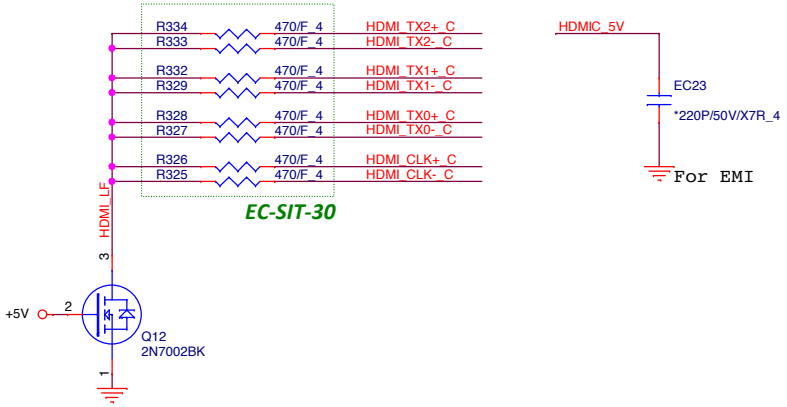


EC-SIT-33

EMI reserve for HDMI



EC-DV-34



EC-SIT-30

PROJECT : M Note		
Quanta Computer Inc.		
Size: Custom	Document Number: HDMI CONN	Rev: 1A
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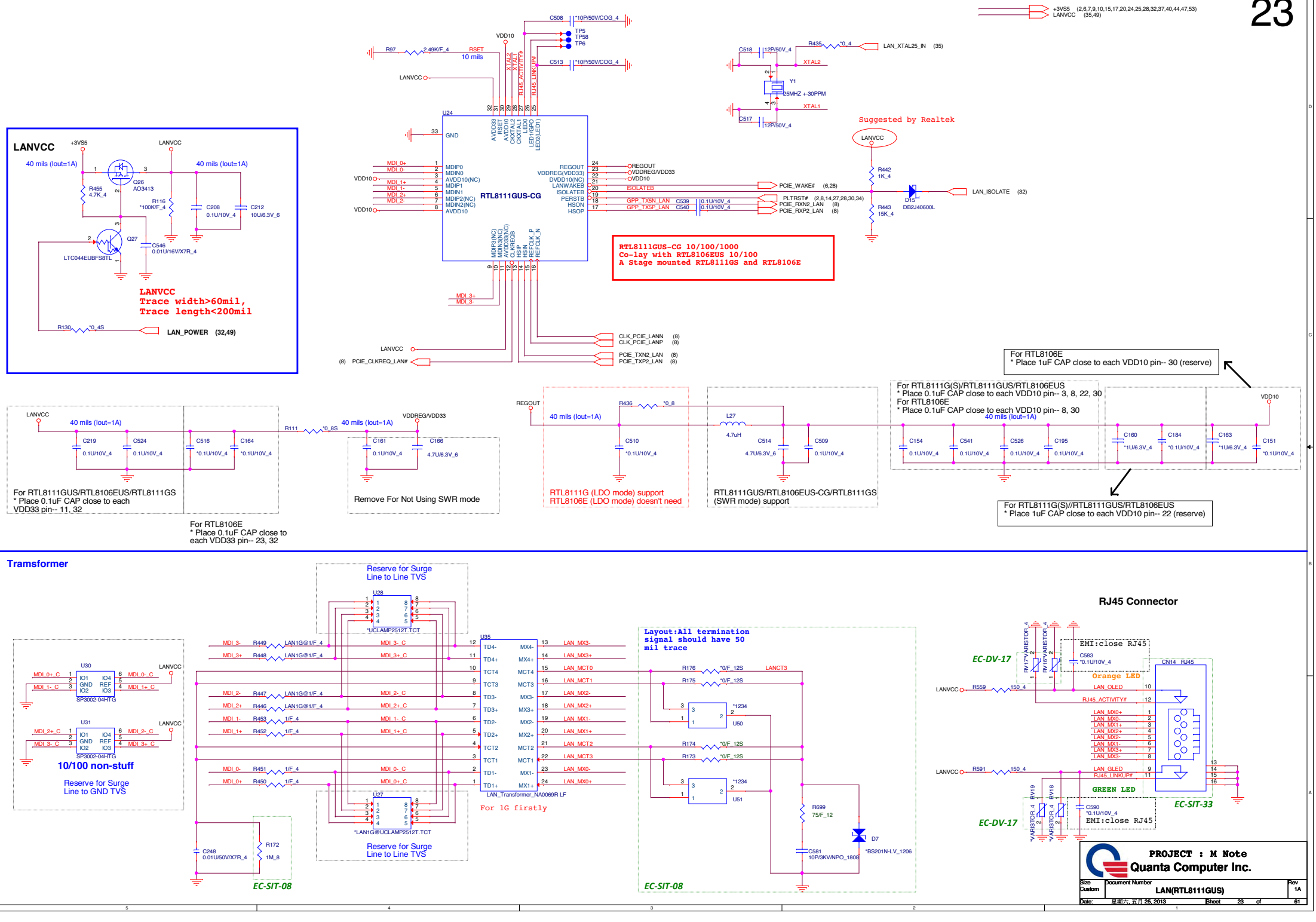
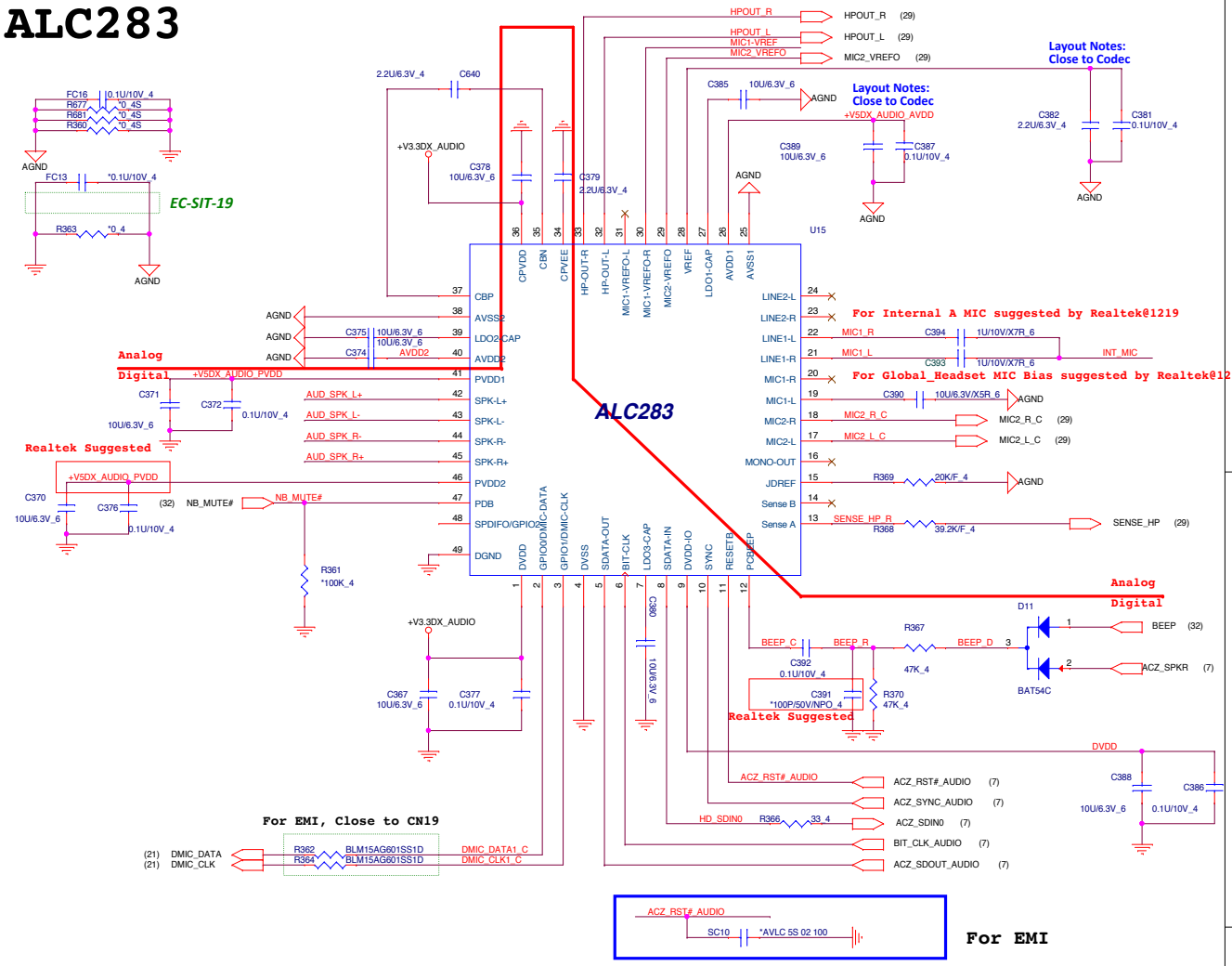
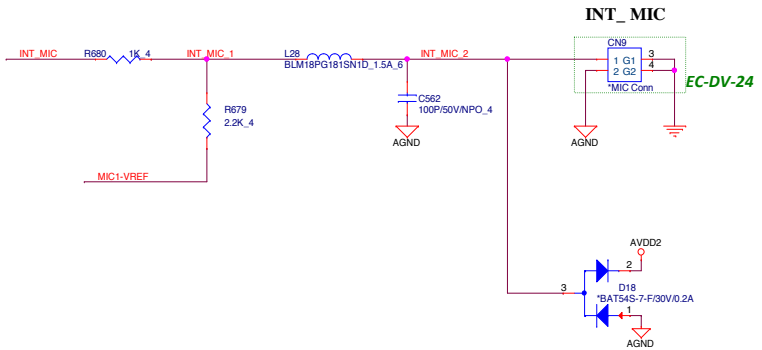

LANVCC
40 mils (Iout=1A)
LANVCC Trace width>60mil, Trace length<200mil
LAN_POWER (32,49)
RTL8111GUS-CG
RTL8111GUS-CG 10/100/1000
Co-lay with RTL8106EUS 10/100
A Stage mounted RTL8111GS and RTL8106E
Suggested by Realtek
For RTL8111GUS/RTL8106EUS/RTL8111GS
* Place 0.1uF CAP close to each VDD33 pin-- 11, 32
For RTL8106E
* Place 0.1uF CAP close to each VDD33 pin-- 23, 32
Remove For Not Using SWR mode
RTL8111G (LDO mode) support
RTL8106E (LDO mode) doesn't need
RTL8111GUS/RTL8106EUS-CG/RTL8111GS (SWR mode) support
For RTL8106E
* Place 1uF CAP close to each VDD10 pin-- 30 (reserve)
For RTL8111G(S)/RTL8111GUS/RTL8106EUS
* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30
For RTL8106E
* Place 0.1uF CAP close to each VDD10 pin-- 8, 30
For RTL8111G(S)//RTL8111GUS/RTL8106EUS
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)
Tramsformer
10/100 non-stuff
Reserve for Surge
Line to GND TVS
Reserve for Surge
Line to Line TVS
For 1G firstly
Layout:All termination signal should have 50 mil trace
EC-SIT-08
RJ45 Connector
EC-DV-17
EC-SIT-33
Orange LED
GREEN LED
EMI:close RJ45
PROJECT : M Note
Quanta Computer Inc.
LAN(RTL8111GUS)

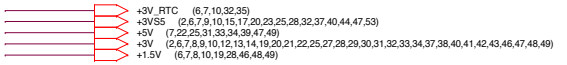
ALC283

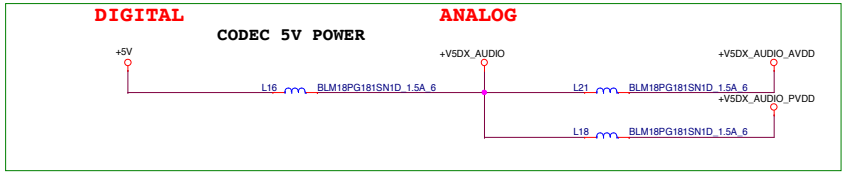


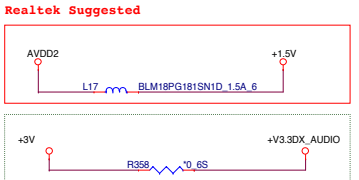
Internal -- A-MIC

Jack insert open

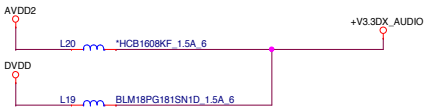




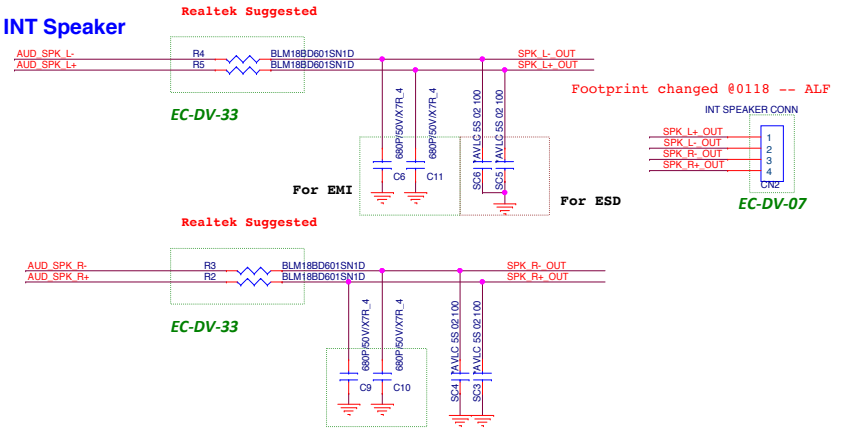




+3.3V_AUDIO_CODEC
Max Current : 419mA

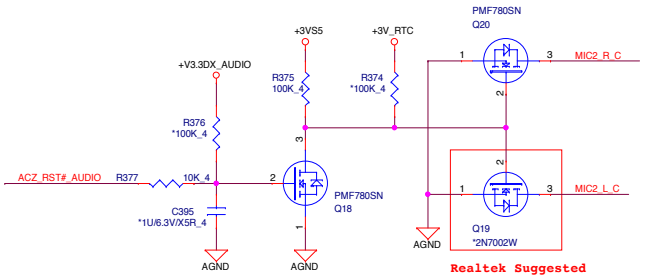


INT Speaker



Grounding circuit for combo jack MIC2_R_C/MIC2_L_C pin

New adding by Realtek suggestion --1219



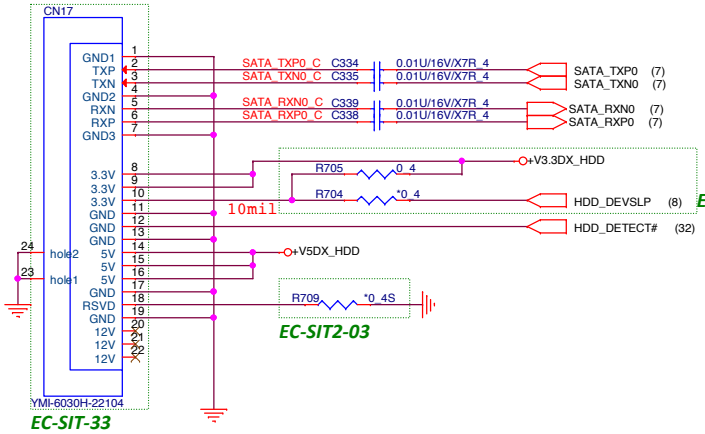
PROJECT : M Note			
Quanta Computer Inc.			
Size: Custom	Document Number: Audio(ALC283)		Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 24 of 61		

HDD

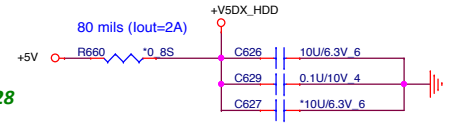
PLACE SATA AC COUPLING
CAPS CLOSE TO Connector

+3VS5 (2,6,7,9,10,15,17,20,23,24,28,32,37,40,44,47,53)
+15V (40,47,48)
+5V (7,22,24,31,33,34,39,47,49)
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,27,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

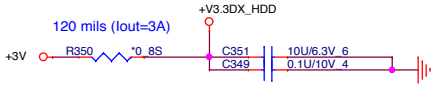
25



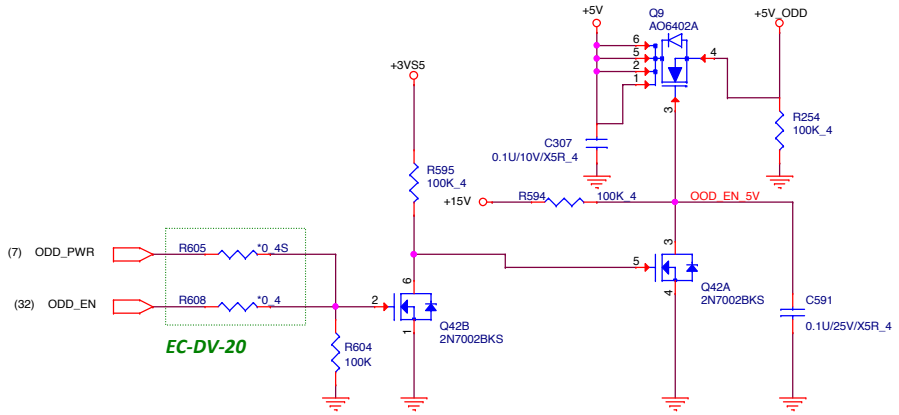
DC Current rating: 2 A (MAX)

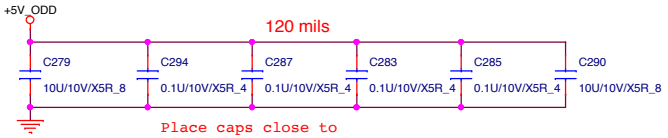


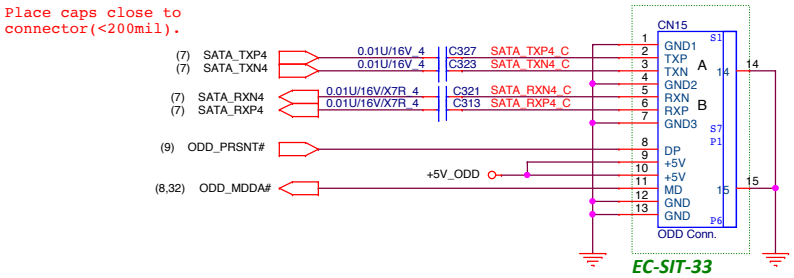
DC Current rating: 3 A (MAX)



SATA ODD Connector.





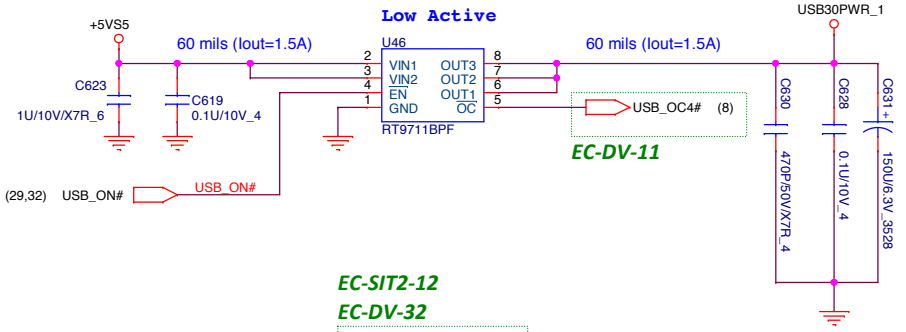


PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA-HDD	1A
Date: 星期六, 五月 25, 2013	Sheet 25 of 61	

+5VS5 (15,19,29,37,38,40,41,42,43,45,46,47,48,49)

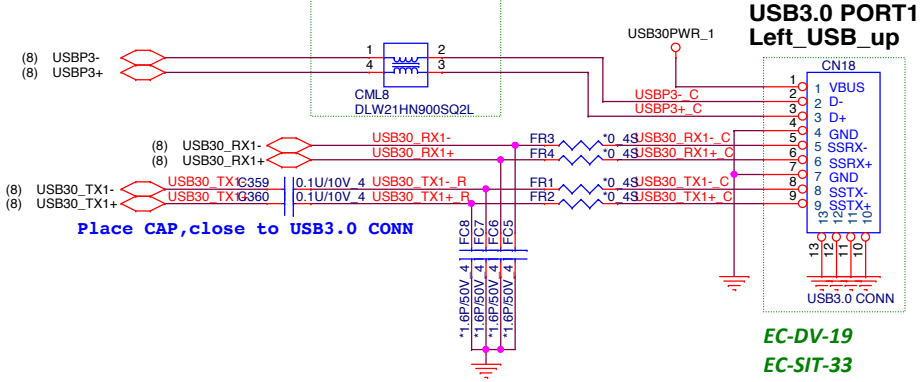
I continuous <1.5A
OC 1.5A
Low Active



EC-DV-11

EC-SIT2-12
EC-DV-32

USB3.0 PORT1
Left_USB_up

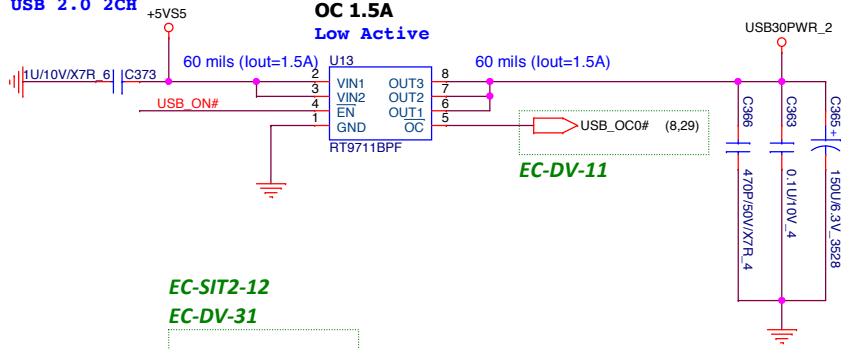


Place CAP,close to USB3.0 CONN

EC-DV-19
EC-SIT-33

FOR USB 2.0 2CH

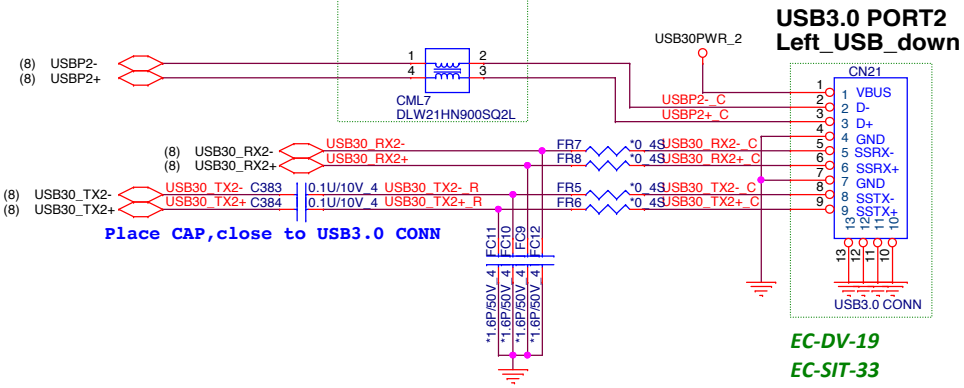
I continuous <1.5A
OC 1.5A
Low Active



EC-DV-11

EC-SIT2-12
EC-DV-31

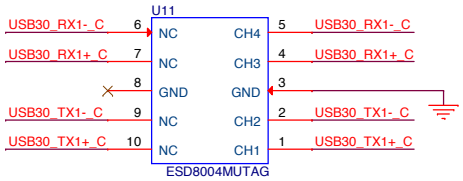
USB3.0 PORT2
Left_USB_down

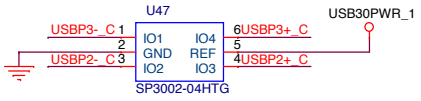


Place CAP,close to USB3.0 CONN

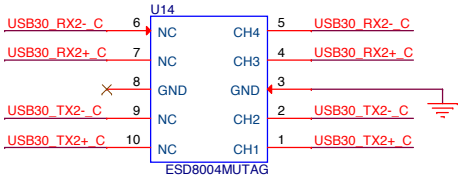
EC-DV-19
EC-SIT-33

ESD





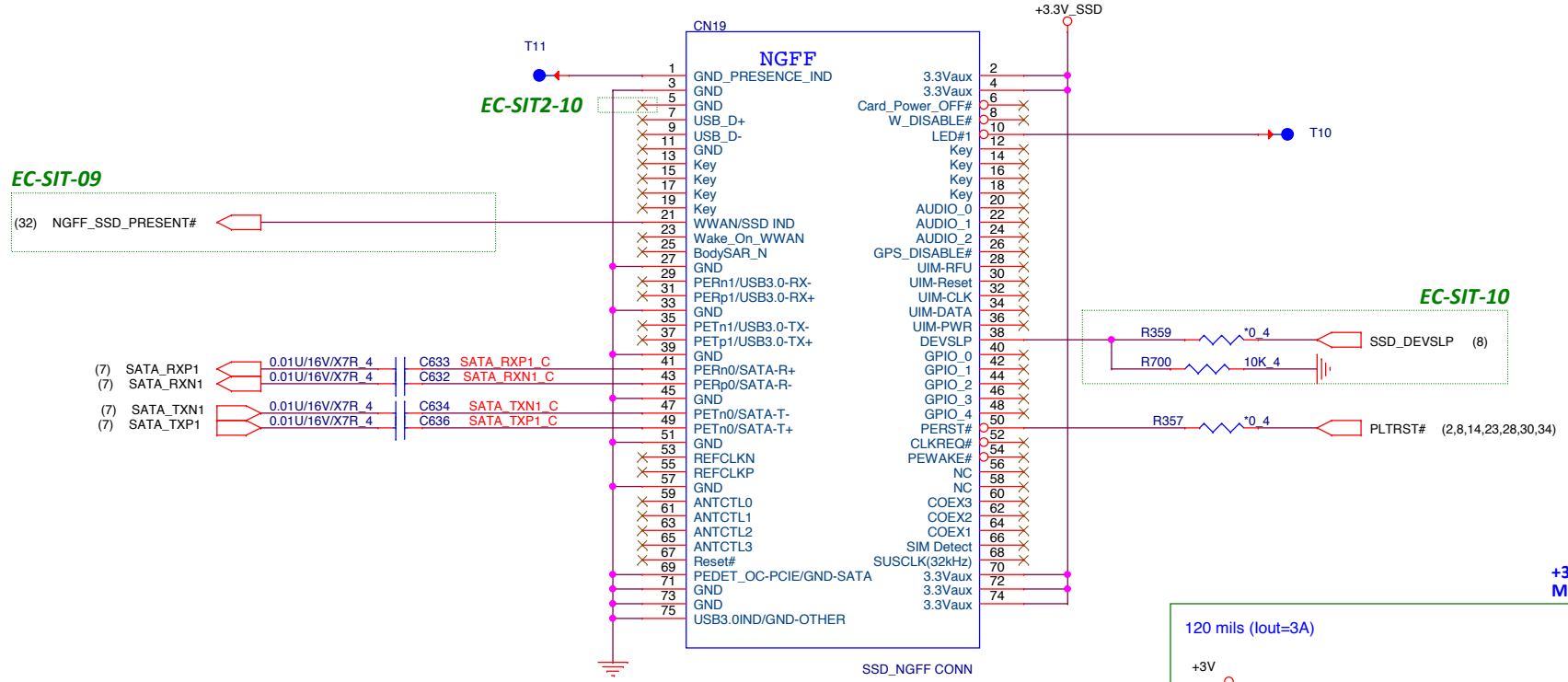
ESD



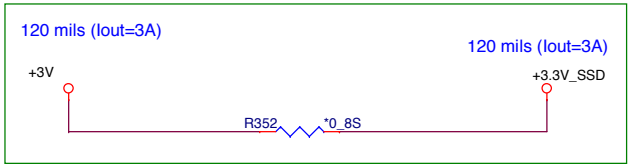
PROJECT : M Note		
Quanta Computer Inc.		
Size: B	Document Number: USB3.0 x2	Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 26 of 61	

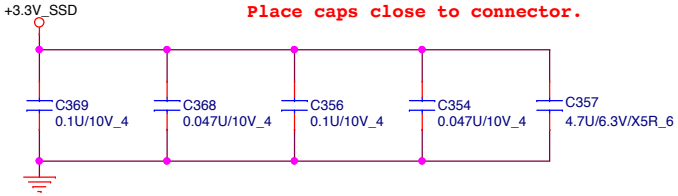
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,28,29,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

NGFF SSD connector



+3.3V_ NGFF_WWAN
Max Current : 2750mA





PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SSD NGFF	1A
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Mini PCIE Wifi/BT connector

+3VS5 (2,6,7,9,10,15,17,20,23,24,25,32,37,40,44,47,53)
+1.5V (6,7,8,10,19,24,46,48,49)

CLK_PCIE_WLAN#
CLK_PCIE_WLAN
C648 *5P/50V_4
C649 *5P/50V_4
EC-SIT-12

CN20
MPCET-S5205-TP52
EC-SIT-33

	1	WAKE#	3.3V_1	2	
	3	RESERVED_1	GND0	4	
	5	RESERVED_2	1.5V_1	6	
	7	CLKREQ#	UIM_PWR	8	
	9	GND1	UIM_DATA	10	
	11	REFCLK-	UIM_CLK	12	
	13	REFCLK+	UIM_RESET	14	
	15	GND2	UIM_VPP	16	
	17	UIM_C8	GND3	18	
	19	UIM_C4	W_DISABLE#	20	
	21	GND4	PERST#	22	
	23	PERn0	3.3VAUX1	24	
	25	PERp0	GND5	26	
	27	GND6	1.5V_2	28	
	29	GND7	SMB_CLK	30	
	31	PETn0	SMB_DATA	32	
	33	PETp0	GND8	34	
	35	GND9	USB_D-	36	
	37	RESERVED_3	USB_D+	38	
	39	RESERVED_4	GND10	40	
	41	RESERVED_5	LED_WWAN#	42	
	43	RESERVED_6	LED_WLAN#	44	
	45	RESERVED_7	LED_WPAN#	46	
	47	RESERVED_8	1.5V_3	48	
	49	RESERVED_9	GND11	50	
	51	RESERVED_10	3.3V_2	52	

+3.3V_MPCIE_WLAN
+1.5V_WLAN
MINICARD_PME#
(8) PCIE_CLKREQ_WLAN#
(8) CLK_PCIE_WLAN#
(8) CLK_PCIE_WLAN
CLK_PCIE_WLAN#
CLK_PCIE_WLAN
LFRAME# (7,32)
LAD0 (7,32)
LAD1 (7,32)
LAD2 (7,32)
LAD3 (7,32)
(7,32) SERIRQ
R664 *0_4
IRQ_SERIRQ_R
TP78
For ESD
RV20 *EGA-0402
WLAN_OFF_R#
PLTRST#
PLTRST# (2,8,14,23,27,30,34)
PCI-Express TX and RX direct to connector
(8) PCIE_RXN1
(8) PCIE_RXP1
(8) PCIE_TXN1
(8) PCIE_TXP1
PCLK_DEBUG
TP51
R662 *0_4S
CLK_33M_DEBUG (8)
USBP10- (8)
USBP10+ (8)
TP52
(7,9) BT_OFF#
D22
DB2J40600L
R661 *0_4S
FC15 *EGA-0402
FC14 *EGA-0402
For ESD / RF
PCLK_DEBUG
C635 15P/50V_4
EC-DV-29
For EMI

+3.3V_MPCIE_WLAN
R672 *10K_4
(6,23) PCIE_WAKE#
*0_4S R678
Q46 LTC044EUBFS8TL
MINICARD_PME#
WLAN
(9,32) SIO_WAKE_SCI#
*0_4 R682
*0_4 R683

Place caps close to connector.
+3.3V_MPCIE_WLAN
C618 0.1U/10V_4
C622 0.047U/10V_4
C642 0.1U/10V_4
C352 0.047U/10V_4
C615 4.7U/6.3V/X5R_6

WLAN_OFF_R#
D23 DB2J40600L
WLAN_ON/OFF# (9)
R668 *0_4

+3.3V_ NGFF_WLAN
Max Current : 1000mA
Don't Support AOAC..
EC-SIT2-05
+3VS5
40 mils (Iout=1A)
+3.3V_MPCIE_WLAN
+3V
40 mils (Iout=1A)
Q44 AOS3413
R667 4.7K_4
R665 *0_6
15mils
R365 22_8
R663 *100K/F_4
C637 0.1U/10V_4
Q16 PMF780SN
Support AOAC..
EC
(32) EC_WLAN_EN
D24 DB2J40600L
(6) WLAN_AOAC_ON
D25 *RB500V-40
Q45 LTC044EUBFS8TL
C639 0.01U/16V/X7R_4
PCH

+1.5V_WLAN
C617 0.01U/16V/X7R_4
C621 0.1U/10V_4
C625 10U/6.3V_6
+1.5V_WLAN
+1.5V
R345 *0_6S
40 mils (Iout=1A)

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Wifi/BT MiniPCIE	1A
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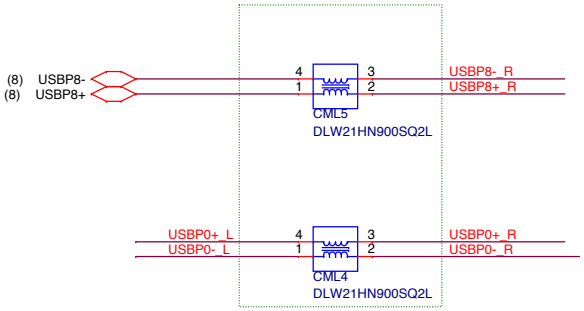
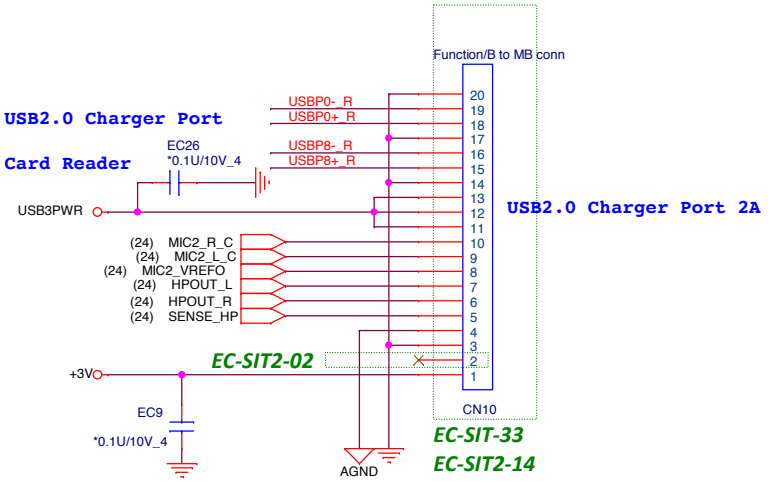
3.3_ALW
+5VS5 (15,19,26,37,38,40,41,42,43,45,46,47,48,49)
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,30,31,32,33,34,37,38,40,41,42,43,46,47,48,49)



EC-SIT-23
EC-SIT2-12

USB2.0 Charger Port
Card Reader

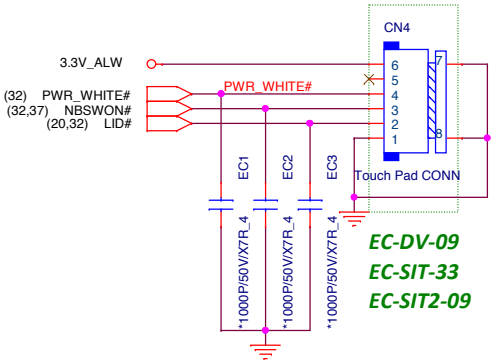


EC-SIT2-02

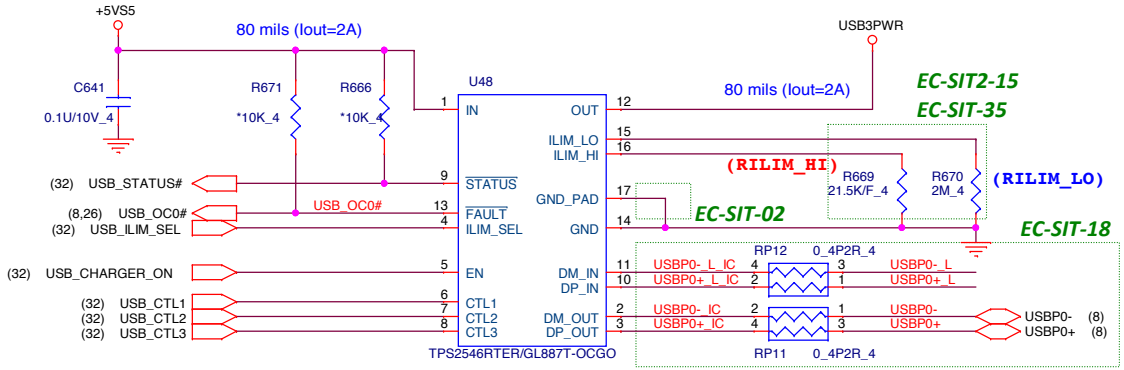
USB2.0 Charger Port 2A

EC-SIT-33
EC-SIT2-14

Power/B CONN



EC-DV-09
EC-SIT-33
EC-SIT2-09



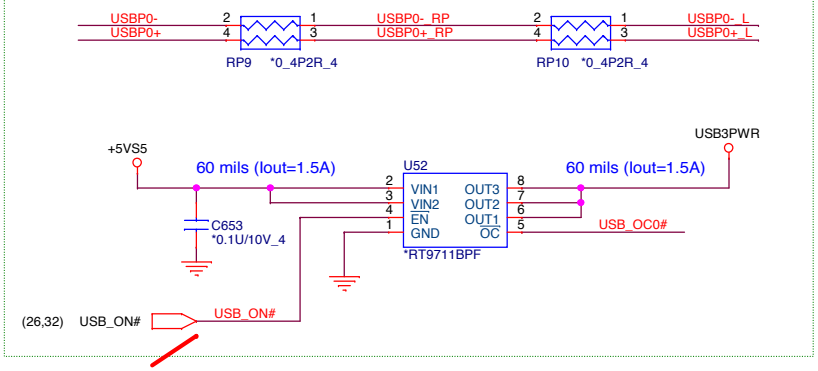
EC-SIT2-15
EC-SIT-35
EC-SIT-02
EC-SIT-18

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

EC-SIT-18

For BM6 without AOU5 function



Confirmed with SW team already!!

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB2.0–Audio Jack Conn	1A
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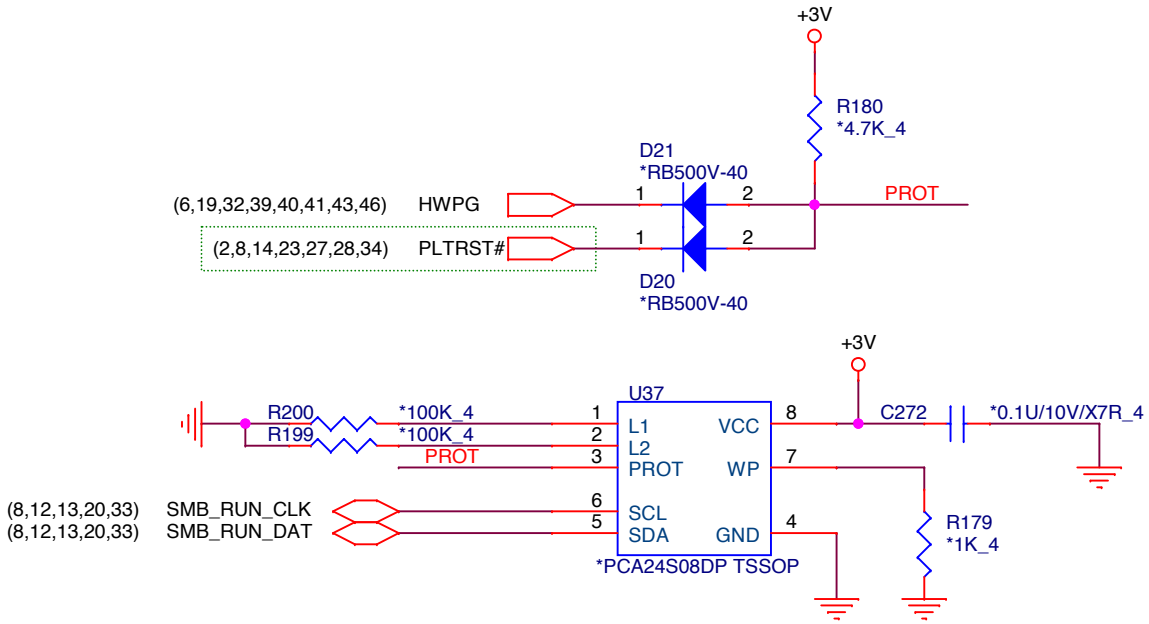
RFID

+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,31,32,33,34,37,38,40,41,42,43,46,47,48,49)

30



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
A	RFID	1A
Date: 星期六, 五月 25, 2013	Sheet 30 of 61	

+5V (7,22,24,25,33,34,39,47,49)
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,30,32,33,34,37,38,40,41,42,43,46,47,48,49)

+5V
DB2J40600L
D14
+5V_CRT2
CRT_VCC_R
F1
FUSE1.1A_8V_POLY
C506
0.1U/10V/X5R_4

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

(6) CRT_R
(6) CRT_G
(6) CRT_B
L10 BLM15BA470SS1D
L9 BLM15BA470SS1D
L7 BLM15BA470SS1D
CRT_R1
CRT_G1
CRT_B1
R129 150/F_4
R123 150/F_4
R118 150/F_4
C240 22P/50V_4
C229 22P/50V_4
C215 22P/50V_4
C218 22P/50V_4
C230 22P/50V_4
C246 22P/50V_4
TP17
VGA_DDC_DAT_RT C235 *470P/50V_4
CRTHSYNC C507 10P/50V_4
CRTVSYNC C505 10P/50V_4
VGA_DDC_CLK_RT C207 *470P/50V_4
CRT CONN
CN13

EC-DV-30
EC-SIT-33

ESD PROTECTION

New Adding @ 1203

U29
CRT_G1
CRTHSYNC
IO1 IO4 GND REF IO2 IO3
CRT_R1
VGA_DDC_DAT_RT
SP3002-04HTG

U26
CRTVSYNC
VGA_DDC_CLK_RT
IO1 IO4 GND REF IO2 IO3
CRT_B1
SP3002-04HTG

CRT_VCC_R
C245 *0.1U/10V/X7R_4

+5V +3V
C544 0.1U/10V_4
C197 0.1U/10V_4
DDCCLK R82 2.7K_4
DDCDATA R83 2.7K_4

U23
+5V_CRT2
+5V
C190 0.22U/25V_6
CRT_BYP
+3V
VCC_SYNC
VCC_DDC
BYP
VCC_VIDEO
VIDEO_1
VIDEO_2
VIDEO_3
GND
SYNC_OUT2
SYNC_OUT1
SYNC_IN2
SYNC_IN1
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
TPD7S019

CRT_R1
CRT_G1
CRT_B1
CRT_VSYNC1 R437 22_4 CRTVSYNC
CRT_HSYNC1 R84 22_4 CRTHSYNC
VSYNC_COM
HSYNC_COM
VSYNC_COM (6)
HSYNC_COM (6)
DDCCLK
DDCDATA
DDCCLK (6)
DDCDATA (6)
VGA_DDC_CLK_RT
VGA_DDC_DAT_RT
+5V_CRT2
R85 2.2K_4
R86 2.2K_4

For Checklist 0826

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
B	CRT	1A
Date: 星期六, 五月 25, 2013	Sheet 31 of 61	

IT8587

For detecting the RTC power level

EC-SIT-27

For EMI, Close U16. pin74

Layout Note:
Place all capacitors close to IT8512.

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Layout Note:
net "3VALW" and "RTC_VCC" minimum trace width 12mils.

EC-SIT-16

Layout Note:
Place this test point on top side

EC-DV-25

FOR DEEP S3

FOR EC auto load code
FOR DEEP S3

EC-SIT-14

EC-SIT-13

EC-SIT2-04

for GC6 support

FOR DEEP S3

EC-SIT-04

EC-DV-12

EC-SIT-09

EC-SIT2-16

for ODD used --1204

(For PLL Power)

FOR DEEP S3

For EC E-flash(embedded flash) auto load code

Note:
H01 use IT8587 with 128K-byte e-flash
Auto load code condition:
1. Let PCH SPI interface in High-Z state.
2. RSMRST# pull low
   (PCH SPI pins are tri-stated prior to RSMRST# de-assertion)
3. EC pin 100(GPG2) pull high(force EC load code)
4. Supply power to SPI flash ROM,PCH(VCCSPI,+1.05V_SUS) and EC

Moved the TEMP_ALERT# & VGA_OVT# to PCH -1221

EC-SIT2-04

For ESD

EC-SIT-15

POWER SWITCH

POWER SWITCH For Bring Up Test

AOU5 function select setting

	With	Without
Stuff	Ra (Hi) Default	Rb (Lo)

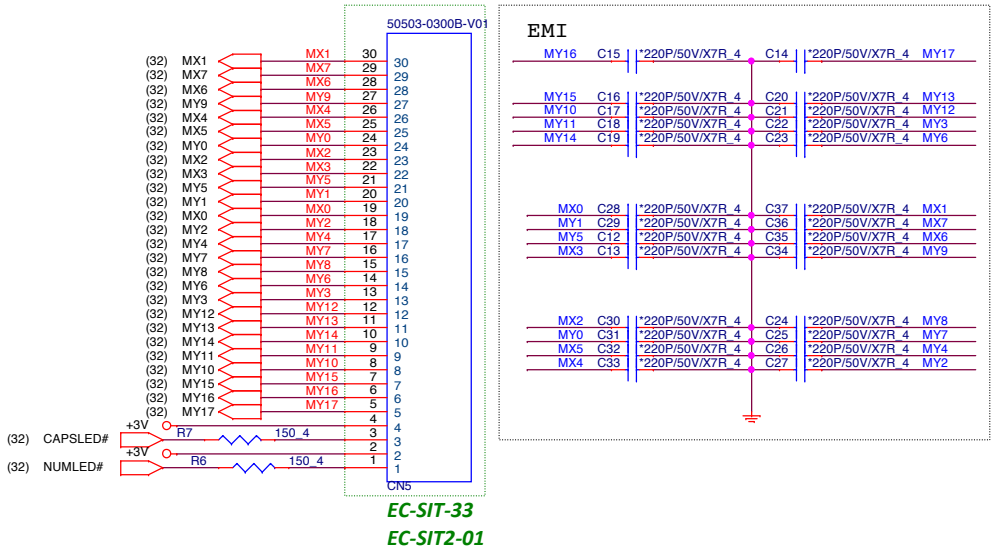
EC-SIT-20

PROJECT : M Note
Quanta Computer Inc.

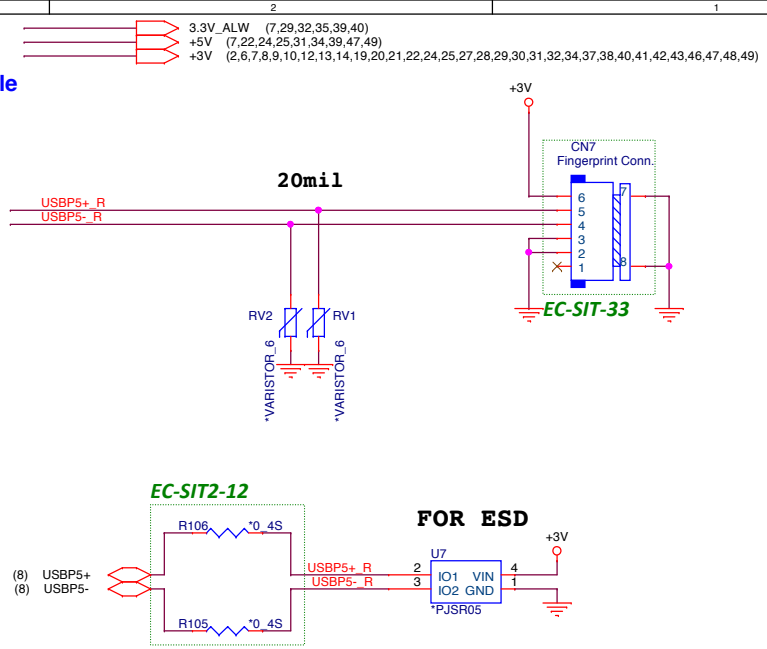
Size	Document Number	Rev
Custom	KBC IT8587	1A

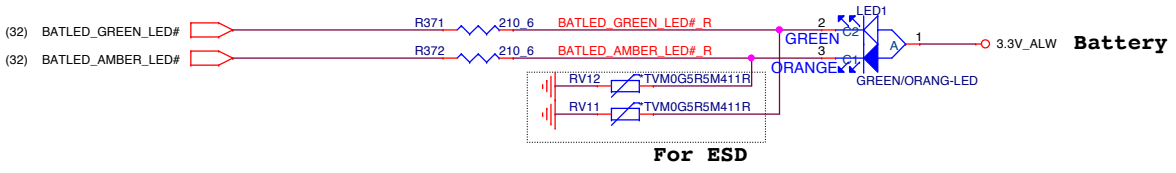
Date: 星期六, 五月 25, 2013 Sheet 32 of 61

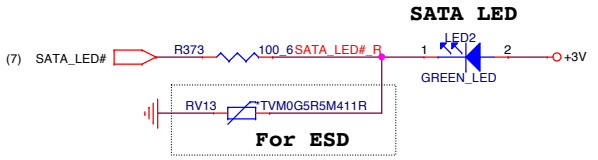
KEYBOARD



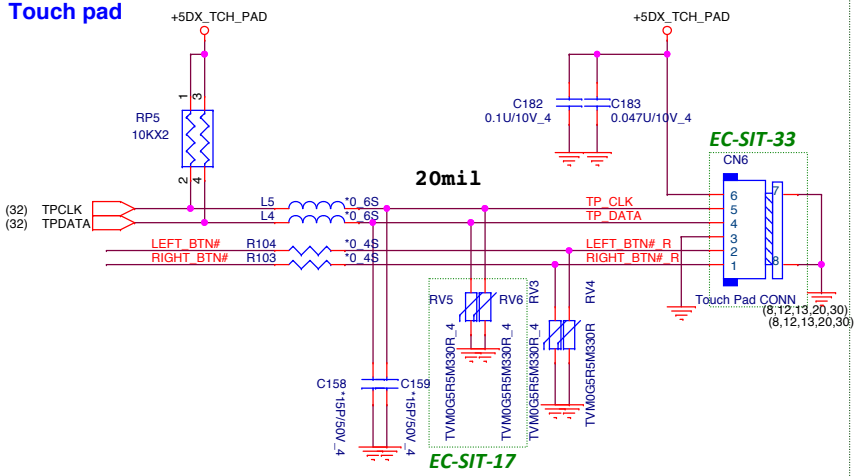
Fingerprint module

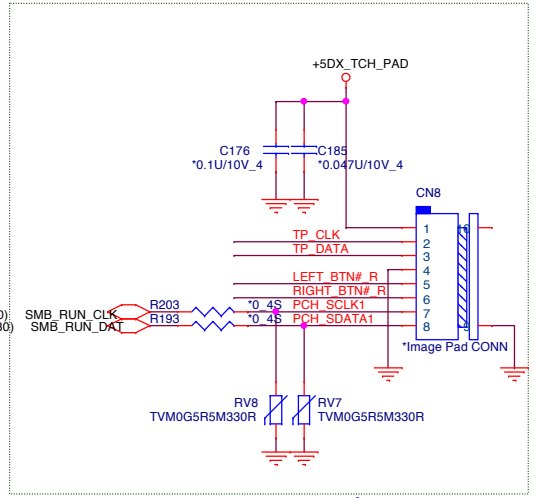


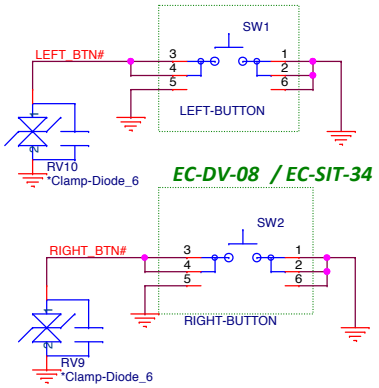




Touch pad







Profile Sensor 6Pin (Default)

Voltage: +5V
Max Current : 50mA

Image Sensor 8 Pin

Voltage: +3V
Max Current : 50mA

Quanta Computer Inc.	PROJECT : M Note	
Size: Custom	Document Number: KB/TP/LID	Rev: 1A
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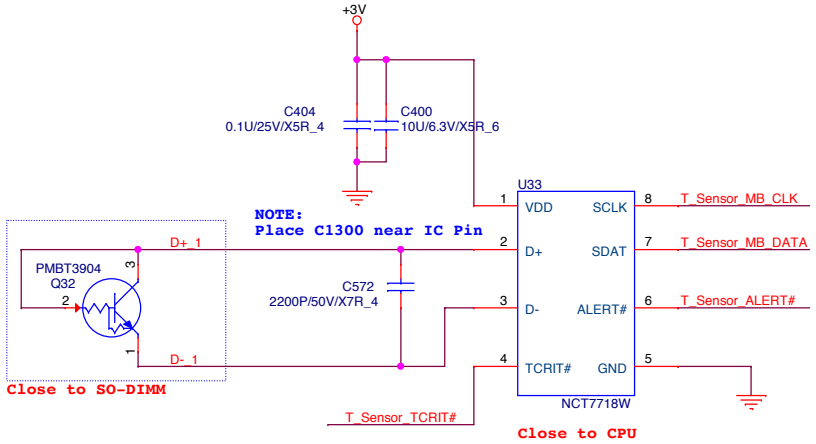
FAN CONTROL & Thermal IC

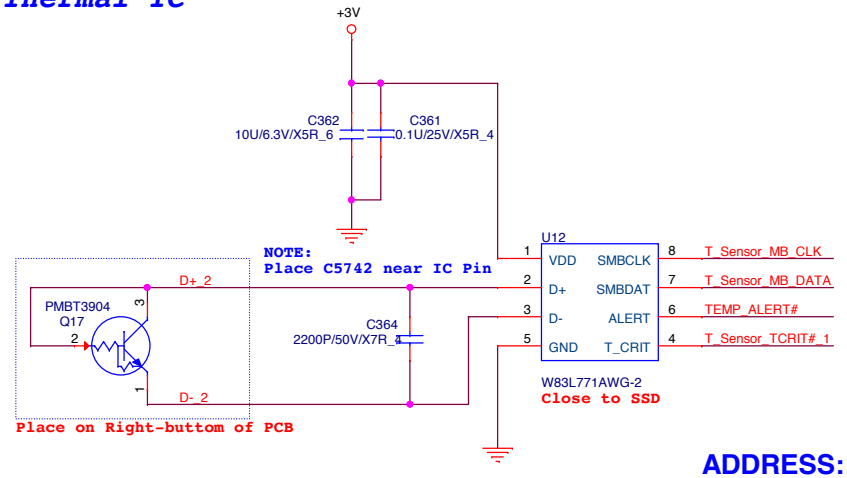
+5V (7,22,24,25,31,33,39,47,49)
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,37,38,40,41,42,43,46,47,48,49)

Thermal IC(HW Shutdown)

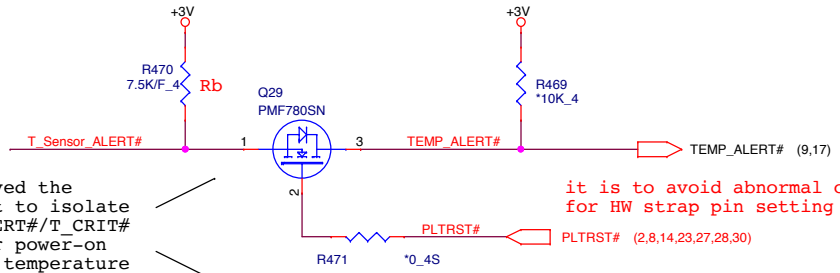


ADDRESS: 98

Thermal IC

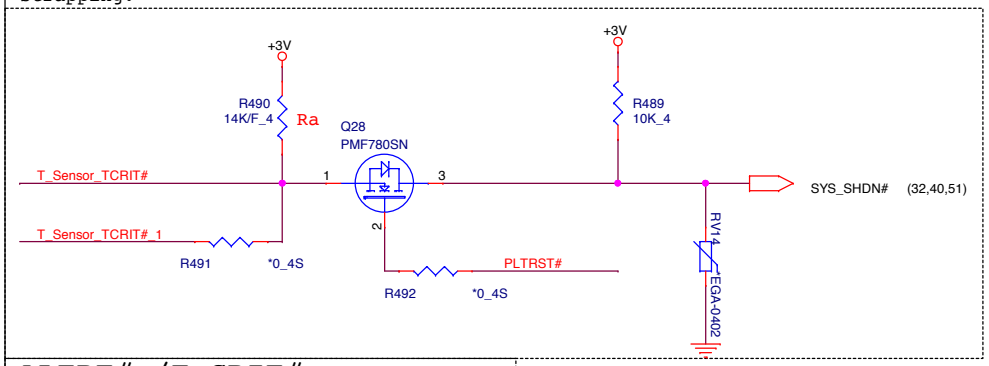


ADDRESS: 9A



*Reserved the circuit to isolate the ALERT#/T_CRIT# pin for power-on T_CRIT temperature strapping.

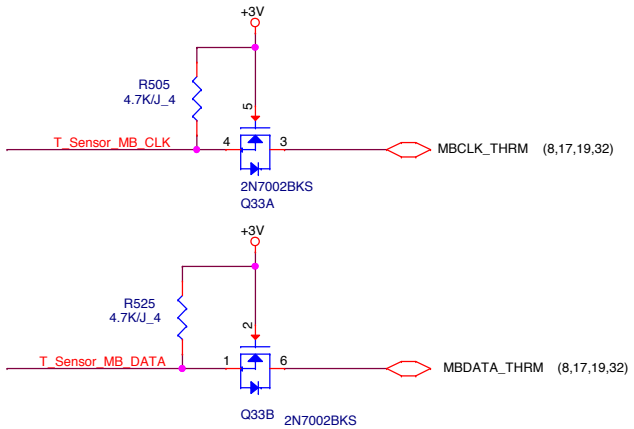
it is to avoid abnormal operation when power on within 100ms for HW strap pin setting HW Shut-down Temp. 109 ℃

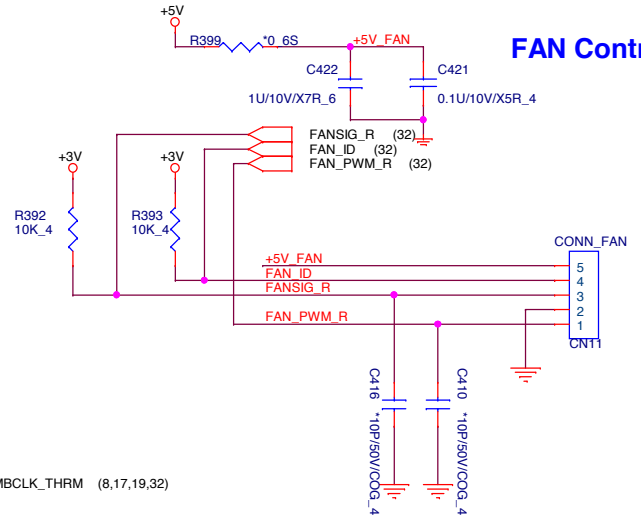


ALERT# /T_CRIT# Pull-up Resistor

Rb \ Ra	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point





FAN Controller

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN/Thermal	1A

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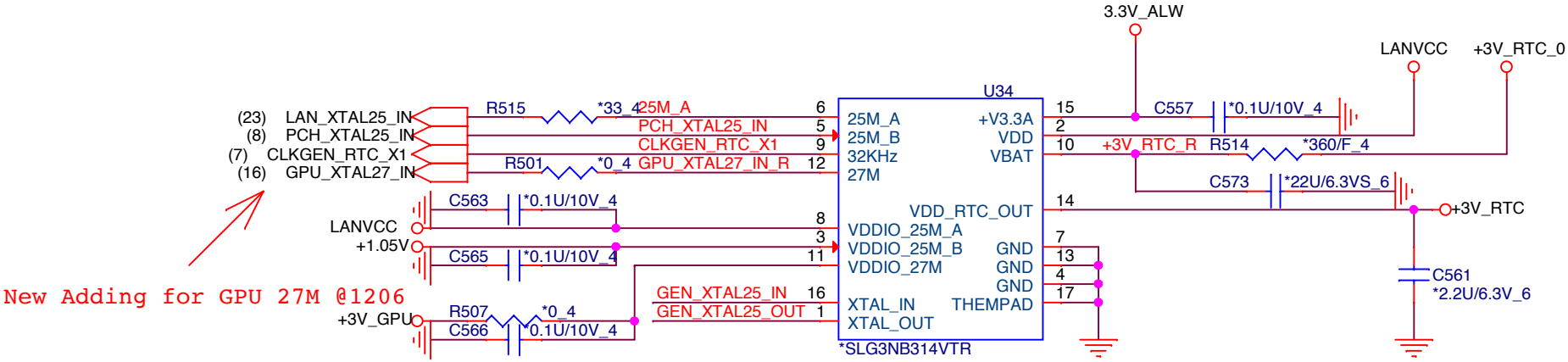
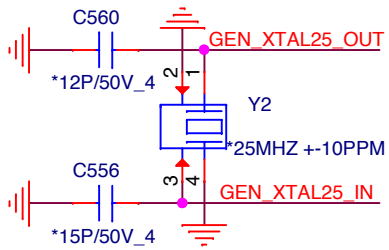
Green CLK Circuitry

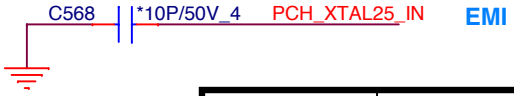
+3V_RTC_0 (7,32)
+3V_RTC (6,7,10,24,32)
3.3V_ALW (7,29,32,33,39,40)
+3V_GPU (14,17,38,45,48,50)
LANVCC (23,49)
+1.05V (2,4,9,10,43,48,49,53)

+3V_RTC_0,+3V_RTC_R,+3V_RTC..
20mils width(min)



New Adding for GPU 27M @1206





	U63 P/N
DIS	AL000314000
UMA	AL3NB244000

DIS
32Kx1+25M*2+27Mx1

UMA
32Kx1+25M*2

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
A	Green Clock	1A
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PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Blank	1A

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+5VS5 (15,19,26,29,38,40,41,42,43,45,46,47,48,49)
+3VS5 (2,6,7,9,10,15,17,20,23,24,25,28,32,40,44,47,53)
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,30,31,32,33,34,38,40,41,42,43,46,47,48,49)

If don't need the USB3.0 repeater @1219

(8,37) USB30_TX3-
(8,37) USB30_TX3+
RP3 *0_4P2R_4
USB30_TX3-_R
USB30_TX3+_R
RP1 *0_4P2R_4
RE_USB30_TX3-
RE_USB30_TX3+

(8,37) USB30_RX3-
(8,37) USB30_RX3+
RP4 *0_4P2R_4
USB30_RX3-_R
USB30_RX3+_R
RP2 *0_4P2R_4
RE_USB30_RX3-
RE_USB30_RX3+

+3VS5
C41 1U/6.3V_4
C42 0.1U/10V_4
C51 2.2U/10V_6
C50 470P/50V_4

USB3.0 re-driver IC

U2
SN65LVPE502ARGER

(8,37) USB30_TX3-
(8,37) USB30_TX3+
C52 0.1U/10V_4 USB30_TX3-_C
C53 0.1U/10V_4 USB30_TX3+_C
(8,37) USB30_RX3-
(8,37) USB30_RX3+
C54 0.1U/10V_4 USB30_RX3-_C
C55 0.1U/10V_4 USB30_RX3+_C
RX1-
RX1+
TX2-
TX2+
VCC
VCC
EQ1
EQ2
DE1
DE2
OS1
OS2
TX1-
TX1+
RX2-
RX2+
EN_RXD
CM
NC1
NC2
GND
GND
GND
GND
RE_USB30_TX3-
RE_USB30_TX3+
RE_USB30_RX3-
RE_USB30_RX3+
R38 *4.99K/F_4
R33 4.99K/F_4
R31 *4.99K/F_4
R32 4.99K/F_4
+3VS5
REXT
Debug
B_DE1
A_DE1

New adding @1124

EC-SIT-03

Follow Intel Design Guide, Put AC CAP on DB

Cable Docking Conn.
CN12

(2) ExDPP0_N
(2) ExDPP0_P
(2) ExDPP1_N
(2) ExDPP1_P
(6) ExDP_AUXN
(6) ExDP_AUXP
ExDP_AUXN
ExDP_AUXP
Docking_HPD
CONFIG1
+3V
(39) DOCK_CONSUMP
(32) Dock_Detect#
(29,32) NBSWON#
+5VS5
EC13 *1000P/50V/X7R_4
Confirmed Lenovo!!

EC-SIT2-12
R12 *0_4S
R13 *0_4S
(8) USBP7-
(8) USBP7+
USBP7-_C
USBP7+_C
RE_USB30_RX3-
RE_USB30_RX3+
C645 0.1U/10V_4
C644 0.1U/10V_4
RE_USB30_RX3-_C
RE_USB30_RX3+_C
RE_USB30_TX3-
RE_USB30_TX3+
C647 0.1U/10V_4
C646 0.1U/10V_4
RE_USB30_TX3-_C
RE_USB30_TX3+_C
FC1 *1.6P/50V_4
FC2 *1.6P/50V_4
FC3 *1.6P/50V_4
FC4 *1.6P/50V_4

EC-SIT-11
EC-DV-06

+3VS5
EC-SIT-31
R27 *4.99K/F_4
R28 *4.99K/F_4
R17 *4.99K/F_4
R25 *4.99K/F_4
R16 4.99K/F_4
R20 4.99K/F_4
R22 *4.99K/F_4
R29 *4.99K/F_4
R18 *4.99K/F_4
R26 *4.99K/F_4
R15 *4.99K/F_4
R21 *4.99K/F_4
EQ1
EQ2
DE1
DE2
OS1
OS2

EC-SIT-03
Reserve some Rs for Parade USB3.0 re-driver.
R692 *4.99K/F_4 REXT
+3VS5
Debug R693 *4.7K_4
R697 0_4 B_DE1 R694 *4.7K_4
R696 0_4 A_DE1 R695 *4.7K_4
for TI, MUST

+3V
C452 1U/6.3V_4
C454 0.1U/10V_4
+5VS5
C444 1U/6.3V_4
C440 0.1U/10V_4
Place CAP,close to CN1304

+3V
R11 *100K_4 ExDP_AUXN
R10 *100K_4 ExDP_AUXP
Follow Docking Design Guide, Pull up/down on system

ESD

U1
USBP7-_C
USBP7+_C
IO1 VIN
IO2 GND
+5VS5
*PJSR05

U20
RE_USB30_RX3-_C
RE_USB30_RX3+_C
RE_USB30_TX3-_C
RE_USB30_TX3+_C
NC NC GND NC NC
CH4 CH3 GND CH2 CH1
*AZ1045-04F
EC-SIT-11

+3V
R30 1M_4
(6) ExDP_HPD
Q1 2N7002BK
Docking_HPD
R39 20K/F_4

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cable Docking	1A
Date: 星期六, 五月 25, 2013	Sheet 37 of 61	

keyboard Lockhole

HOLE11
*h-c295ic131d91p2

CPU HOLE

HOLE5
*INTEL-CPU-BKT3

GPU Bracket HOLE

HOLE4 *H-C142D142N
HOLE9 *H-C142D142N
HOLE10 *H-C142D142N

HDD Right Side's Lockhole

HOLE12
*hg-c295ic150d110p2

NGFF HOLE

HOLE21
FBAJ2003010

PCH HOLE

HOLE19 *MBBQ1001011
HOLE20 *MBBQ1001011

HDD Hole

HOLE13
*O-BM5-1

MB's LockHole

HOLE2 *hg-c295d91p2
HOLE8 *hg-c295d91p2
HOLE3 *hg-c295d91p2

With NUT

HOLE18
FBKN2020011

NPTH Hole

PAD1 *spad-re320x70np
HOLE7 *h-c87d87n
HOLE15 *h-c87d87n
HOLE1 *h-c87d87n

EC-DV-16

HOLE17 *hg-c295d110p2
HOLE6 *hg-c295d110p2
HOLE16 *hg-c295d91p2
HOLE14 *hg-c295d110p2

HOLE22
*hg-c295d110p2

EC-DV-13

EMI

VIN (20,39,40,41,42,43,45,46,51)
+5VS5 (15,19,26,29,37,40,41,42,43,45,46,47,48,49)
+1.35VSUS (2,4,12,13,41,49)
+3V (2,6,7,8,9,10,12,13,14,19,20,21,22,24,25,27,28,29,30,31,...,41,42,43,46,47,48,49)
+3V_GPU (14,17,35,45,48,50)
+1.5V_GPU (14,15,18,48,50)

+5VS5: C443 C49 C358 C638 C40 C579 C346 — 0.1U/10V_4

+3V: C597 C177 C420 C593 C60 C269 C594 C225 C574 — 0.1U/10V_4

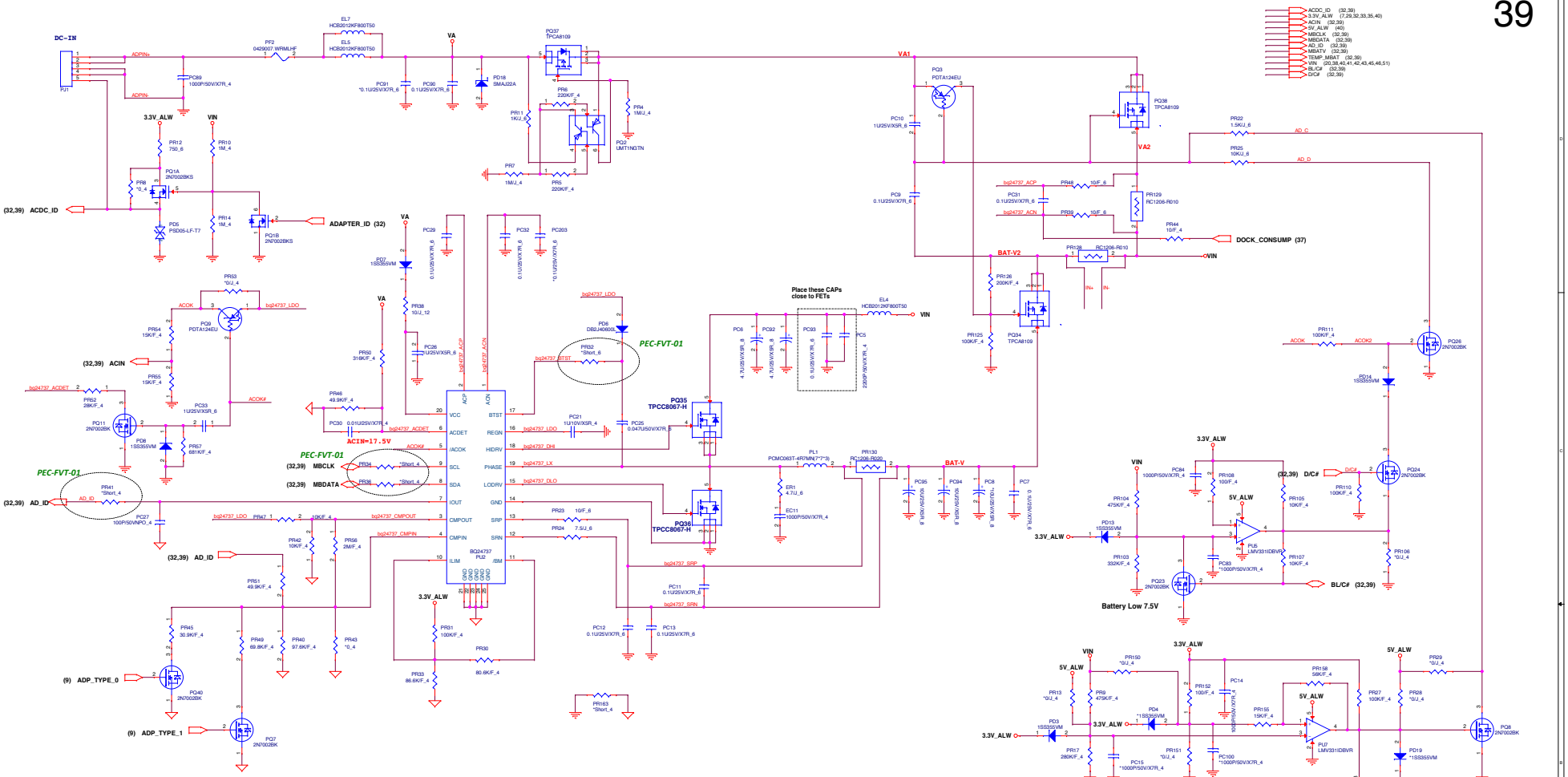
VIN: C407 C3 C598 C350 C262 C135 C451 — 0.1U/25V/X7R_6

+1.35VSUS: C261 C142 C576 C85 — 0.1U/10V_4
+3V_GPU: C495 C273 — 0.1U/10V_4
+1.5V_GPU: C263 C494 — 0.1U/10V_4

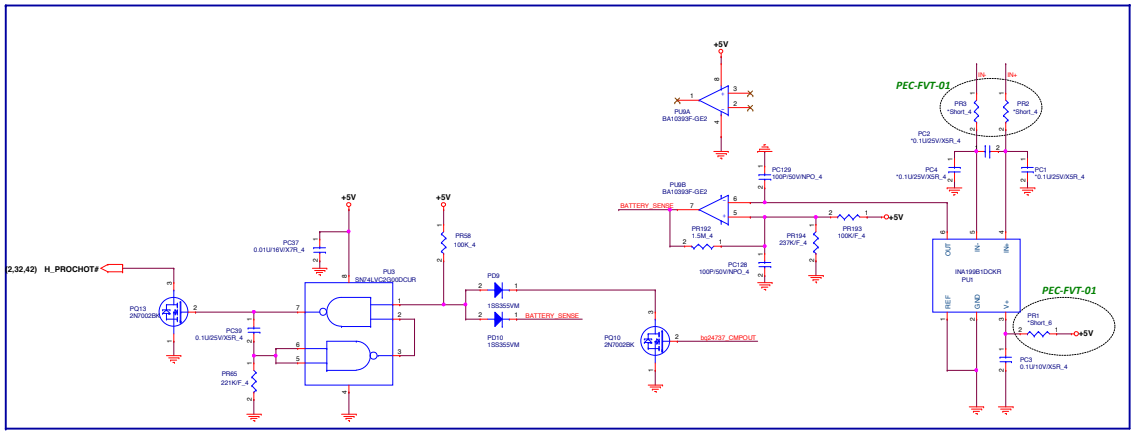
PROJECT : M Note
Quanta Computer Inc.

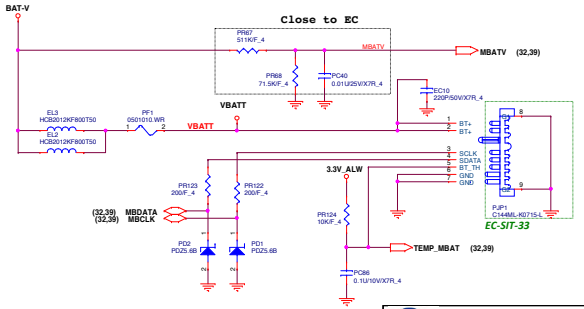
Size	Document Number	Rev
B	Screw Hole/EMI	1A

Date: 星期六, 五月 25, 2013 Sheet 38 of 61

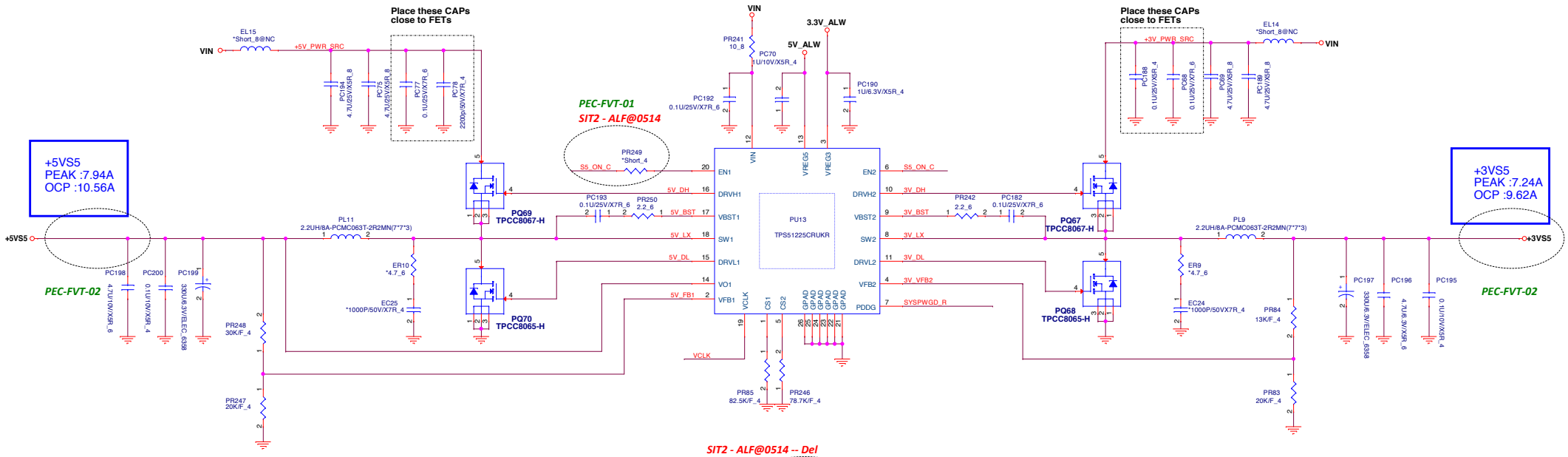


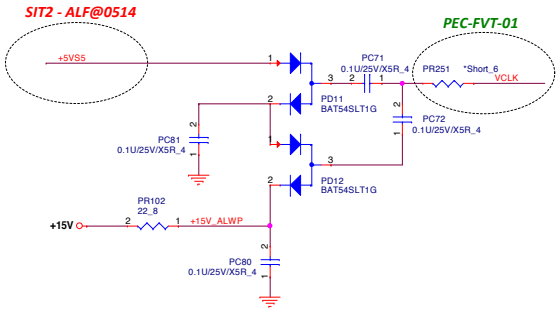
10ms one-shot circuit

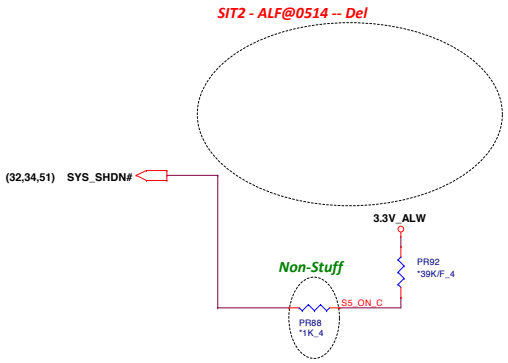


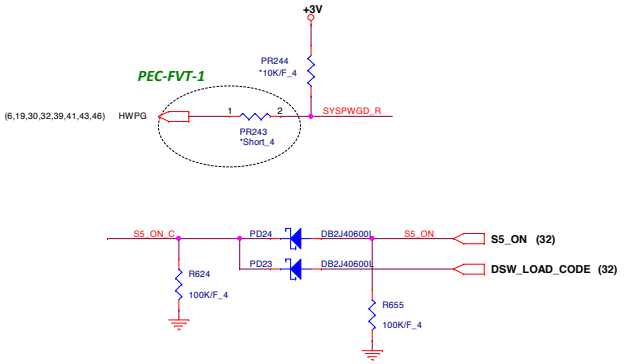


PROJECT : M Note
Quanta Computer Inc.
Size: Custom | Document Number: Charger (BQ24737) | Rev: 1A
Date: 星期六, 五月 25, 2013 | Sheet 39 of 61

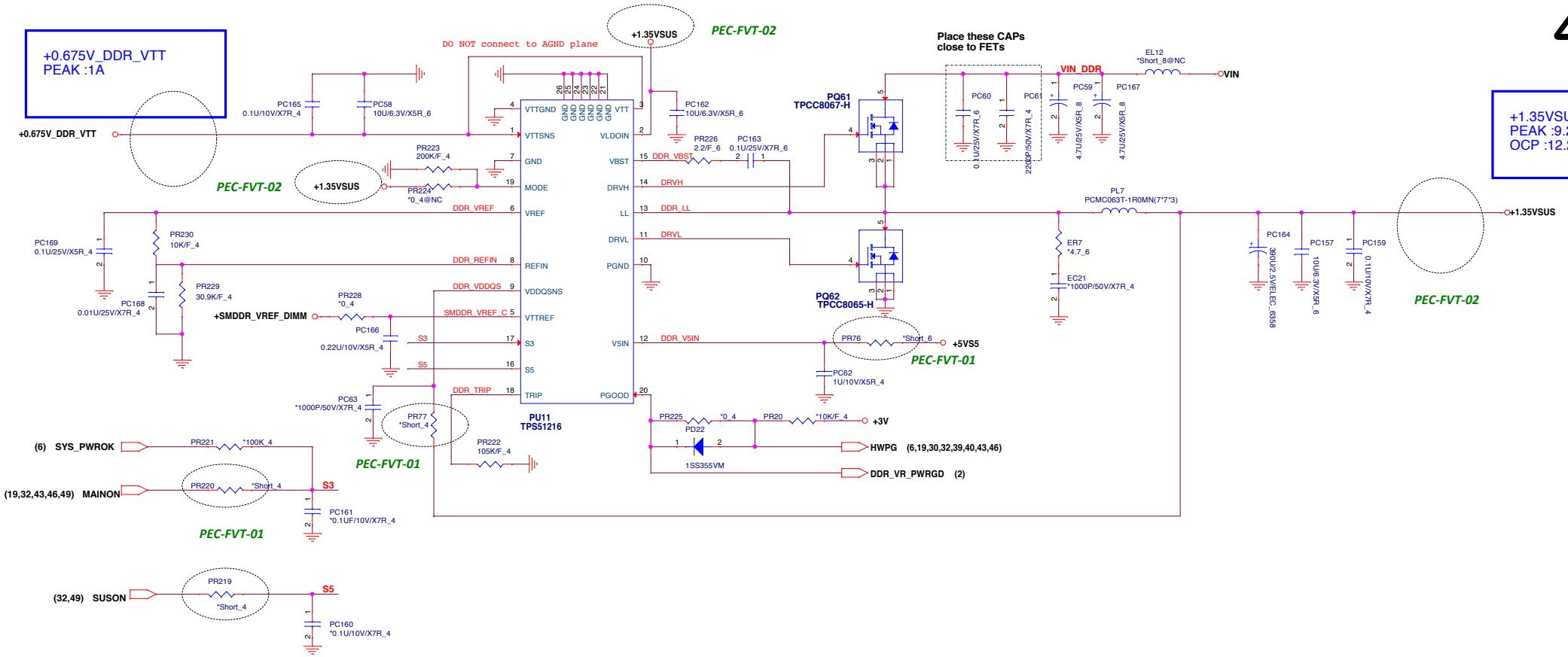








Quanta Computer Inc.	PROJECT : M Note	
Size: Custom	Document Number: System Power(TPS51225)	Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 40 of 61	


+0.675V_DDR_VTT
PEAK :1A
+1.35VSUS
PEAK :9.2A
OCP :12.23A
DO NOT connect to AGND plane
Place these CAPs close to FETs
PEC-FVT-02
PEC-FVT-01
PU11
TPS51216
PQ61
TPCC8067-H
PQ62
TPCC8065-H
VIN_DDR
VIN
PL7
PCMC063T-1R0MN(7*7*3)
DDR_VREF
DDR_REFIN
DDR_VDDQS
SMDDR_VREF_C
DDR_TRIP
DDR_VBST
DDR_LL
DDR_V5IN
+SMDDR_VREF_DIMM
+5VS5
+3V
HWPG (6,19,30,32,39,40,43,46)
DDR_VR_PWRGD (2)
(6) SYS_PWROK
(19,32,43,46,49) MAINON
(32,49) SUSON
S3
S5
1SS355VM
PROJECT : M Note
Quanta Computer Inc.
DDR Power (TPS51216)
Size Custom
Document Number
Rev 1A
Date: 星期六, 五月 25, 2013
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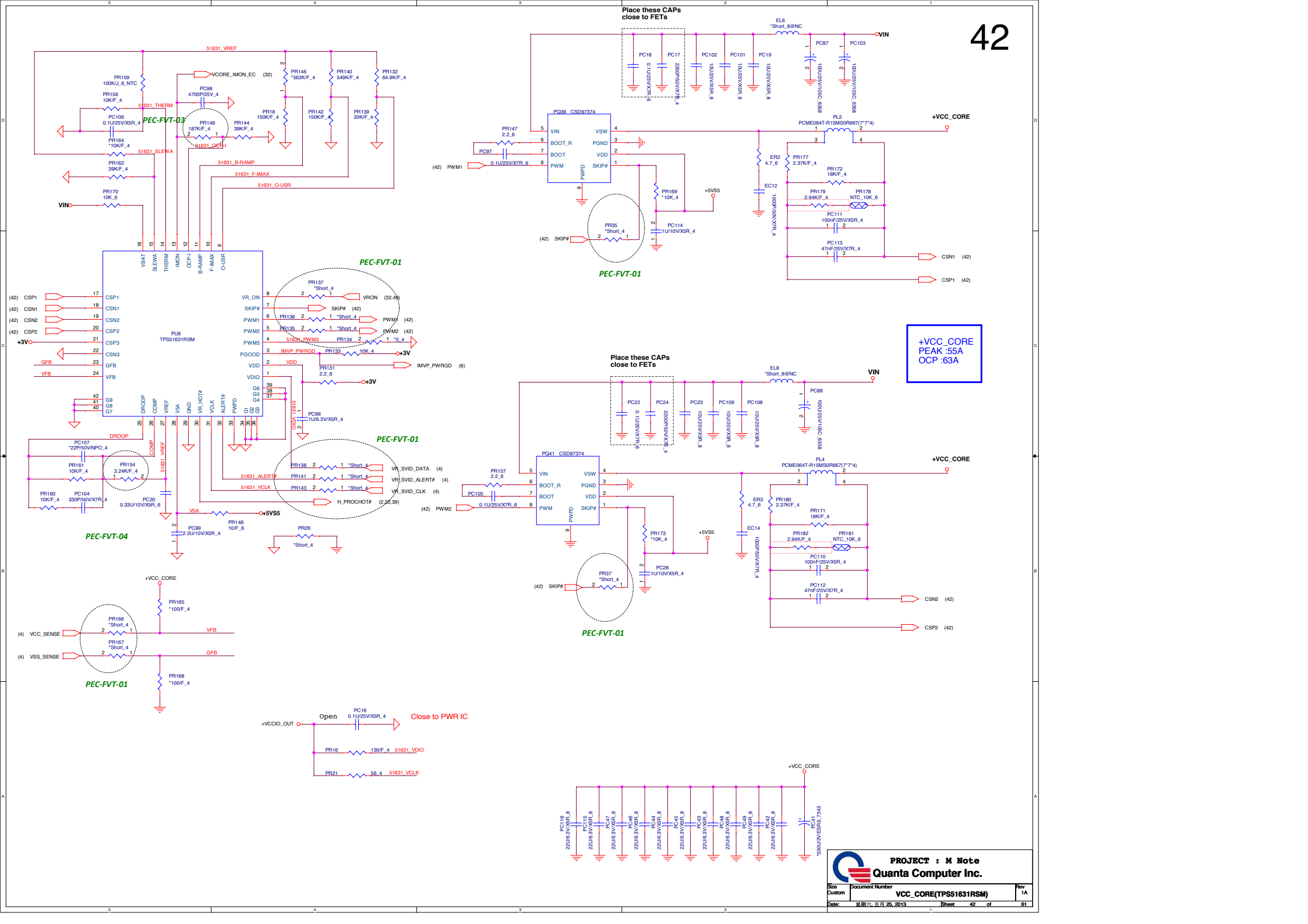
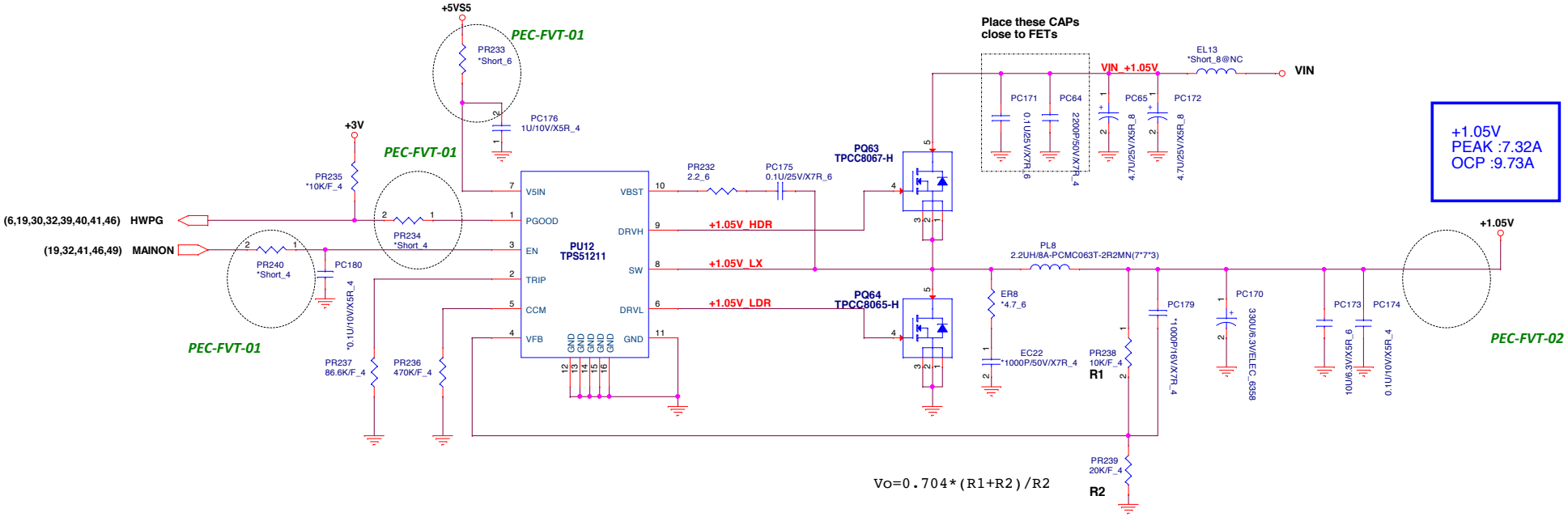
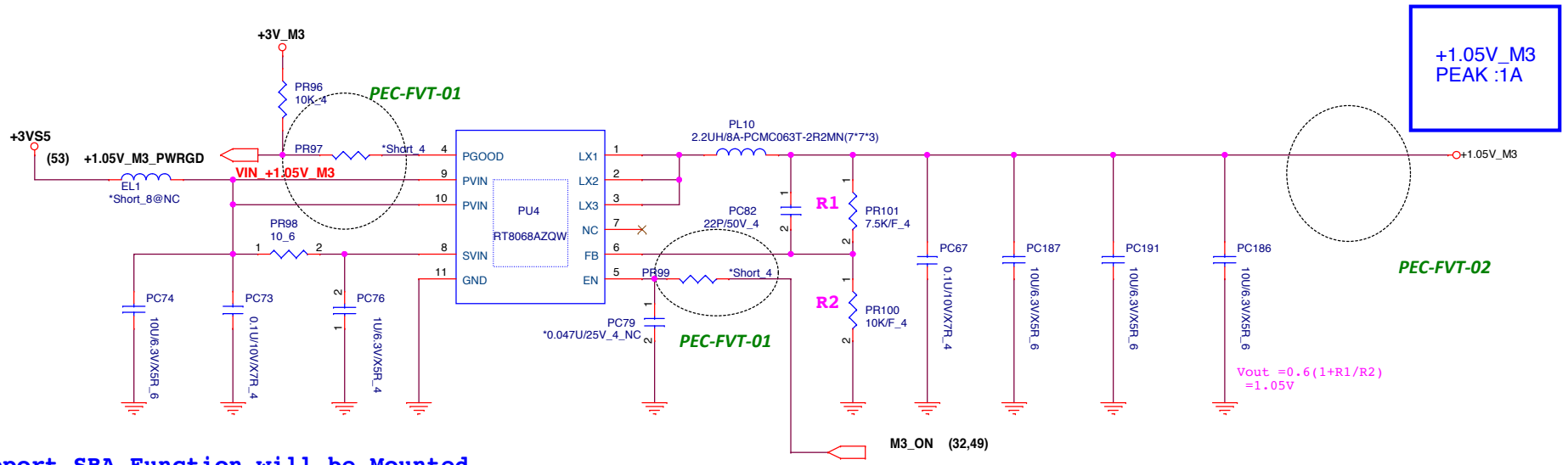

Place these CAPs close to FETs
PU6 TPS51631RSM
PQ39 CSD97374
PQ41 CSD97374
PEC-FVT-01
PEC-FVT-03
PEC-FVT-04
+VCC_CORE
PEAK :55A
OCP :63A
Close to PWR IC
PROJECT : M Note
Quanta Computer Inc.
VCC_CORE(TPS51631RSM)



PROJECT : M Note		
Quanta Computer Inc.		
Size: Custom	Document Number: +1.05V(TPS51211)	Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 43 of 61	

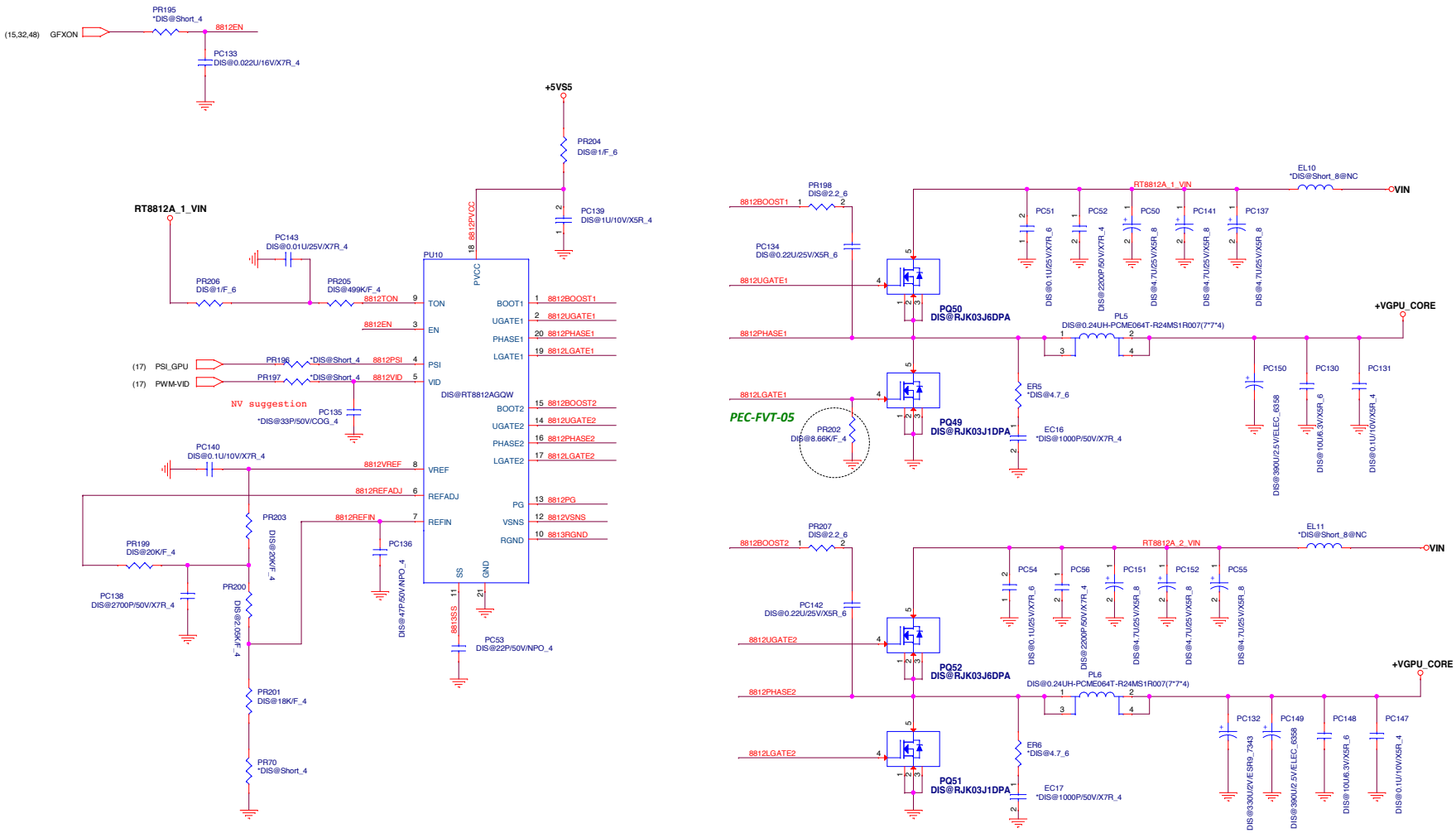
+3V_M3 (7,10,47,49,53)
+1.05V_M3 (10,49,53)



Support SBA Function will be Mounted

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
B	M3 Power(RT8068A)	1A
Date: 星期六, 五月 25, 2013	Sheet 44 of 61	



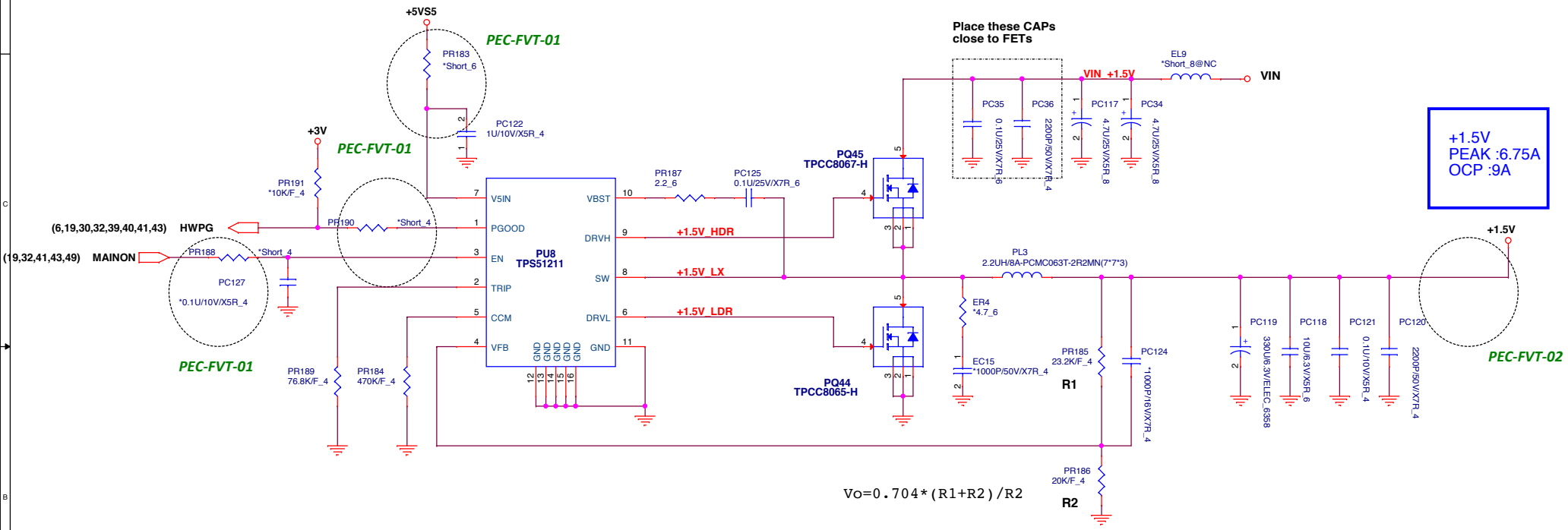
+VGPU_CORE
EDP-C: 35A
EDP-Peak: 55A
OCP: 60A

Nvidia	N14P-GV2 (Config B)	N14M-GL N14M-GE (Config C)
PR199	20KΩ	39KΩ
PR203	20KΩ	30KΩ
PR200	2.05KΩ	3KΩ
PR201	18KΩ	27KΩ
PR70	0Ω	0Ω
PC138	2.7nF	1.8nF

PROJECT : M Note
Quanta Computer Inc.

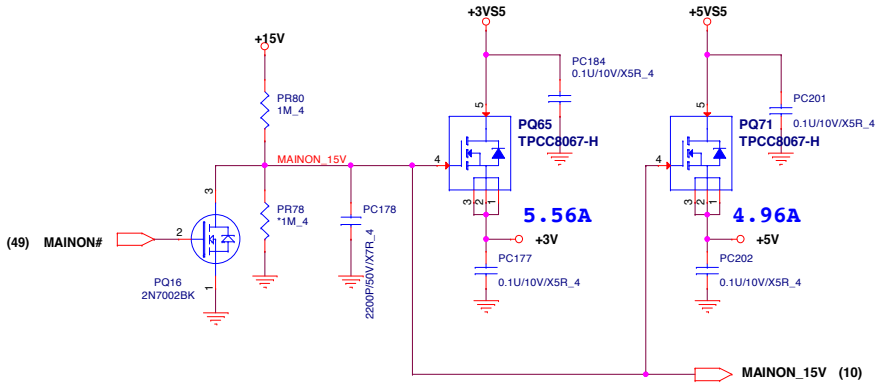
Size	Document Number	Rev
Custom	VGPU_CORE(RT8812A)	1A

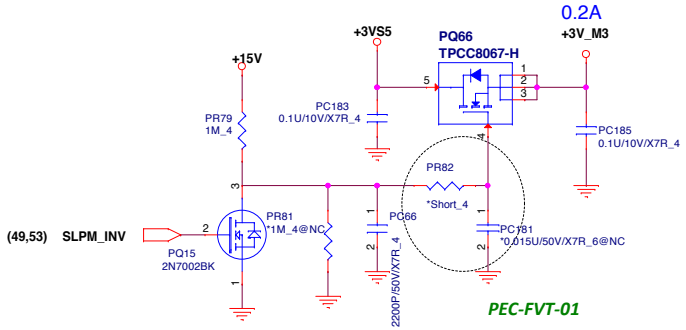
Date: 星期六, 五月 25, 2013 Sheet 45 of 61



PROJECT : M Note		
Quanta Computer Inc.		
Size: Custom	Document Number: +1.5V	Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 46 of 61	

+3V, +5V

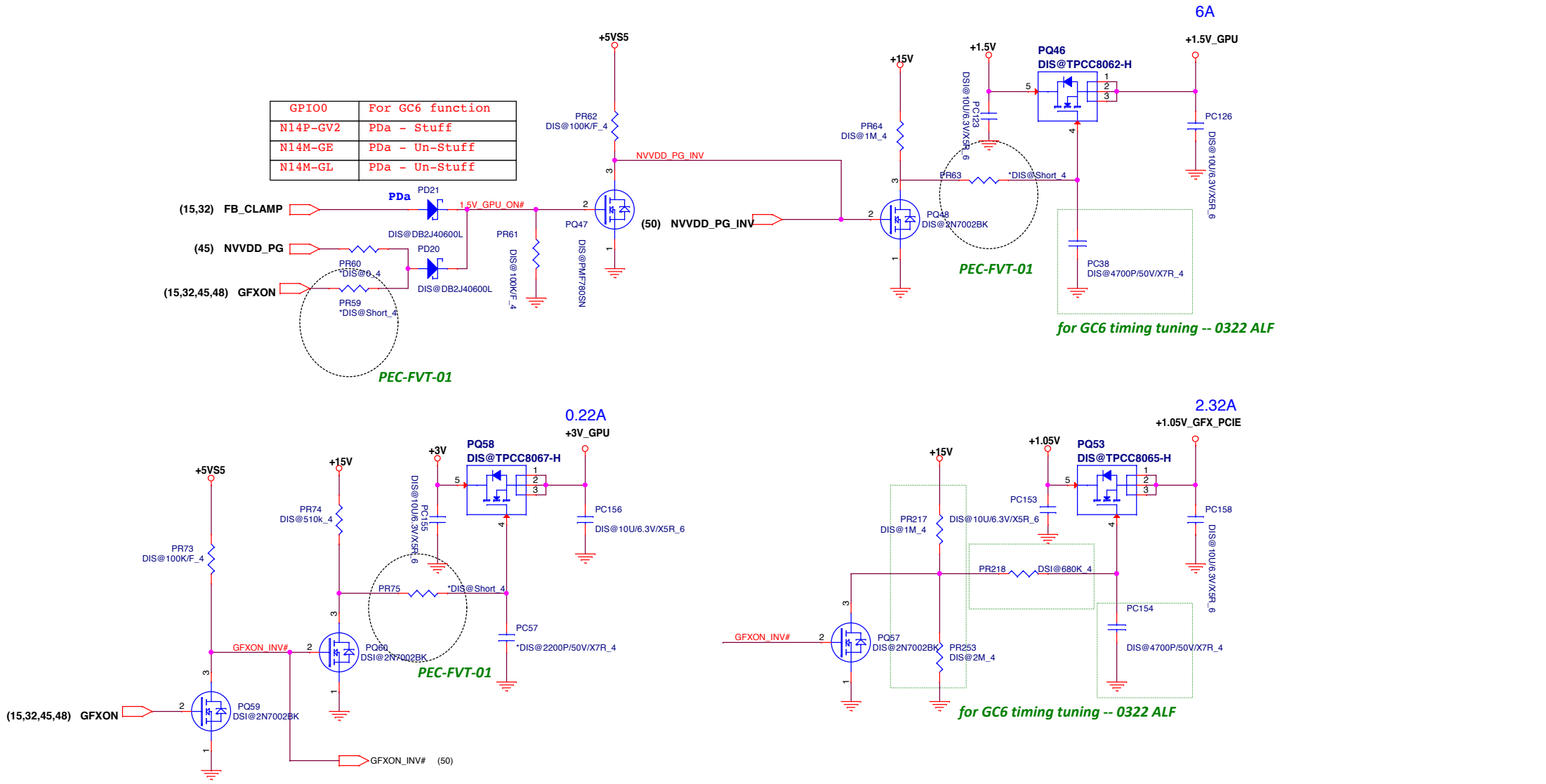




PEC-FVT-01

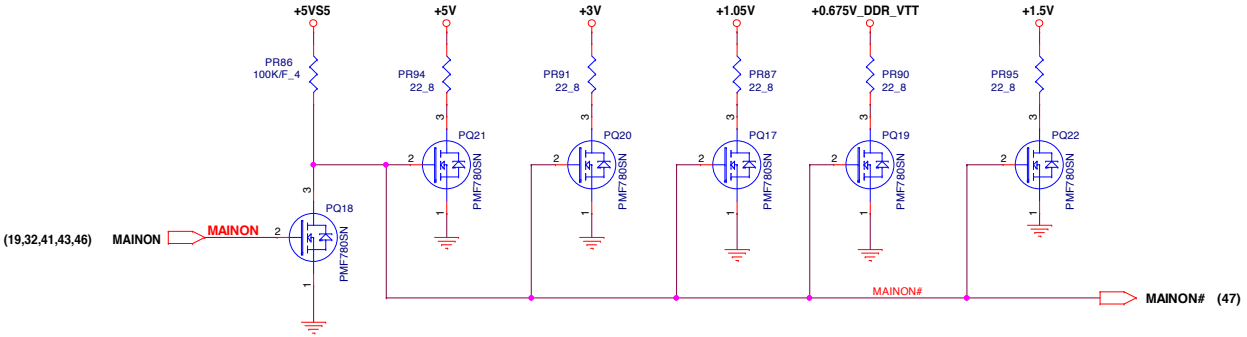
Support SBA Function will be Mounted

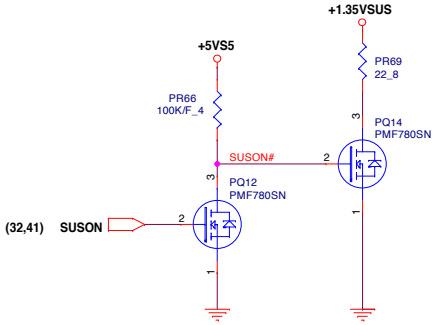
PROJECT : M Note Quanta Computer Inc.		
Size: Custom	Document Number: Load Switch	Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 47 of 61	

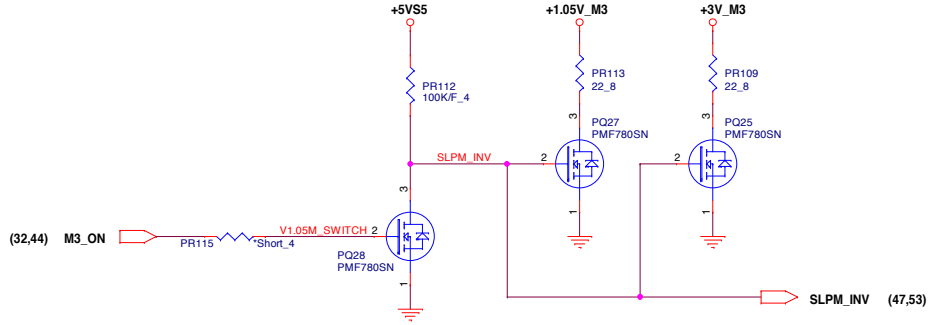


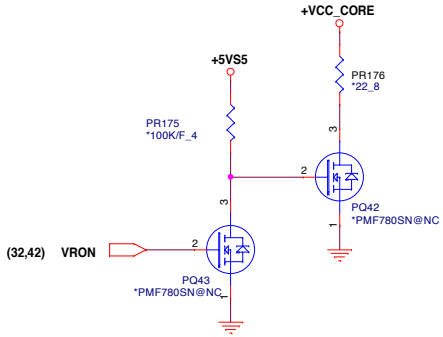
PROJECT : M Note			
Quanta Computer Inc.			
Size: Custom	Document Number: Discrete Load Switch		Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 48 of 61		

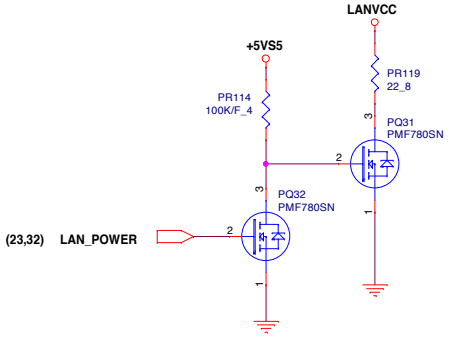
DISCHARGE









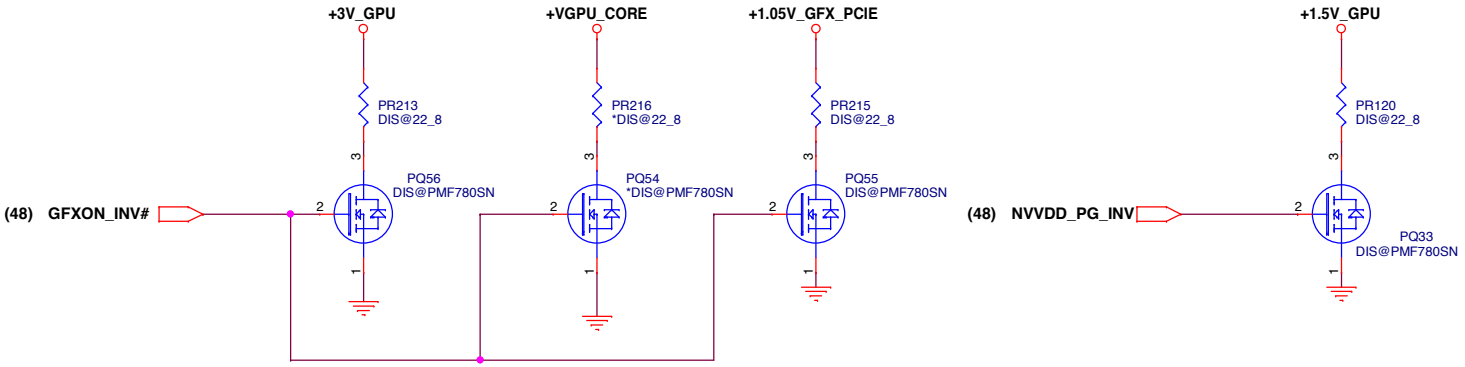


PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

Date: 星期六, 五月 25, 2013 Sheet 49 of 61

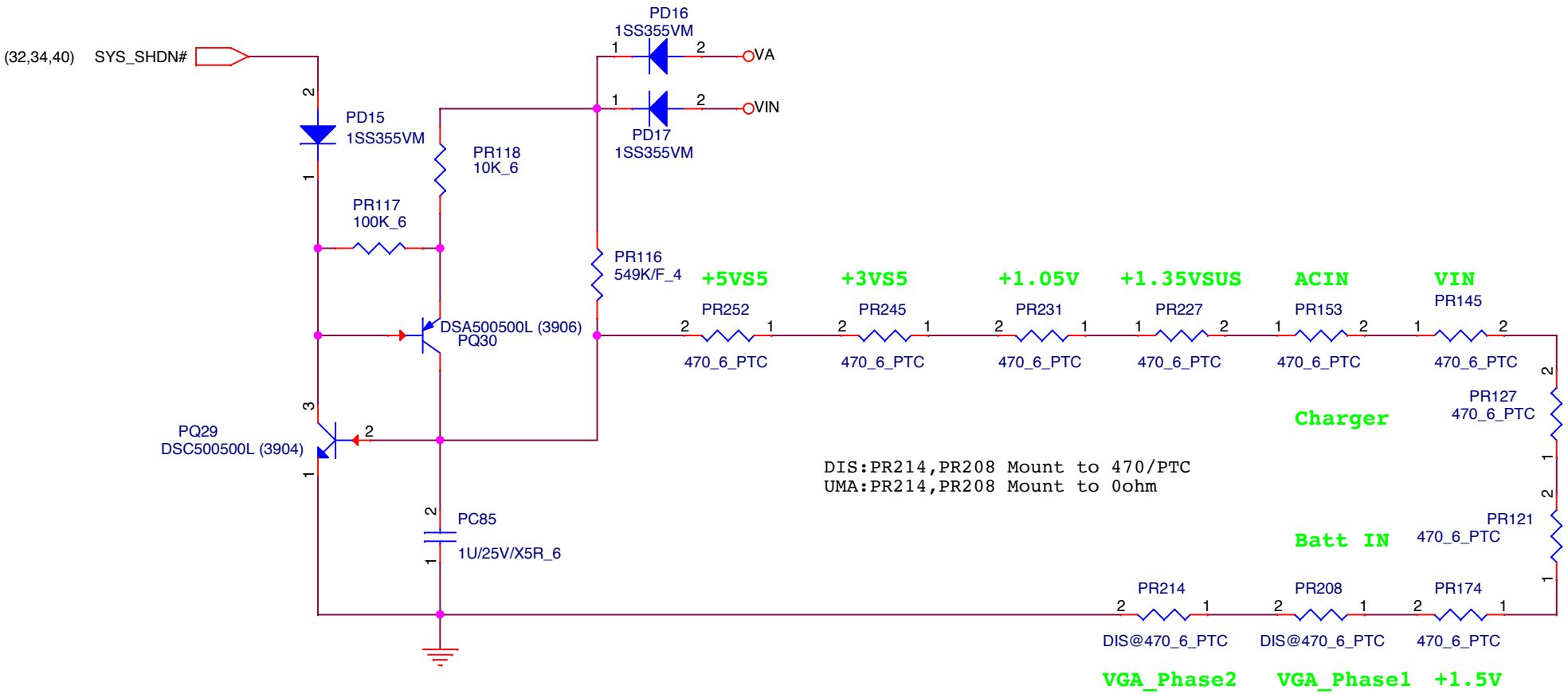
Discrete only



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
B	Discrete Discharge	1A
Date: 星期六, 五月 25, 2013	Sheet 50 of 61	



PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
A	PTC Circuit	1A
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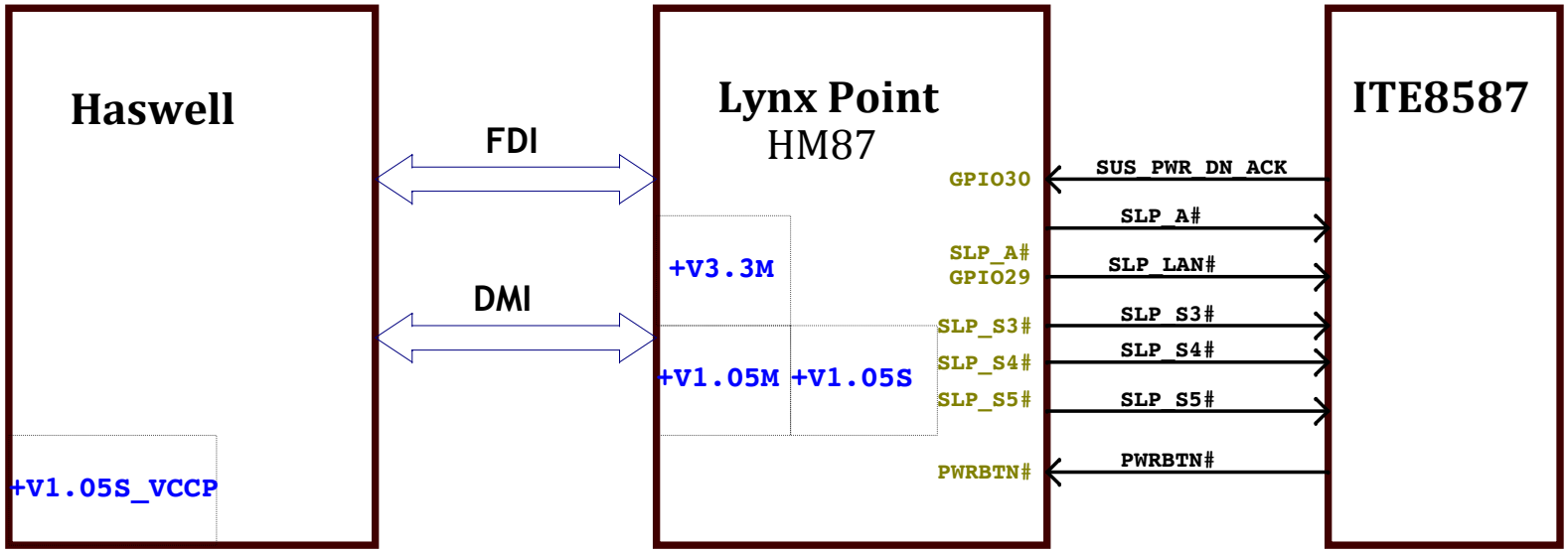

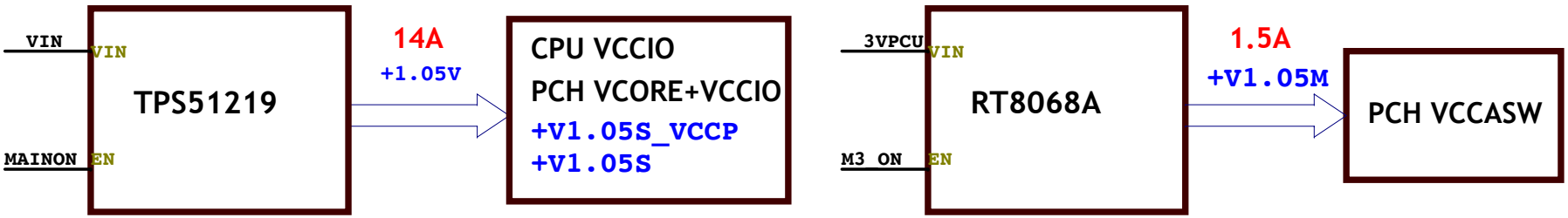

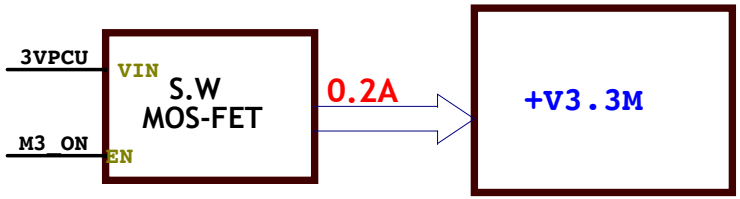

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SBA Power Block	1A

Date: 星期六, 五月 25, 2013 Sheet 52 of 61

+3VS5 (2,6,7,9,10,15,17,20,23,24,25,28,32,37,40,44,47)
+3V_M3 (7,10,44,47,49)
+3V_DEEP_SUS (6,7,8,9,10)
+1.05V_M3 (10,44,49)
+1.05V (2,4,9,10,35,43,48,49)

PCH Dual SPL -- ME ROM

32Mbit (2M or 8M Byte), SPI

BIOS+ME=8MB	R	Status
Non-SBA	R684	Stuff
SBA	R684	Un-Stuff

EC-DV-02

(7,32) 8512_SCE# — R684 *0_4 — SPI_CS0#_R

EC-DV-02

(7) PCH_SPI_CS0# — R685 *0_4S — SPI_CS0#_R
(7) SPI_CLK — R656 33J_4 — SPI_CLK_2
(7) SPI_SI — R658 33J_4 — SPI_SI_2
(7) SPI_SO — R654 33J_4 — SPI_SO_2

+3V_M3 — R657 1K_4
+3V_M3 — R653 1K_4

U45 W25Q64FVSSIQ
CE# SCK SI SO WP# VDD HOLD# VSS
SPI_CS0#_R SPI_CLK_2 SPI_SI_2 SPI_SO_2

C620 *22P/50V/NPO_4
C624 *22P/50V/NPO_4
C616 0.1U/10V/X7R_4

(7) PCH_SPI_IO2 — R659 *33_4 — PCH_SPI_IO2_2
(7) PCH_SPI_IO3 — R652 *33_4 — PCH_SPI_IO3_2

BOM P/N Okay @1227

Vender	Size	P/N
Winbond V	8MB	AKE3EFP0N07
MXIC	8MB	AKE3EZN0Z00

SBA POWERGD/SBA Power select

If EC support embedded flash , SPI power must be used S5_ON power rail for EC load code.

+3V_DEEP_SUS — L15 *1uH/25mA_6 — +3V_M3
+1.05V — R628 *0/F_8 — +1.05V_M3

Without SBA Function will be Mounted

+3VS5
+3V_M3
R348 10K_4
R349 10K_4
+3V_M3_PWRGD
Q14 PMF780SN
Q13 PMF780SN
R347 10K_4

Support SBA Function will be Mounted

SBA LOGIC

+3VS5
C353 0.1U/10V/X7R_4

(44) +1.05V_M3_PWRGD — +1.05V_M3_PWRGD
+3V_M3_PWRGD
U10 TC7SH08FU
R351 22K/J_4 — APWROK — APWROK (6)
C355 0.1U/10V/X7R_4

(47,49) SLPM_INV — SLPM_INV — Q15 2N7002BK

Support SBA Function will be Mounted

PROJECT : M Note
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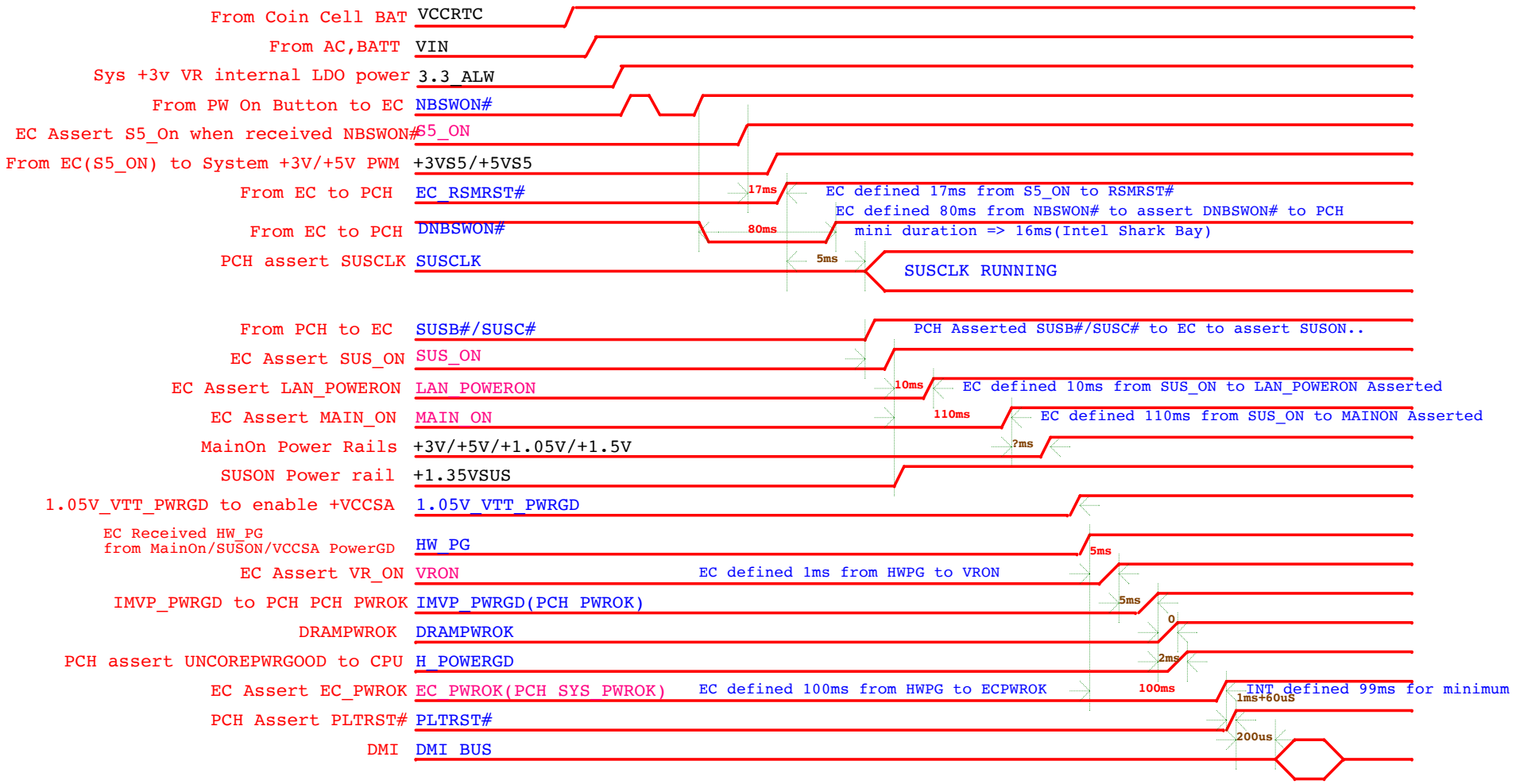
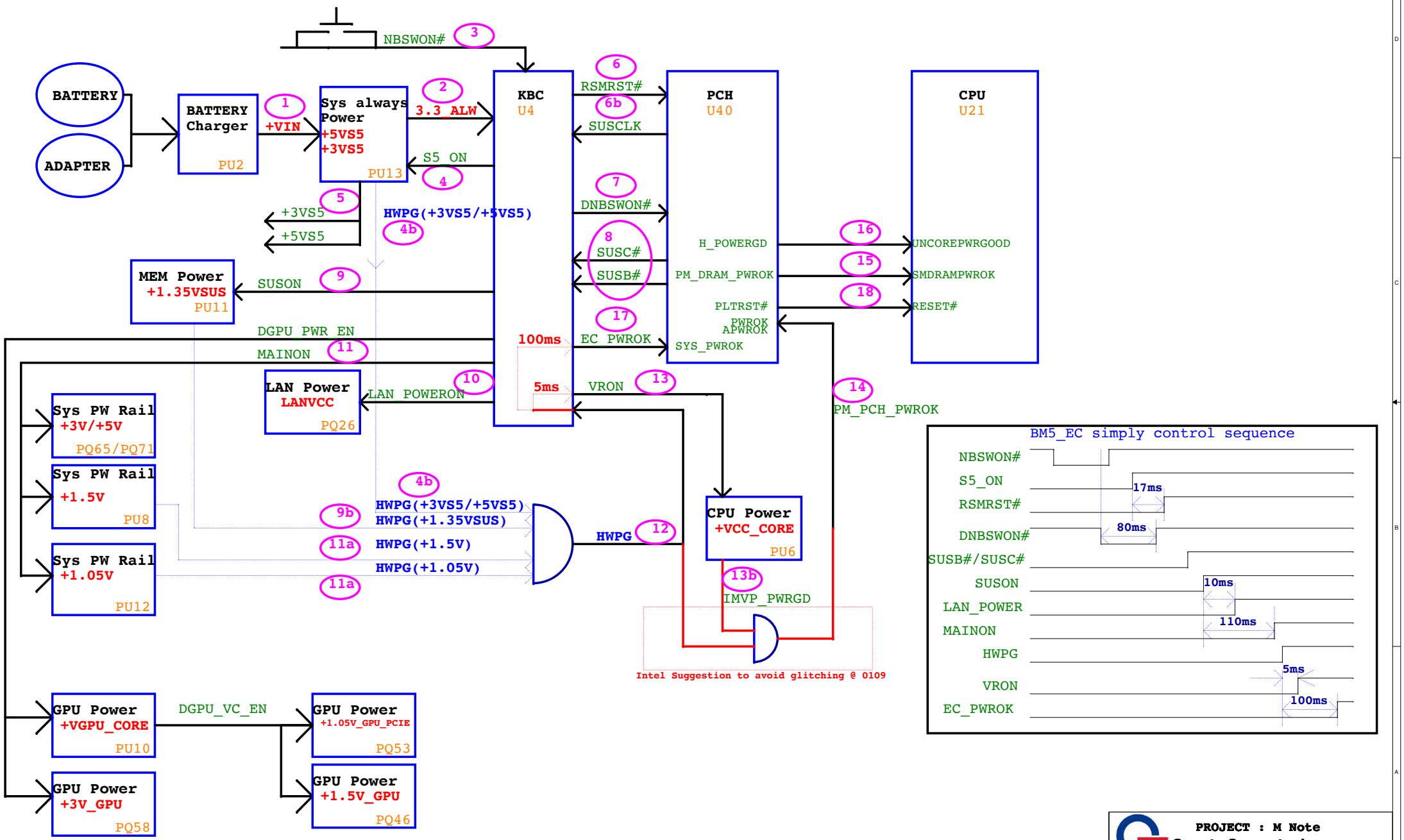
Size	Document Number	Rev
Custom	Circuit for Intel SBA	1A
Date: 星期六, 五月 25, 2013	Sheet 53 of 61	

BM5/6 -- Intel Shark Bay mainly Power On Sequence(G3 to S0)



PROJECT : M Note		
Quanta Computer Inc.		
Size: Custom	Document Number: Power On Sequence CDP ROF	Rev: 1A
Date: 星期六, 五月 25, 2013	Sheet 54 of 61	

BM5/6 -- Intel Shark Bay mainly Power On Sequence(G3 to S0)



PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Control Procesure CDP ROF	1A

Date: 星期六, 五月 25, 2013 Sheet 55 of 61

EC #	Page	Description	Part Affected
EC-DV-01	10	Change component to "Stuff" to supply the power for VCCASW.	R301
EC-DV-02	53	Add one CS0# for SPI ROM for suppoted non-SBA function. BIOS+ME at one 8MB SPI ROM.	R685,R684
EC-DV-03	8	Changed the Power Rail to +3V_DEEP_SUS following CRB	Q41
EC-DV-04	6	Follow up Intel suggestion to meet the power up sequence for Shark Bay Platform	R686,R187,U49,C643,U36,R185,C274
EC-DV-05	21	Changed the Touch Screen CONN footprint and swap Pin Define.	CN1
EC-DV-06	37	Changed the internal docking CONN footprint and swap Pin Define.	CN21
EC-DV-07	24	Modify Speaker CONN footprint	CN2
EC-DV-08	33	Modify SW1 & SW2 Switch footprint	SW1,SW2
EC-DV-09	29	Changed the Power/B CONN footprint	CN4
EC-DV-10	7	Changed the 32.768KHz part for single source issue	Y4
EC-DV-11	8	Moved the USB2+/- from port 2 to port 1and USB3+/- from port 3 to port 9 for BIOS debug function.	
EC-DV-12	32	Add HDD_DETECT# pull up 100K ohm to 3.3_ALW	R687
EC-DV-13	38	Modify HOLE 22 footprint	HOLE 22
EC-DV-14	7,10	Separate the BIOS SPI & PCH SPI I/F power from +3V_M3, and adding a +3V_DEEP_SUS power	R688,R689
EC-DV-14	7	Modify the layout routing for EC auto load function to support CS0# (SBA) & CS1#(non-SBA)	
EC-DV-15	10	Un-Stuff the 100K ohm on SLP_SUS_ON_GPG2 for voltage-divider issue	R555
EC-DV-16	38	Add a GND signal suggesded by ESD team	PAD1
EC-DV-17	23	Modify the component footprint suggestion by ESD team	RV15,RV16,RV17,RV18,RV19
EC-DV-18	18	Modify the VRAM footprint, to add the silkscreen for different VRAM package of 2Gb & 4Gb	U9,U32,U6,U22
EC-DV-19	26	Changed the USB3.0 footprint.	CN18,CN21
EC-DV-20	25	Changed the ODD Power control GPIO from EC to PCH by customer request	R605,R608
EC-DV-21	20	Modify the component footprint	C399
EC-DV-22	23	Modify the component footprint	C406
EC-DV-23	16	For install GPU-GV2 driver issue, to stuff to supply power for VID_PLLVDD.	R115
EC-DV-24	24	Swap the Pin define to solve the recorder issue of internal MIC.	CN9
EC-DV-25	32	Change the R vaule to 100K ohm	R52
EC-DV-26	6	Reserver TPs for DDI Port debug, And adding pull-up a R to +3V for Enable DDI Port.	TP79,TP80,TP81,TP82, R691
EC-DV-27	7	EMI Suggestion, stuff 15pF for 24MHz Harmonic	EC18
EC-DV-28	8	EMI Suggestion, stuff 15pF for 33MHz SSC issue	EC5,EC20
EC-DV-29	28	EMI Suggestion, stuff 15pF for 33MHz SSC issue	C635

BM5/6 Schematic EC Tracking Record DV (for DV) Jan. 18, 2013

EC #	Page	Description	Part Affected
EC-DV-30	31	EMI Suggestion, stuff 22pF for CRT EMI issue	C215,C218,C229,C230,C240,C246,
EC-DV-31	26	EMI Sugestion, stuff 90 ohm common choke for USB2.0 port.	CML7,R673,R674
EC-DV-32	26	EMI Sugestion, stuff 90 ohm common choke for USB2.0 port.	CML8,R675,R676
EC-DV-33	24	EMI Sugestion, stuff 600 ohm bead for Speaker port.	R2,R3,R4,R5
EC-DV-34	22	EMI Sugestion, stuff 120 ohm R for HDMI port.	R638,R642,R650,R651
EC-DV-35	09	Board ID for BM5 / BM6 A2 stage	R586,R589,R283,R284,R575,R573,R278,R275

BM5/6 Schematic POWER EC Tracking Record DV (for DV) Jan. 18, 2013

EC #	Page	Description	Part Affected
PEC-DV-01	5	Follow Intel schematic review suggestion	C487,C92,C93,C512,C478

PROJECT : M Note
Quanta Computer Inc.

Size	Document Number	Rev
Custom	POWER EC RECORD DV	1A

Date: 星期六, 五月 25, 2013 Sheet 58 of 61

EC #	Page	Description	Part Affected
EC-SIT-01	05	Intel's Suggestion, to remove 1K ohm on CFG9	R480
EC-SIT-02	29	Added Thermal Pad to GND	U48
EC-SIT-03	37	Reserve design for Parade USB3.0 re-driver IC	U2,R692,R693,R694,R695,R696,R697
EC-SIT-04	32	Added 10K ohm to pull-up the +3VS5 rail on USB_STATUS#	R698
EC-SIT-05	09	Changed the power rail of "SV_DET" to +3V	R542
EC-SIT-06	14	Changed the GPU's enable signal of CLK_REGA_REQ# to "GFXPG"	Q6
EC-SIT-07	07	EMI suggestion to change the capacitor value	EC18,EC19
EC-SIT-08	23	Modify the LAN Surge protected circuit from EMI suggestion	R172,RV15,R699,R173,R174,R175,R176,U50,U51
EC-SIT-09	27,32	Removed the "NGFF_SSD_PRESENT#" to Pin21, and changed to 3.3V_ALW. Lenovo suggestion	CN19
EC-SIT-10	08,27	Added one GPIO controlled by PCH and pull down 10K ohm	R700,CN19,R359
EC-SIT-11	37	Added 4pcs AC Cap at RX/TX for docking USB3.0 function. Lenovo suggestion	C644,C645,C646,C647,CN12,U2,U20
EC-SIT-12	28	Reserve 2pcs Cap on WLAN PCIE Clock 100MHz.	C648,C649
EC-SIT-13	32	Reserve 220pF on ACDC_ID signal	C650
EC-SIT-14	06,32	Non-stuff the parts, ESD suggestion	C59,C586
EC-SIT-15	32	Reserve 0.1uF on "HDD_DETECT# signal	C651
EC-SIT-16	32	Reserve 330pF on +3.3V_RUN_EC power rail	C652
EC-SIT-17	33	Stuff the parts, ESD suggestion	RV5,RV6
EC-SIT-18	29	Reserve without AOU5 circuit	RP9,PR10,RP11,RP12,U52,U48,C653
EC-SIT-19	24	Delete R359 to increase space for circuit of w/o AOU5	R359
EC-SIT-20	32	Added 2 resistances to select AOU5 function	R701,R702
EC-SIT-21	20	Changed the Touch Screen solution, so deleted the CN1 Conn.	CN1
EC-SIT-22	20	Changed the LVDS Conn type to 40Pin for adding touch function	CML1,R402
EC-SIT-23	29	Stuff the parts, EMI suggestion	CML4,CML5,R355,R356,R354,R353
EC-SIT-24	21	Stuff the parts, EMI suggestion	CML6,R395,R396
EC-SIT-25	20	Stuff the parts, EMI suggestion	C4,C5
EC-SIT-26	20	Stuff the parts, EMI suggestion	L23,R406,R407
EC-SIT-27	32	Added on 0 ohm from +3V_RTC rail to RTC_VCC rail	R703
EC-SIT-28	08,25	Reserve HDD_DEVSLP function at HDD device	R704,R705
EC-SIT-29	07	Stuff the some components for preventing the leakage on +3V power rail	Q38,R205,R194,R527,R
EC-SIT-30	22	Changed the R value from 680 to 470 of Cost Reduced Level Shifter for HDMI eye diagram test	R325,R326,R327,R328,R329,R332,R333,R334

BM5/6 Schematic EC Tracking Record SIT (for SIT) Mar. 21, 2013

EC #	Page	Description	Part Affected
EC-SIT-31	37	Added the pull-up R on EQ1 & EQ2 for USB3.0 SI of RX test	R16,R20
EC-SIT-32	07	Changed the Cap Value for fine-tuning the crystal's accuracy	C277,C280
EC-SIT-33		Changed the Conn. to ECSL parts	JDIM2,JDIM1,CN15,CN17, PJP1,CN13,CN14,CN16,CN18,CN21,CN5,CN6 CN7,CN10,CN4,CN20
EC-SIT-34	33	Changed the parts of click pad switch by ME requirement	SW1,SW2
EC-SIT-35	29	Setting the AOU5 RILIM_Hi & RILIM_Lo to current 2.3A & 1.5A	R669,R670
EC-SIT-36	09	Board ID for BM5 / BM6 SIT Stage	R586,R589,R283,R284,R575,R573,R278,R275

PROJECT : M Note

Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC RECORD SIT	1A

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BM5/6 Schematic EC Tracking Record SIT2 (for SIT2) May. 24, 2013

EC #	Page	Description	Part Affected
EC-SIT2-01	33	Changed the CN5 Footprint	CN5
EC-SIT2-02	29	Delete the CN10 Pin 2 +3V for assembly line issue	CN10
EC-SIT2-03	25	Directly connect HDD Conn Pin18 to GND. Lenovo suggestion	CN17
EC-SIT2-04	32	Swap the GPIO Pin on 108 & 30 to support the breathing effect	U4
EC-SIT2-05	28	Add a circuit to don't support AOAC function	R665
EC-SIT2-06	07,20	Added 1 GPIO21 of PCH to control the Touch Panel RST Pin and 1 Cap 0.47u for timing fine tune	U40,R630, C654
EC-SIT2-07	19	Stuff the parts for linking the eDP to LVDS converter IC via SMBus	Q22
EC-SIT2-08	15	Modify the part's footprint	Q35
EC-SIT2-09	29	Changed the CN4 Footprint from 0.5 pitch to 1.0 pitch for assembly line issue	CN4
EC-SIT2-10	27	Delete the GND Pin on Pin5 of NGFF Connector as Vendor's PCR	CN19
EC-SIT2-11	09	Just modify the signal neme to AOAC_EN	U40
EC-SIT2-12		Delete the 0 ohm or common chock on all USB ports	R353,R354,R355,R356,R673,R674,R675,R676,R395,R396,R406,R407,CML2,3
EC-SIT2-13	20	Modify the part's footprint	CML1
EC-SIT2-14	29	Modify the part's footprint	CN10
EC-SIT2-15	29	Modify the ILIM LO R value from 68K ohm to 2M ohm	R670
EC-SIT2-16	32	Added M3_ON pull up 10K ohm with 3.3V_ALW for Auto load code issue	R353
EC-SIT2-17	09	Board ID for BM5 / BM6 SIT2 Stage	R586,R589,R283,R284,R575,R573,R278,R275

PROJECT : M Note

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Size	Document Number	Rev
Custom	EC RECORD SIT2	1A
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