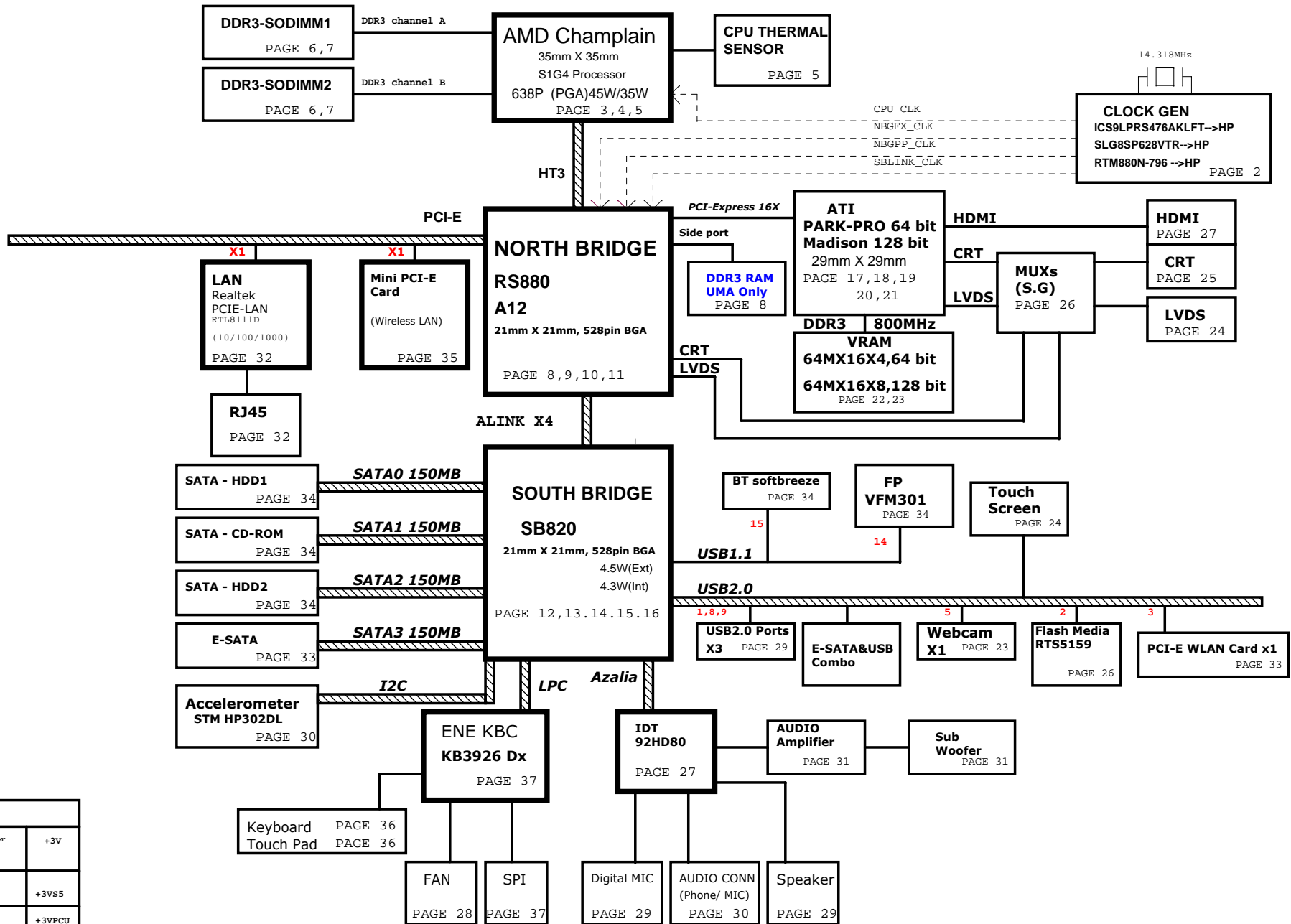


PCB STACK UP

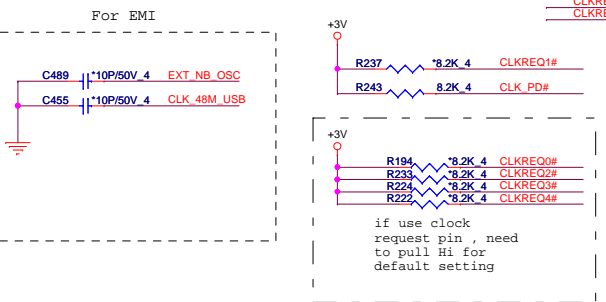
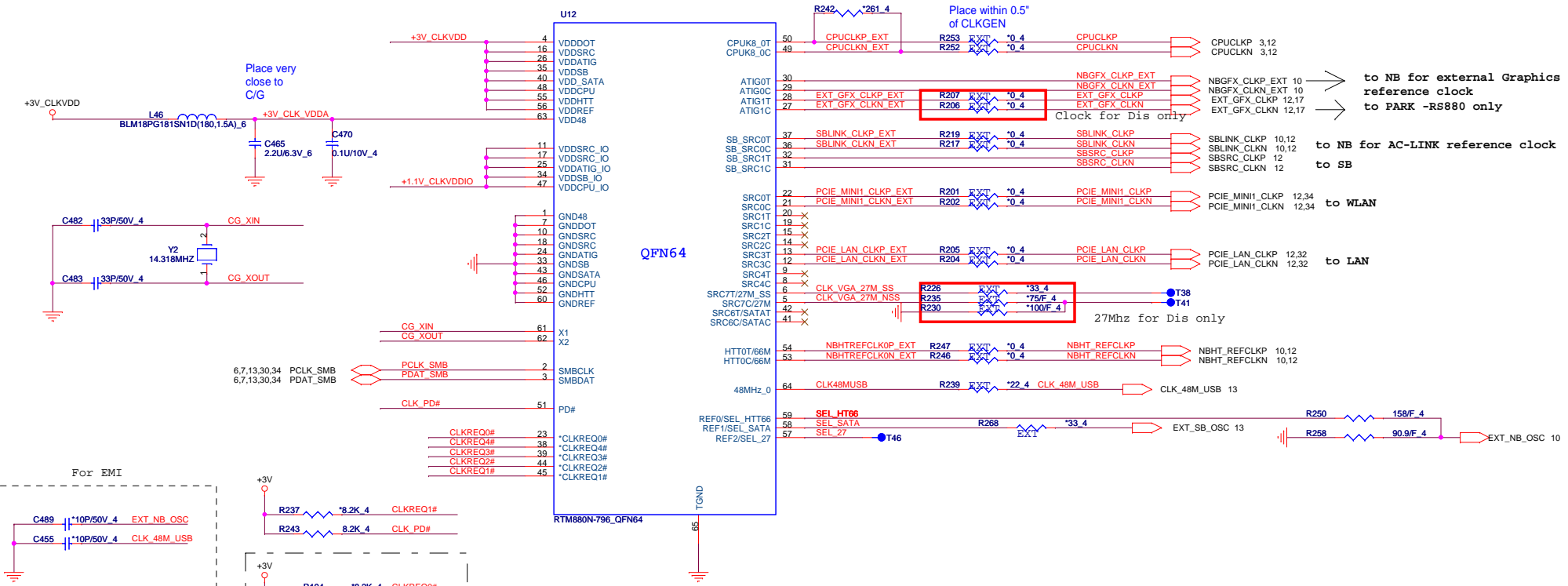
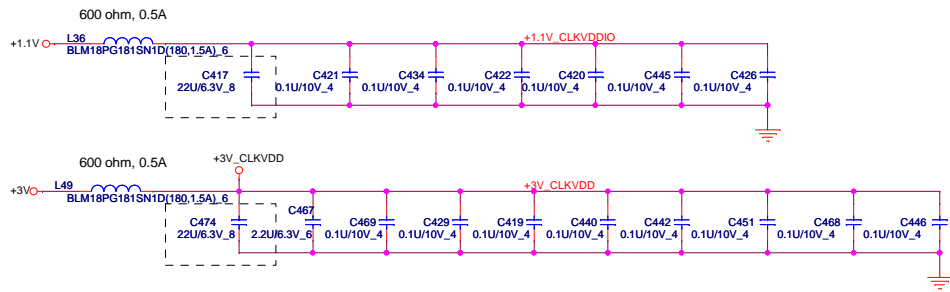
- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

LX89 SYSTEM DIAGRAM



- SYSTEM CHARGER(ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
- VCCP +1.1V AND +1.2V(RT8204) PAGE 35
- VGACORE(1.1V-1.2V)Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/FV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

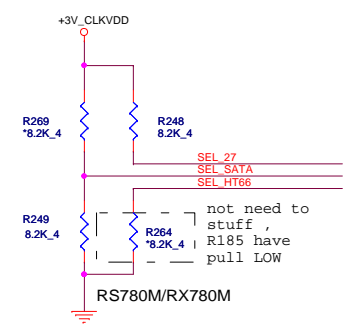


SLG
RTL

SLG8SP628VTR--AL8SP628000
RTM880N-796-- AL000880001

* default

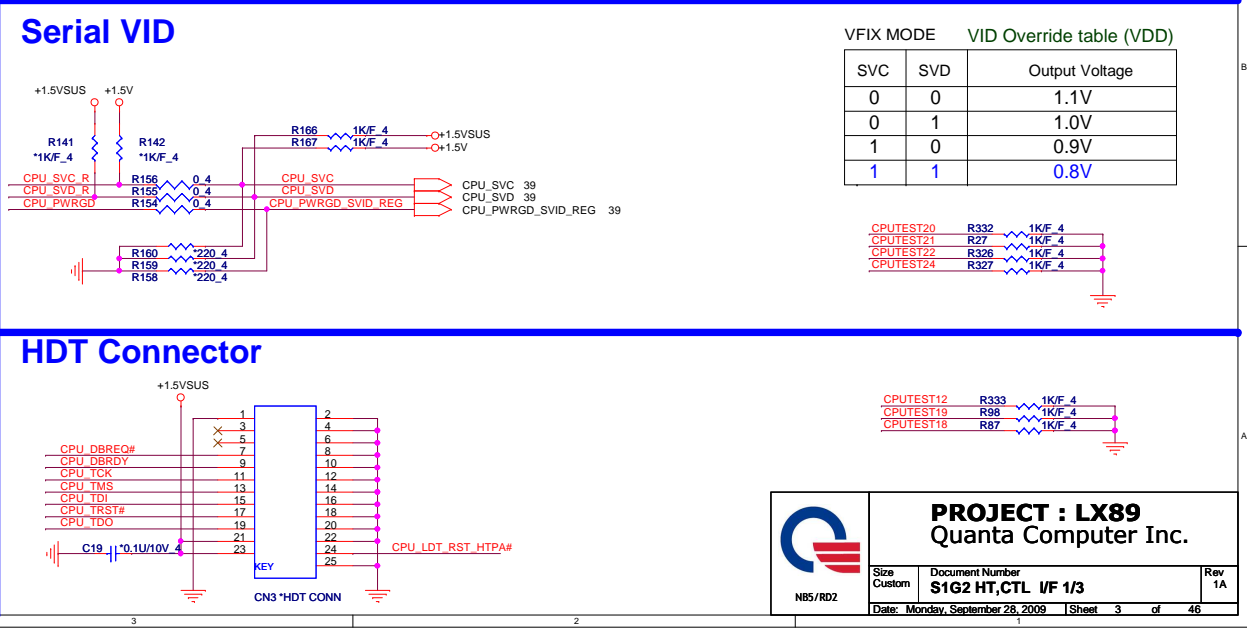
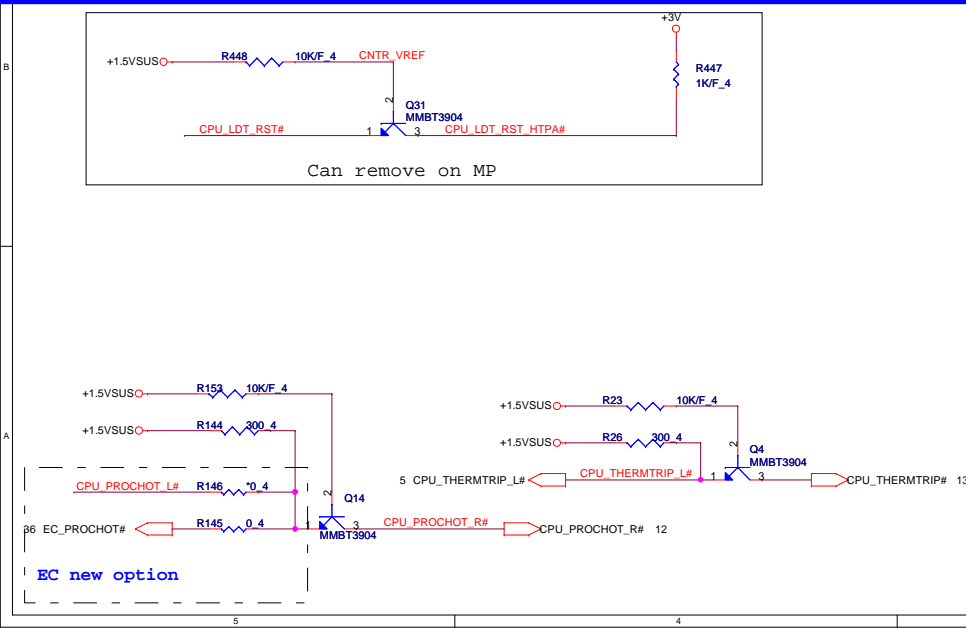
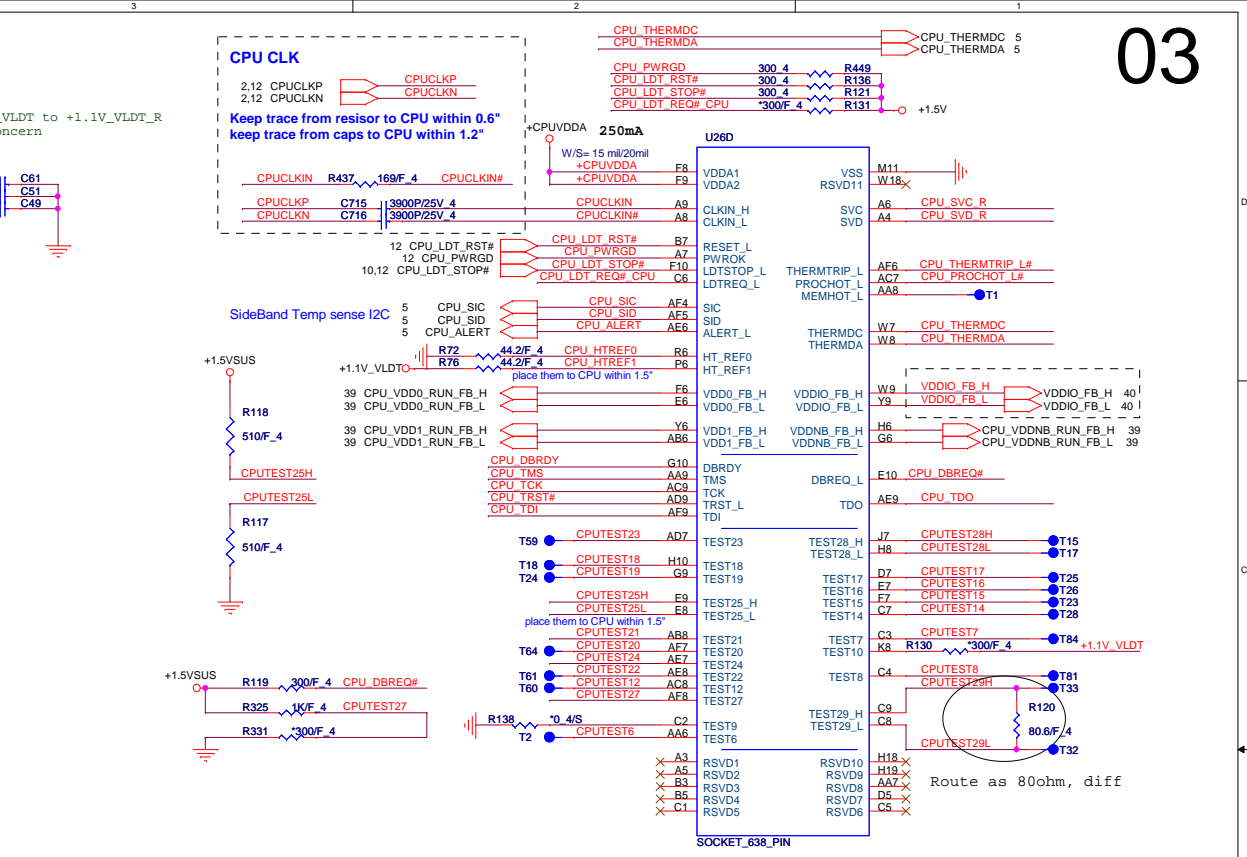
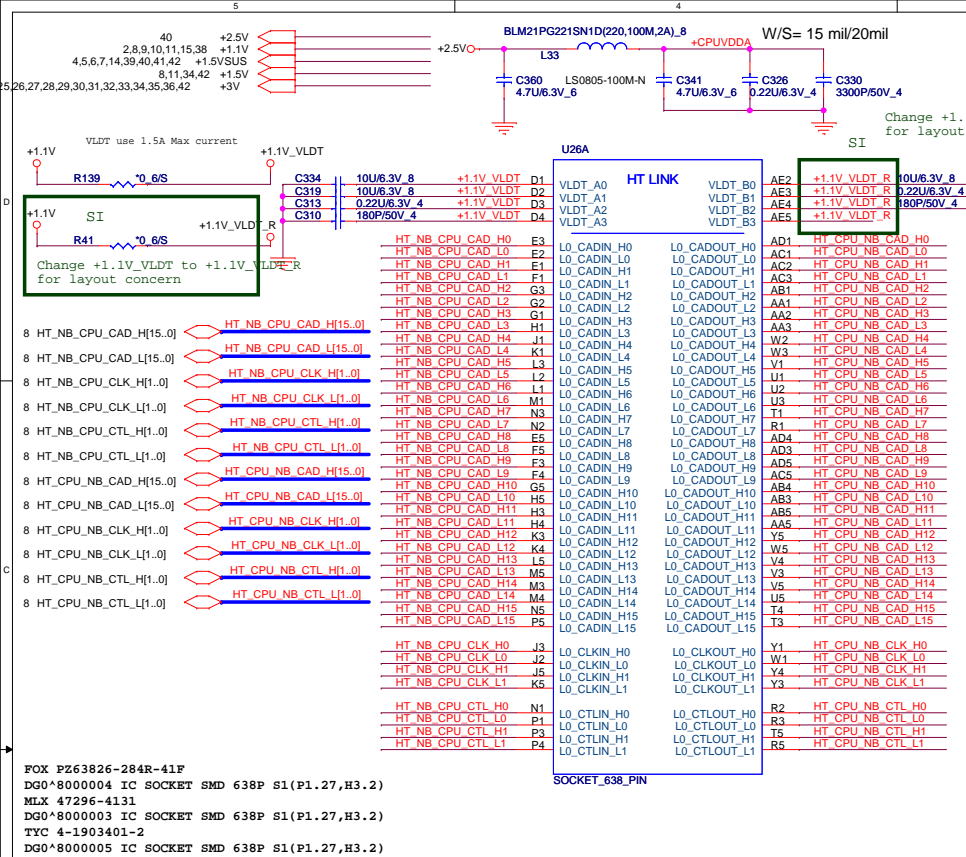
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
SEL_HTT66	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
SEL_SATA	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
SEL_27	0	100 MHz spreading differential SRC clock

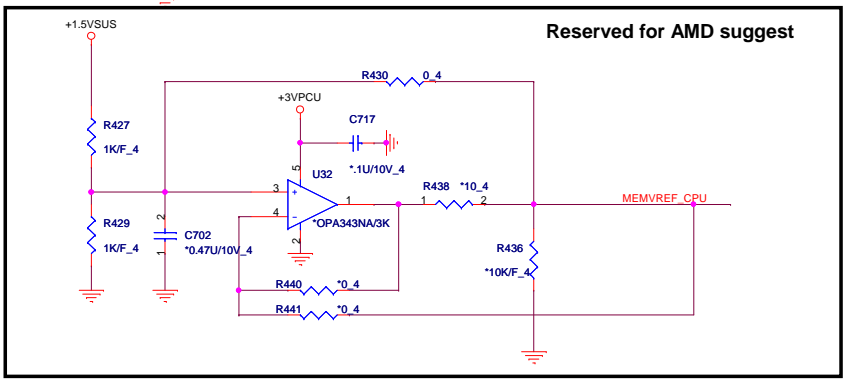
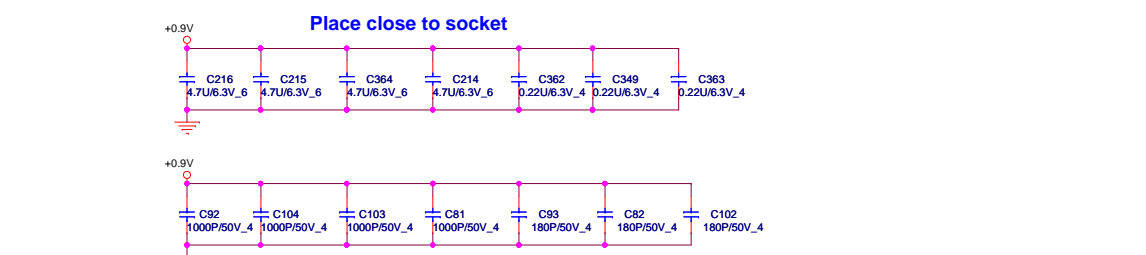
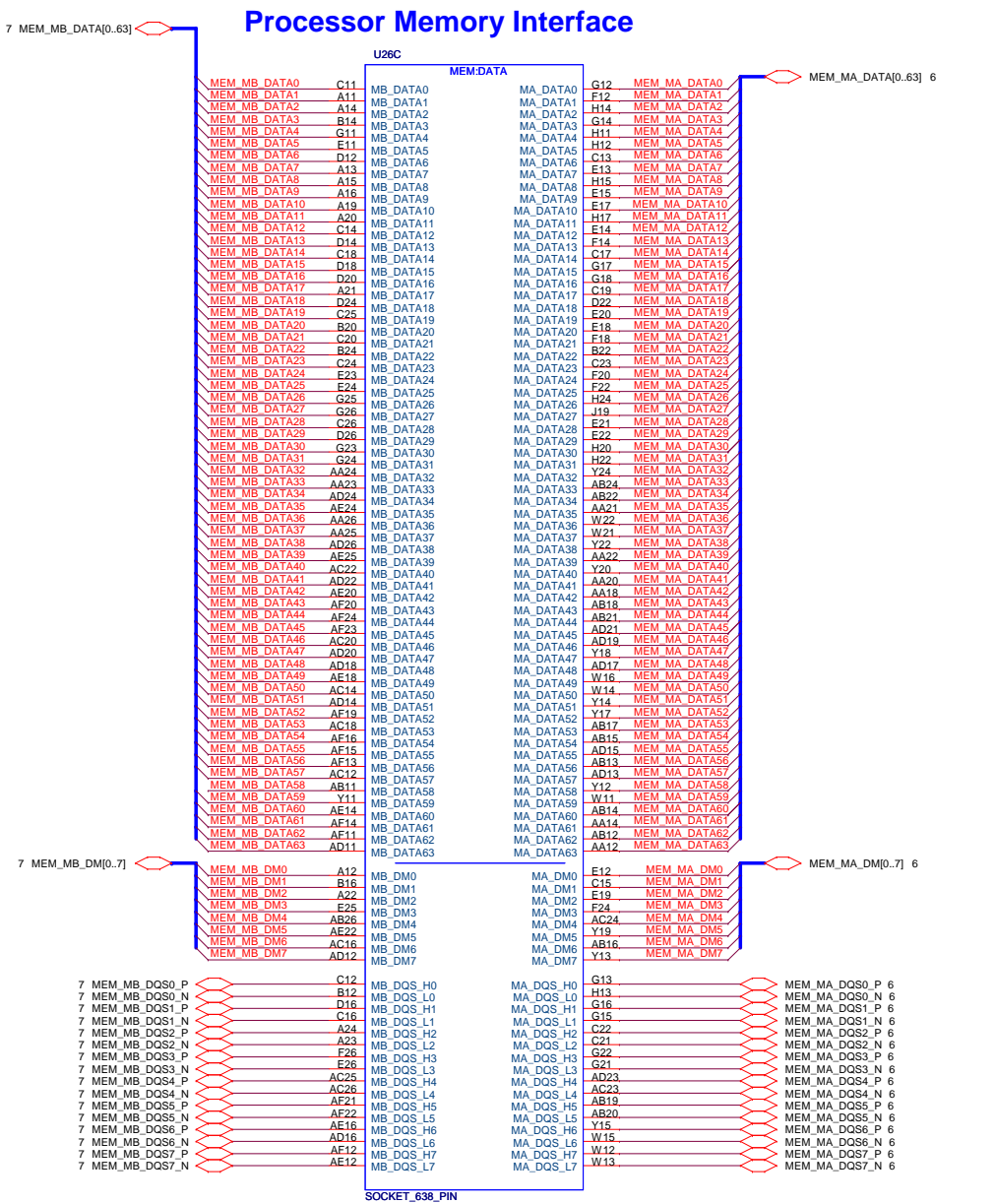
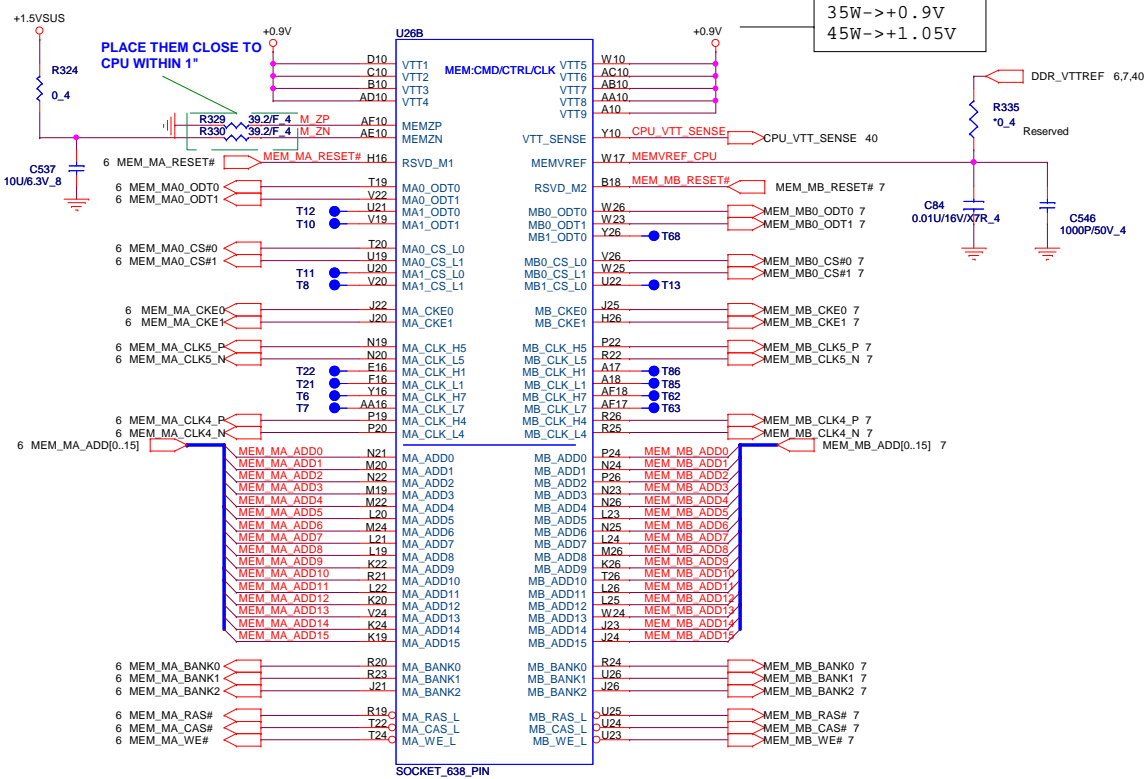


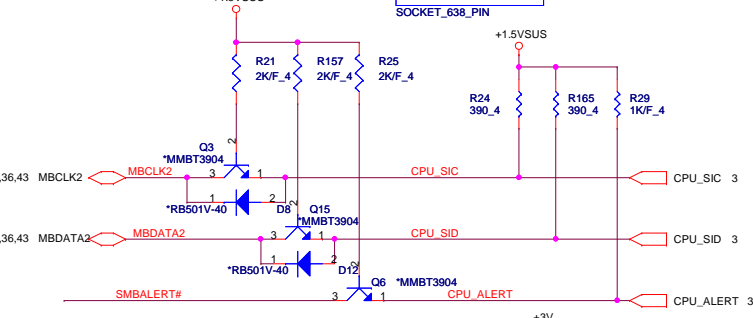
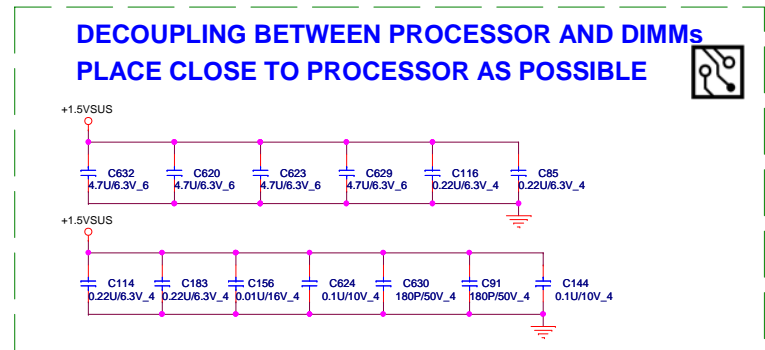
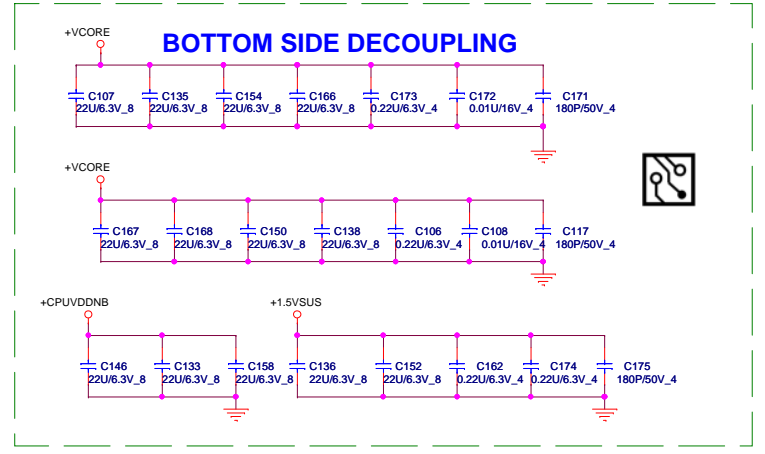
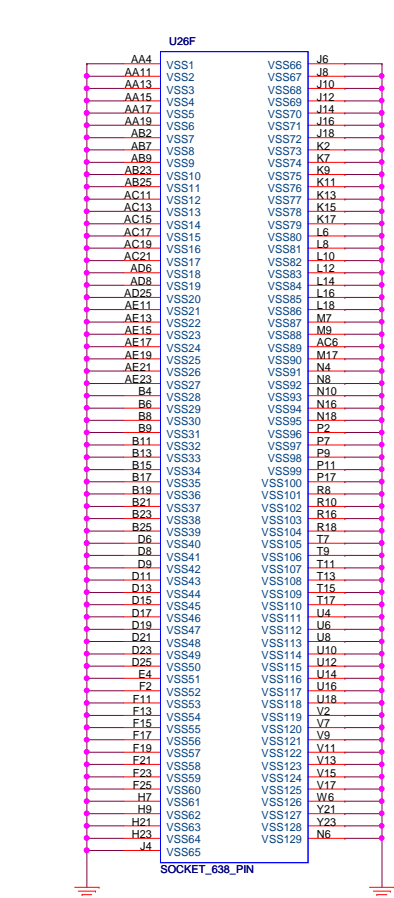
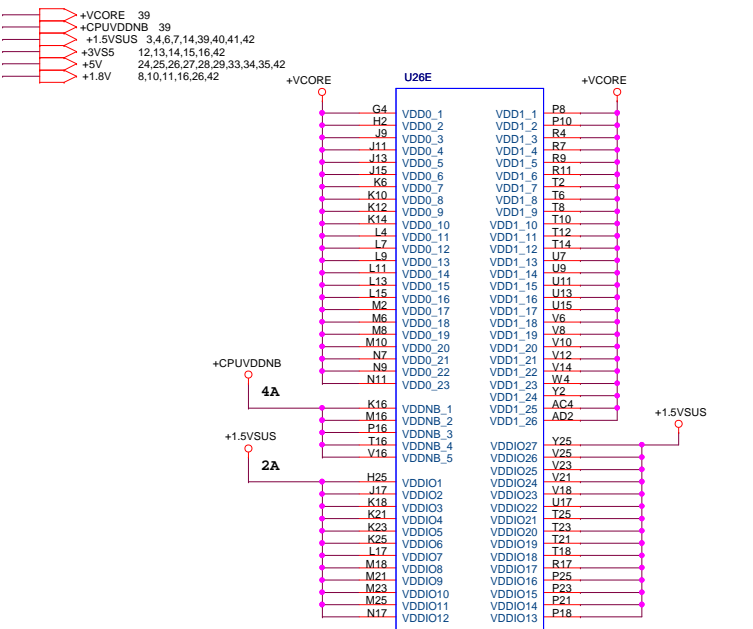
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

PROJECT : LX89
Quanta Computer Inc.

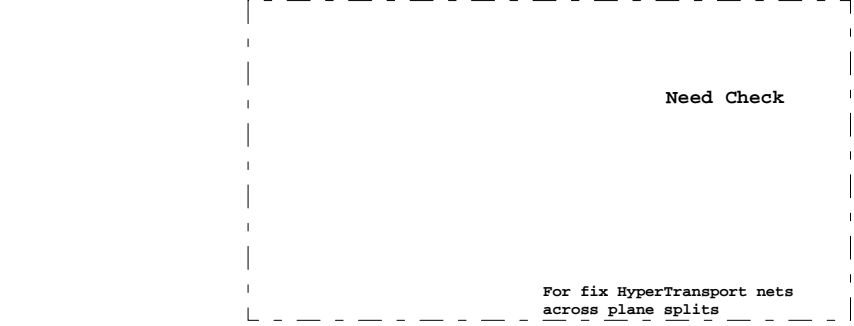
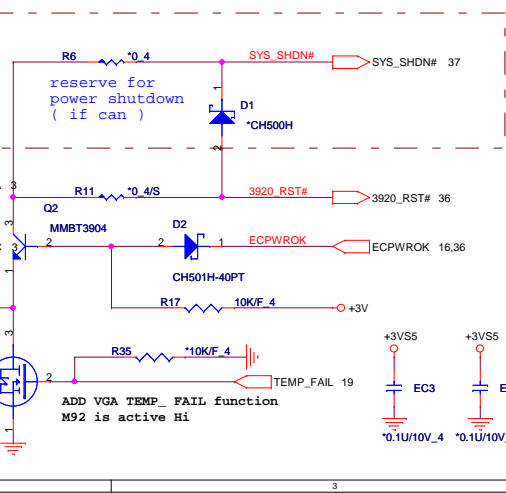
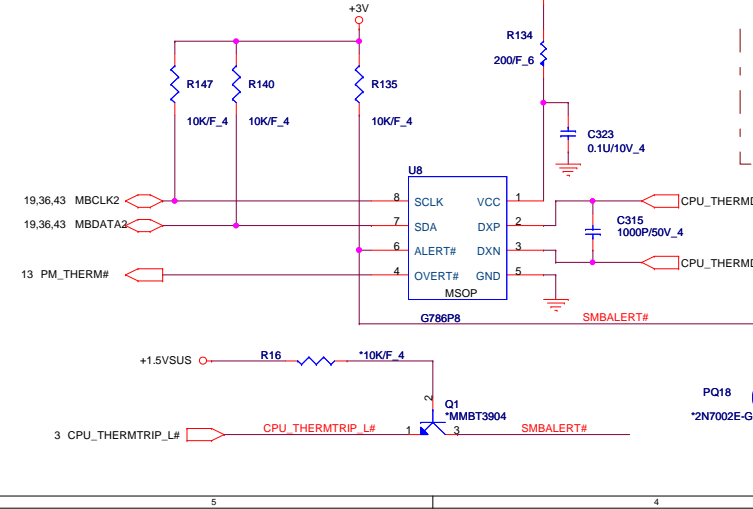
Size Custom	Document Number Clock Generator	Rev 1A
Date: Monday, September 28, 2009 Sheet 2 of 46		







PROCESSOR POWER AND GROUND

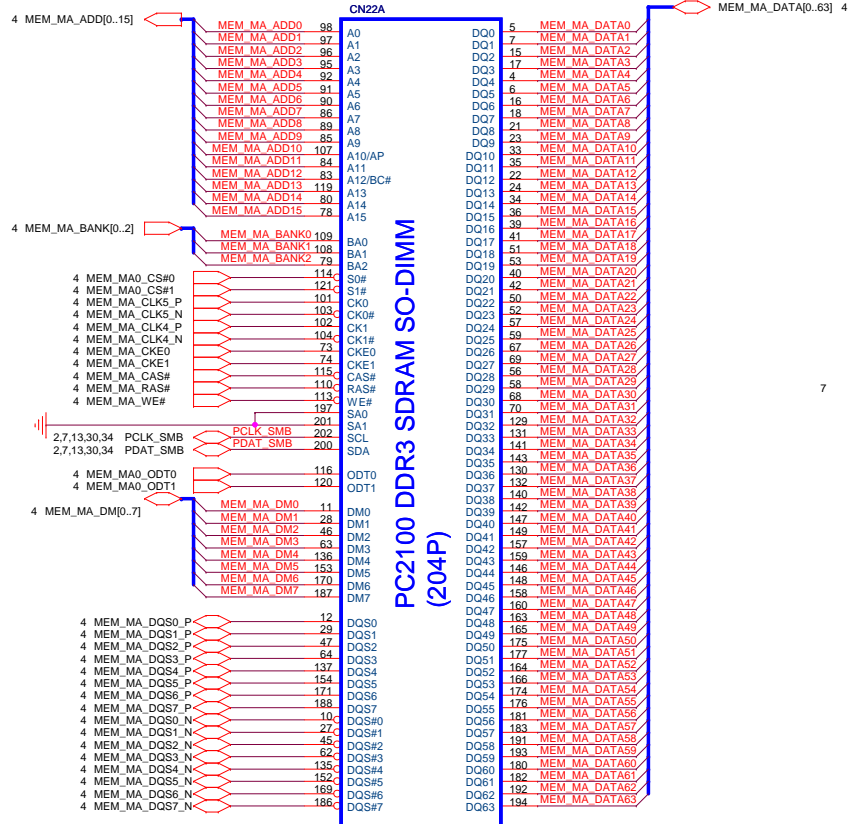


PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number S1G2 PWR & GND 3/3	Rev 1A
Date: Monday, September 28, 2009		Sheet 5 of 46

NBS/RD2

+1.5VSUS 3,4,5,7,14,39,40,41,42
+3V 2,3,5,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+0.75V_DDR_VTT 7,40

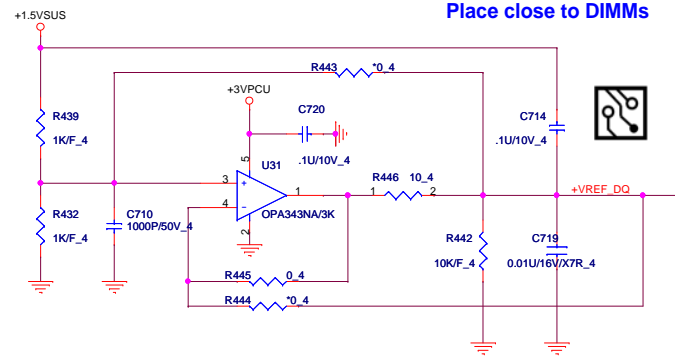
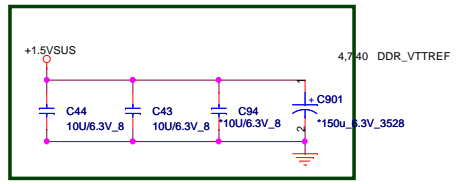
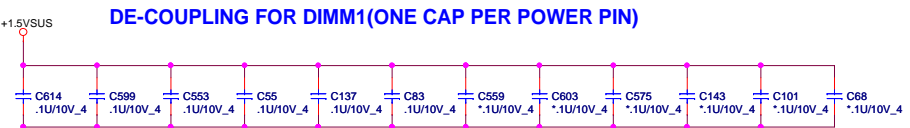


PC2100 DDR3 SDRAM SO-DIMM (204P)

PC2100 DDR3 SDRAM SO-DIMM (204P)

H=5.2 Footprint: "ddr-c-2013289-204p" DGMK4000059

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.



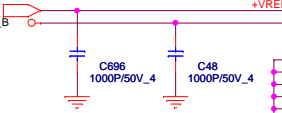
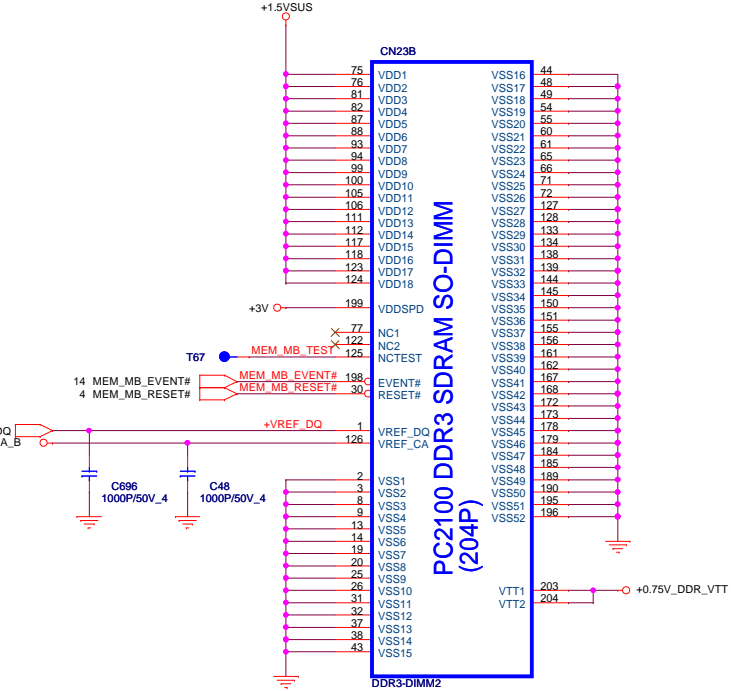
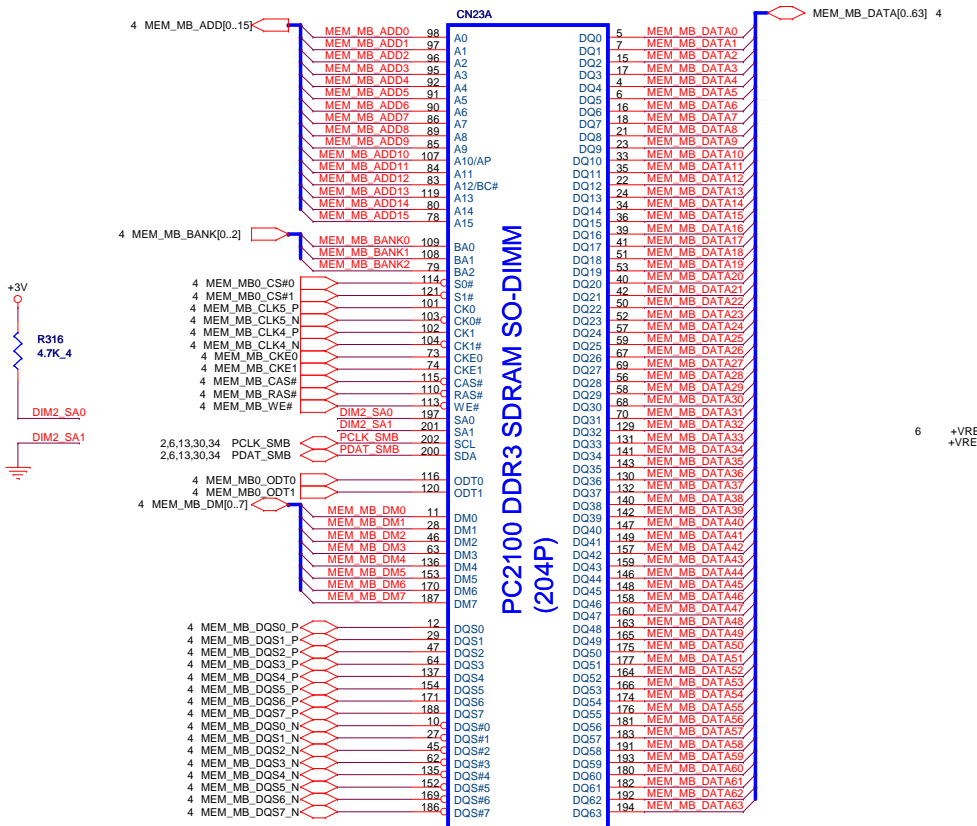
Place close to DIMMs

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
DDR3 SODIMMS: A/B CHANNEL		
Date: Monday, September 28, 2009 Sheet 6 of 46		

NBS/RD2

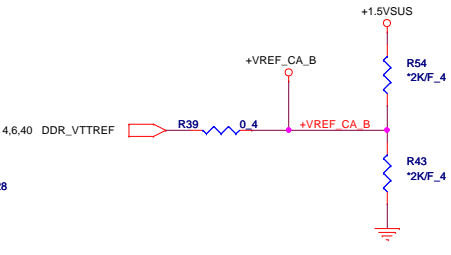
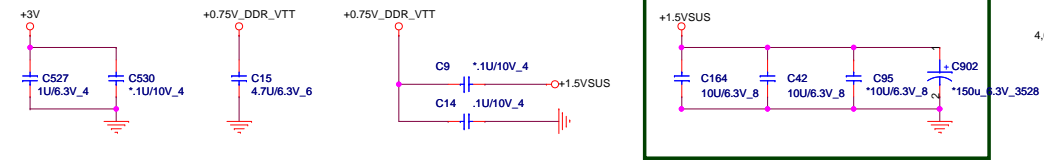
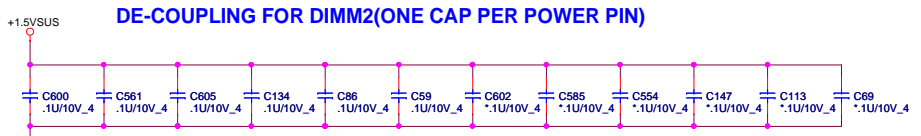
+1.5VSUS 3,4,5,6,14,39,40,41,42
+3V 2,3,5,6,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+0.75V_DDR_VTT 6,40



DDR3-DIMM2
H=9.2 footprint: "ddr-c-2013310-204p-1"

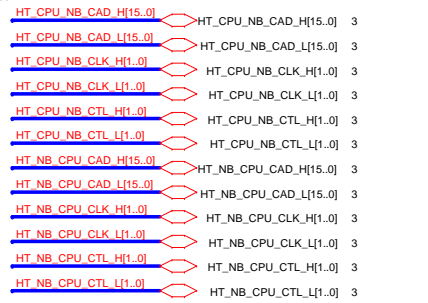
H=9.2 footprint: "ddr-c-2013310-204p-1"
DGMK4000058

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

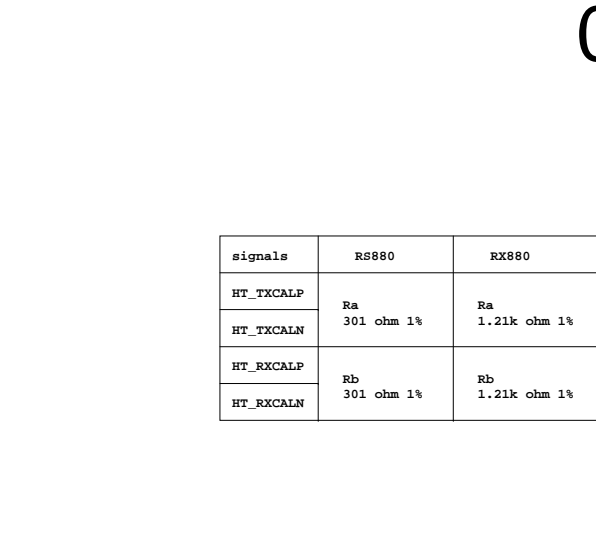


	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
	Document Number	DDR3 SODIMMS TERMINATIONS	
Size Custom	Date: Monday, September 28, 2009	Sheet 7 of 46	

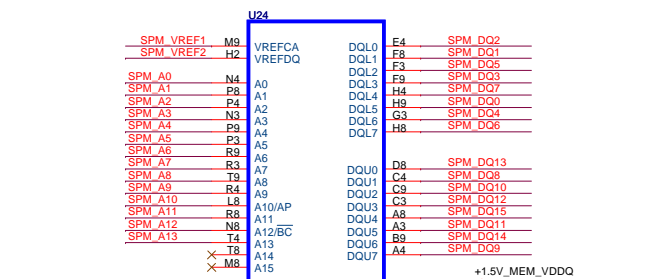
+1.5V 3,11,34,42
 +1.8V 5,10,11,16,26,42
 +1.1V 2,3,9,10,11,15,38



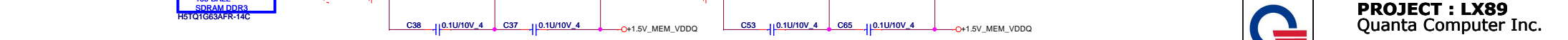
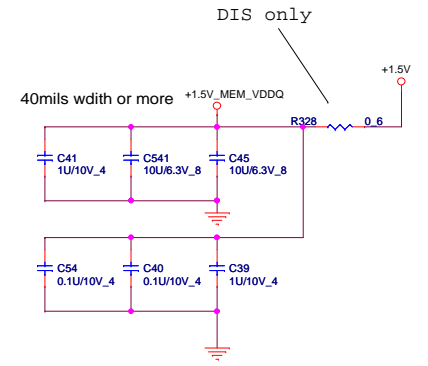
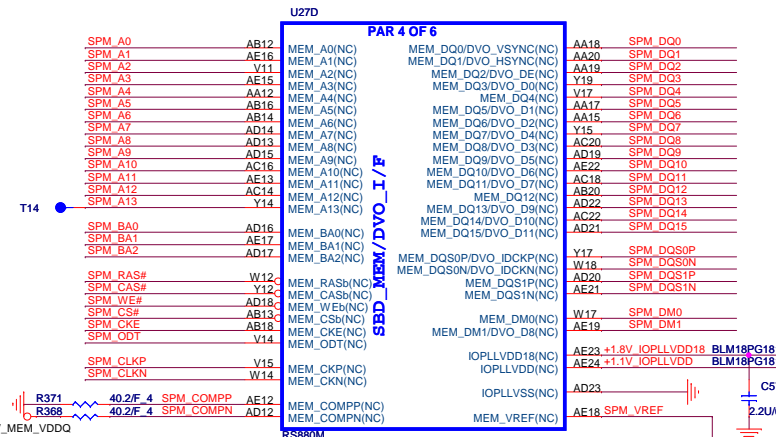
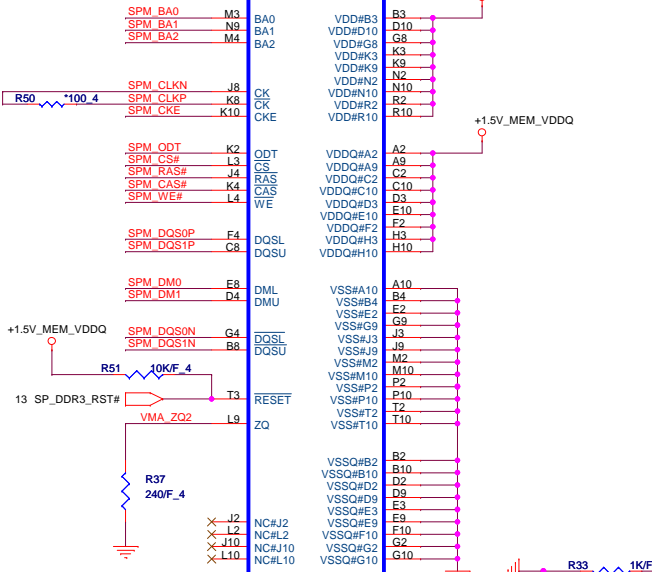
HYPER TRANSPORT CPU I/F



signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		



This block is for UMA only , DIS can remove all component

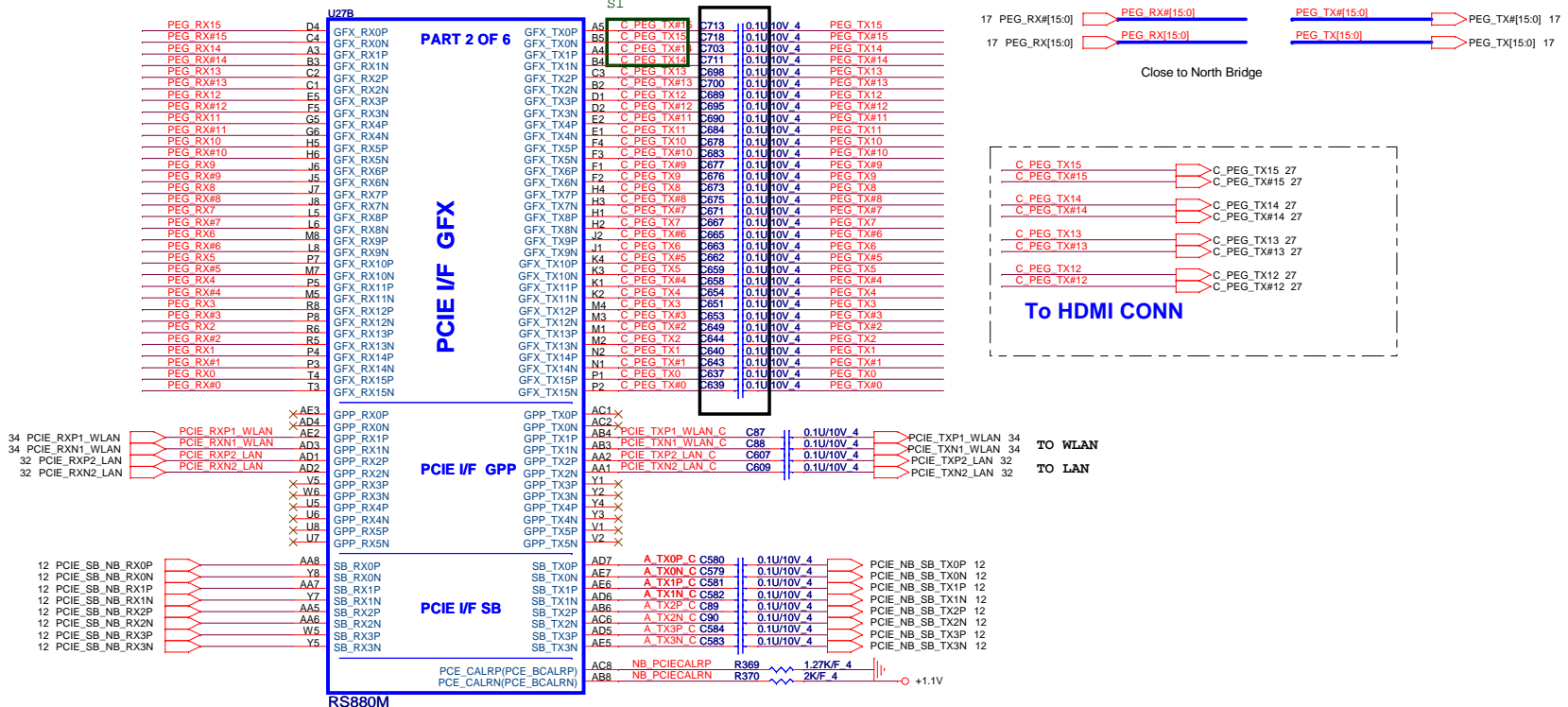


PROJECT : LX89
 Quanta Computer Inc.

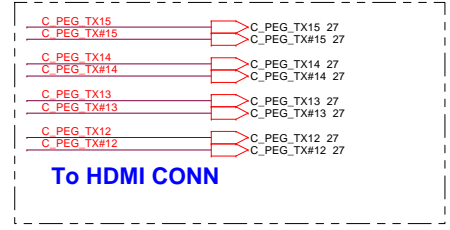
Size Custom	Document Number RS880-HT LINK I/F 1/5	Rev 1A
Date: Monday, September 28, 2009		Sheet 8 of 46

UMA Remove All Cap

Swap pin for Layout



Close to North Bridge



RS880M

RS880 Display Port Support (muxed on GFX)

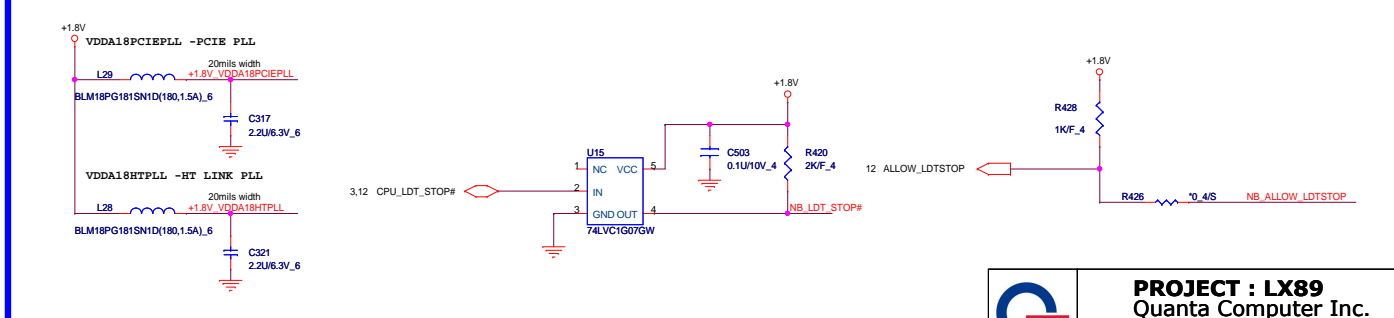
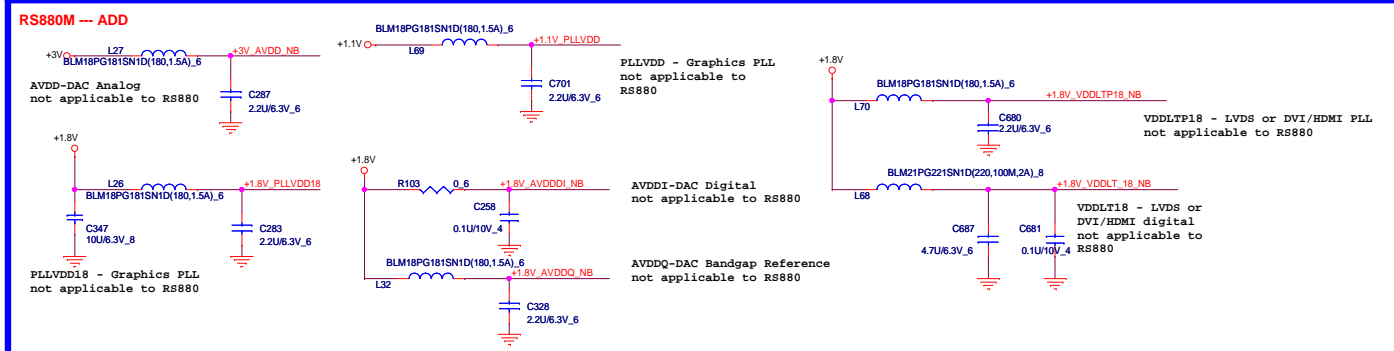
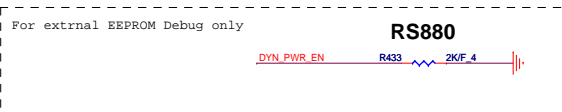
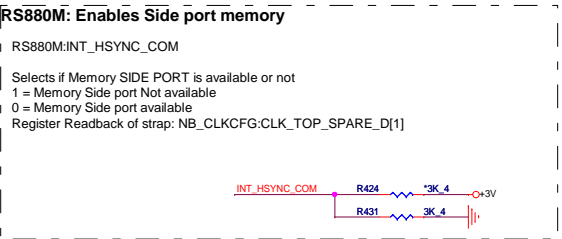
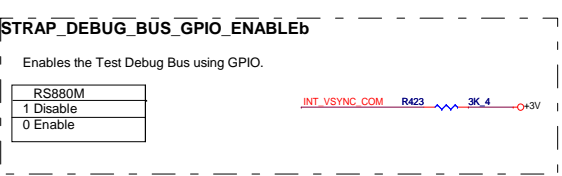
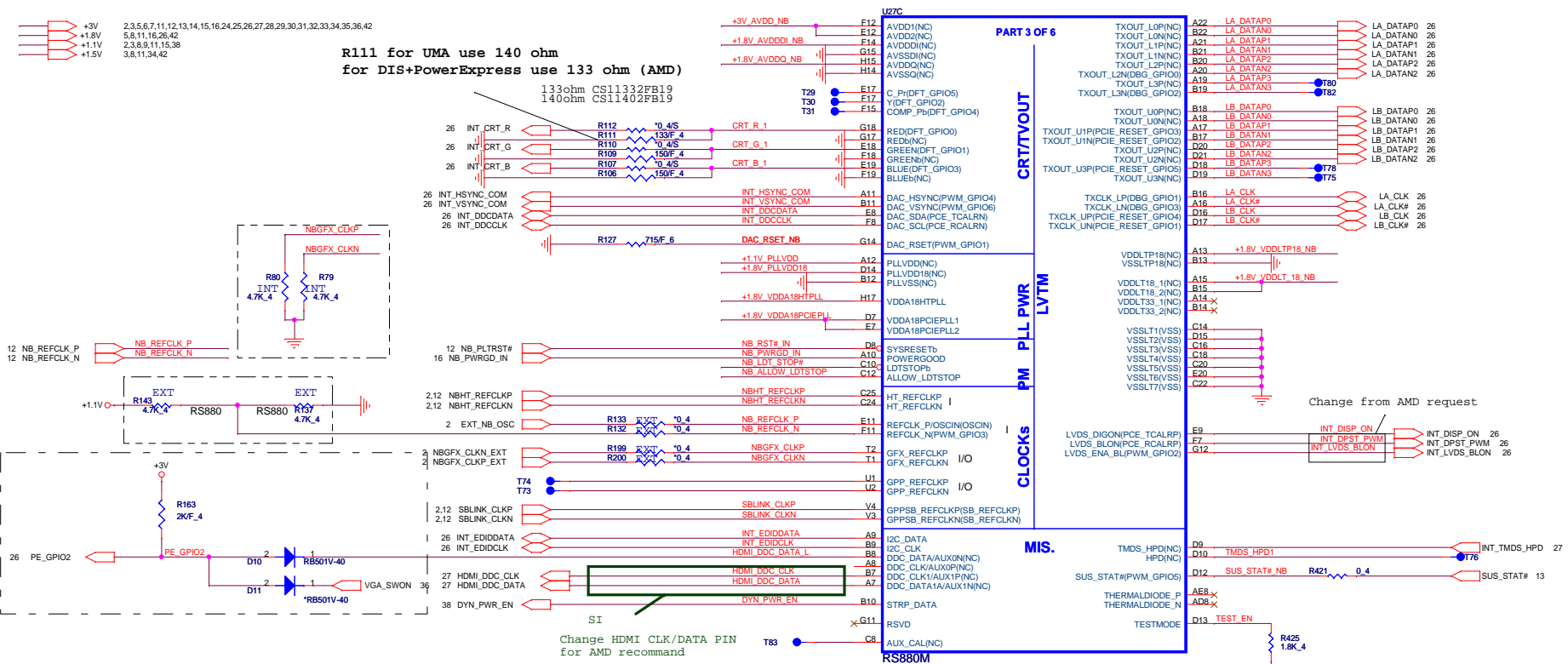
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

<p>NBS/RD2</p>	<p>PROJECT : LX89 Quanta Computer Inc.</p>		<p>Rev 1A</p>	
	<p>Size Custom</p>	<p>Document Number RS880-PCIE I/F 2/5</p>		<p>Date: Monday, September 28, 2009</p>
	<p>Sheet 9</p>	<p>of 46</p>		<p>1</p>

+3V	2,3,5,6,7,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+1.8V	5,8,11,16,26,42
+1.1V	2,3,8,9,11,15,38
+1.5V	3,8,11,34,42

R111 for UMA use 140 ohm
for DIS+PowerExpress use 133 ohm (AMD)

133ohm CS11332FB19
140ohm CS11402FB19

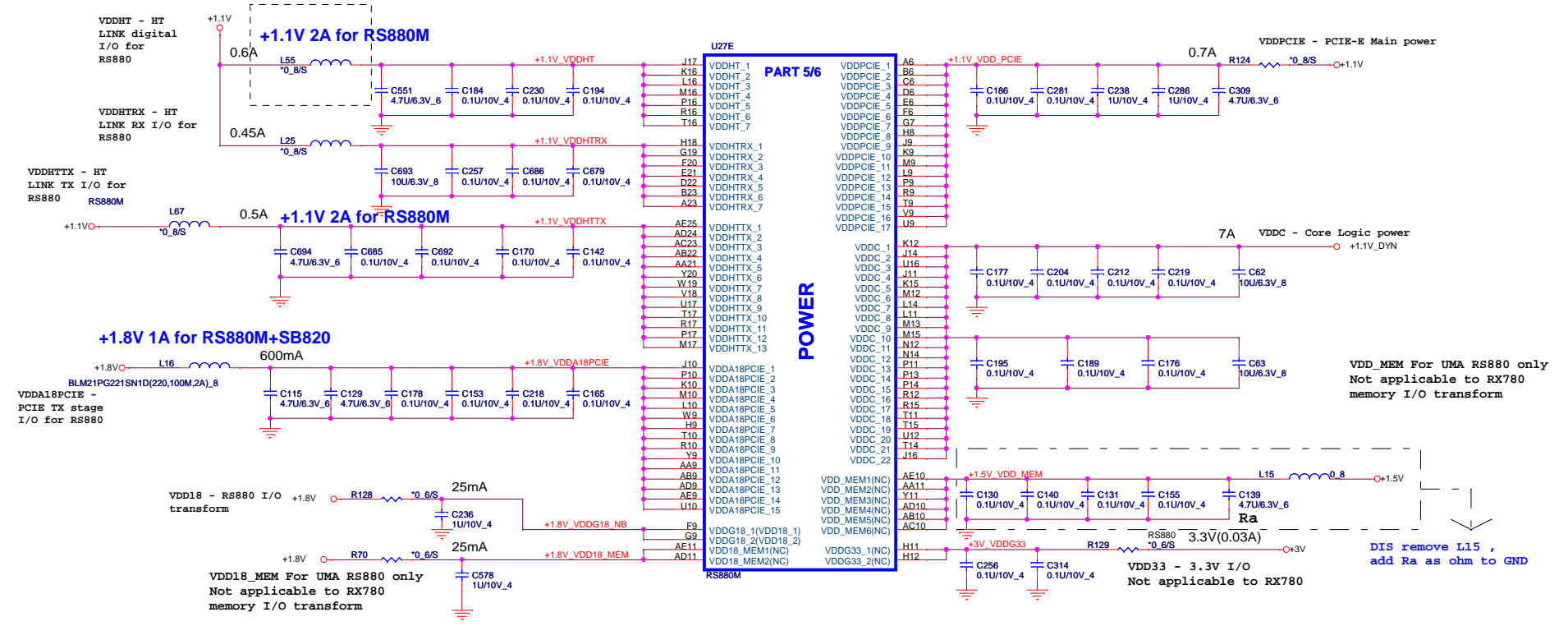
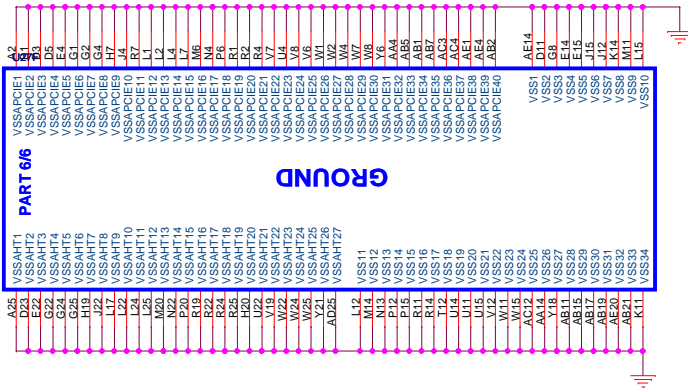


PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev
	RS880-SYSTEM I/F 3/5	1A
Date: Monday, September 28, 2009		Sheet 10 of 46

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC



POWER

VDD_MEM For UMA RS880 only
Not applicable to RX780
memory I/O transform

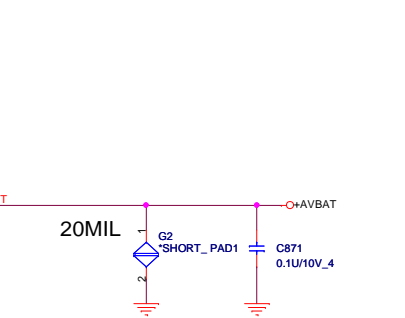
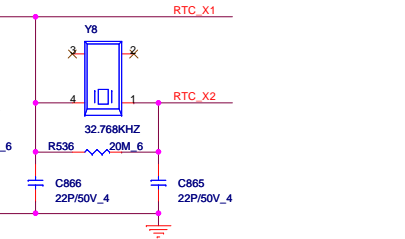
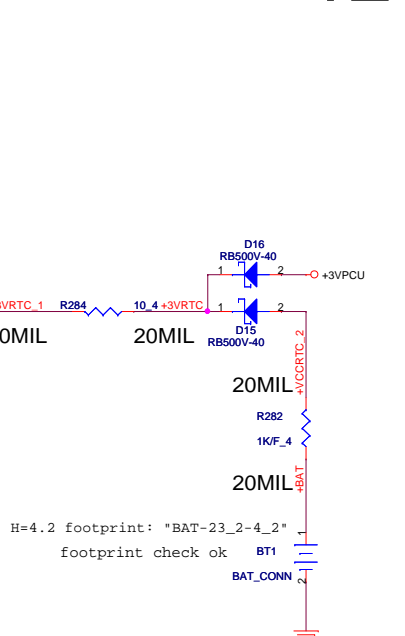
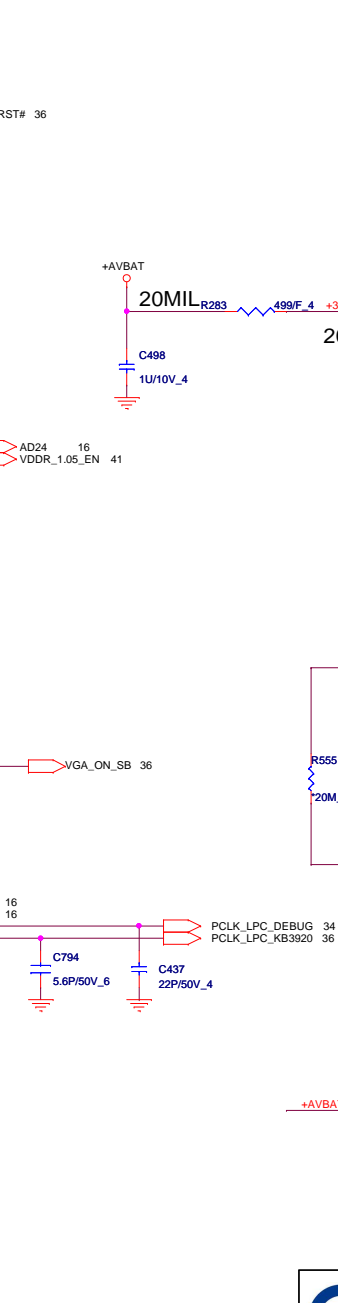
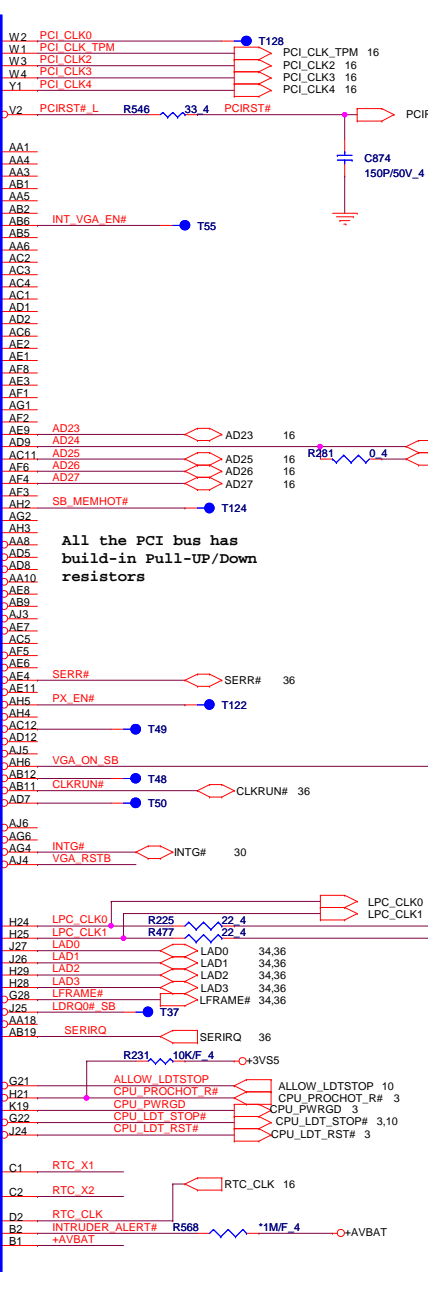
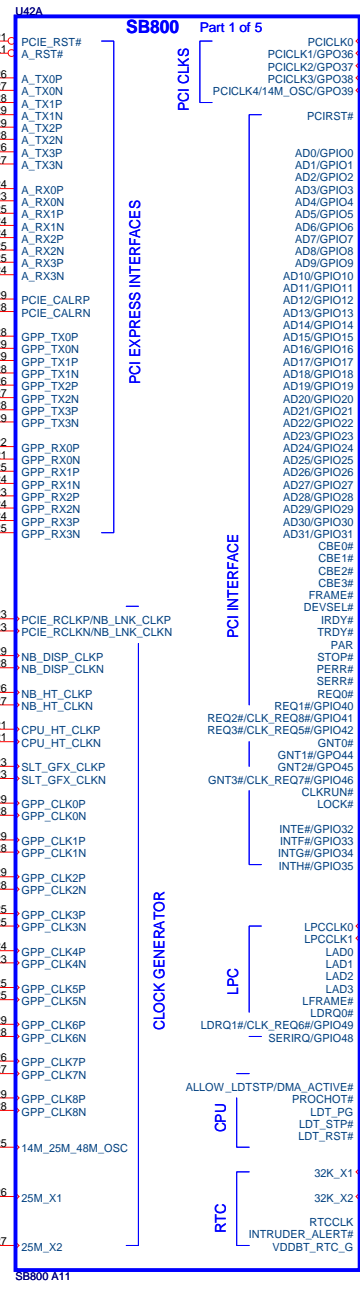
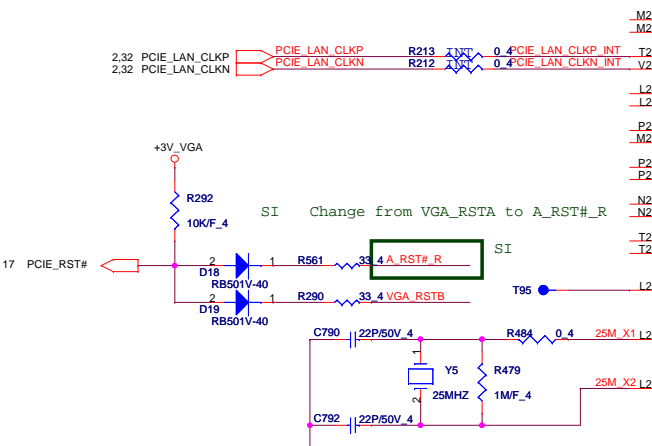
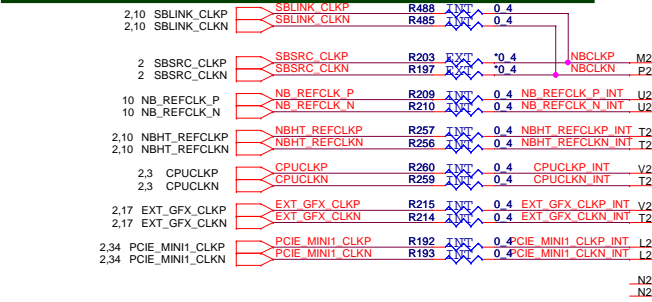
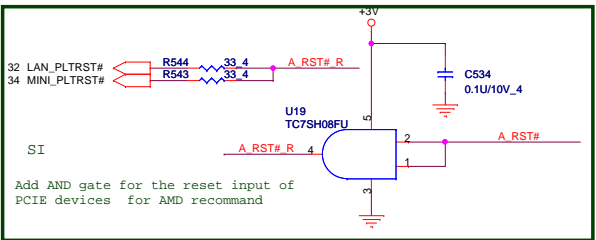
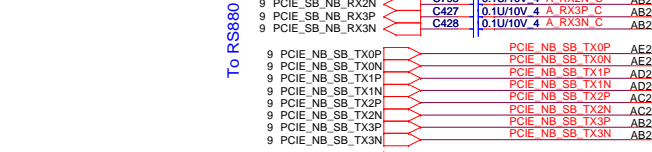
DIS remove L15 ,
add Ra as ohm to GND

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number RS880-POWER5/5	Rev 1A
Date: Monday, September 28, 2009		Sheet 11 of 46

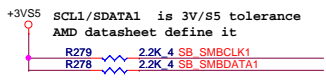
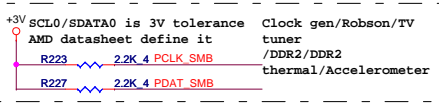
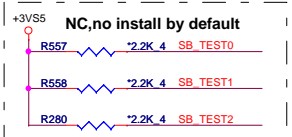
+1.1V_PCIE_VDDR 15
+3V_VGA 21,41
+3VS5 5,13,14,15,16,42
+3VPCU 4,6,24,33,35,36,37,38,39,40,41,42,43

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U7007

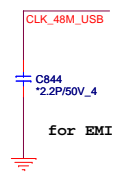
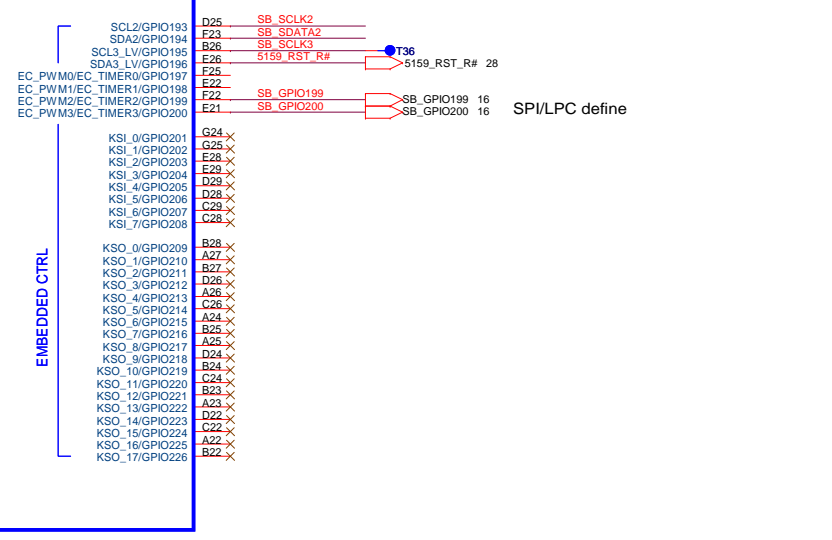
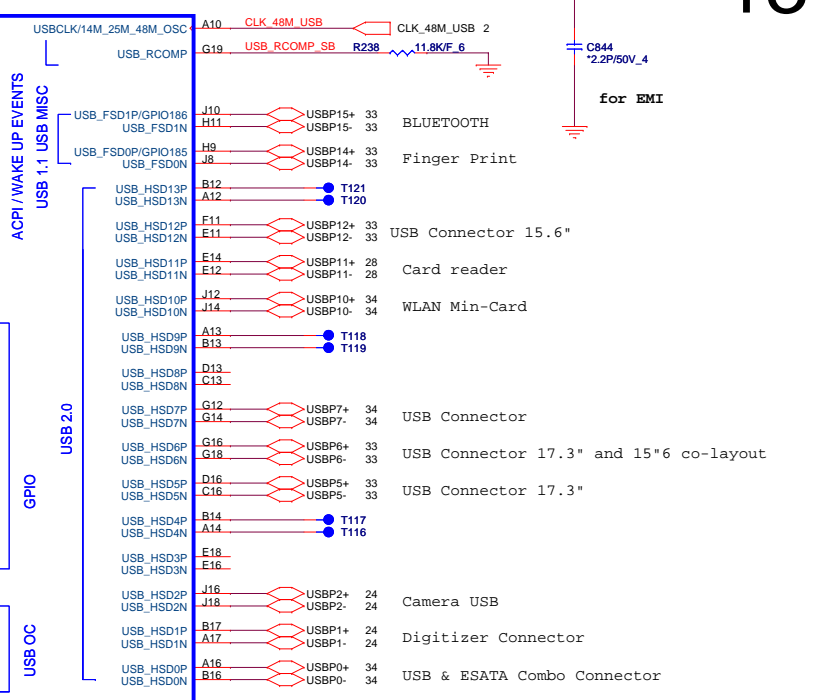
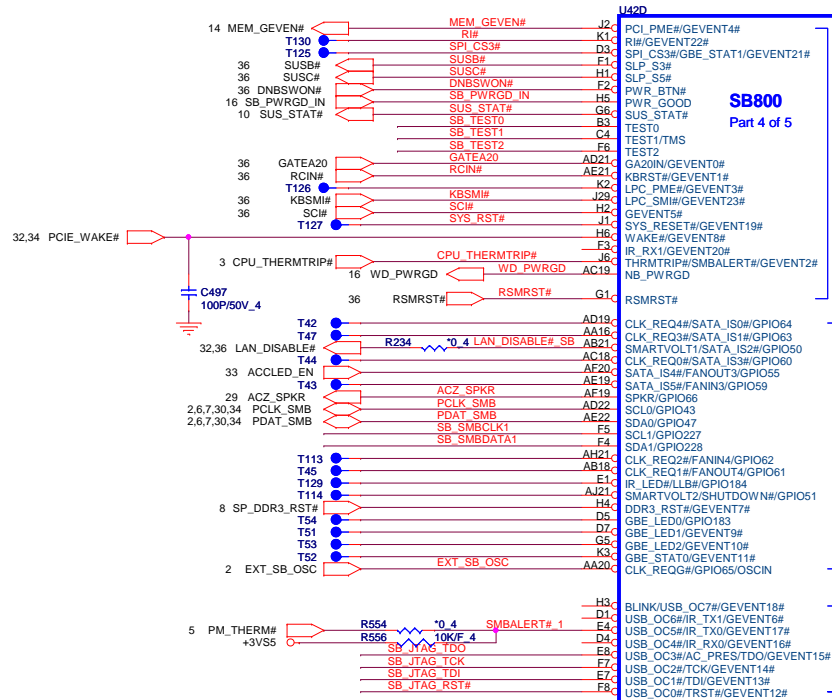
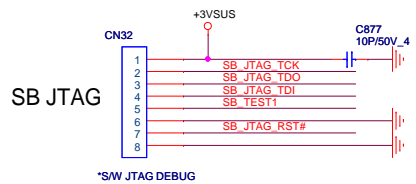
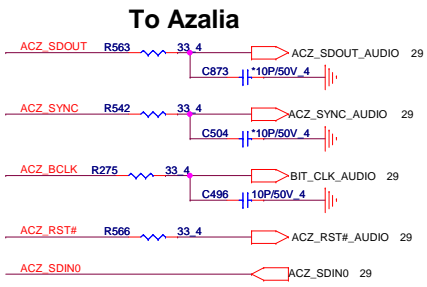
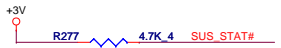
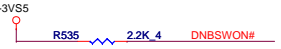
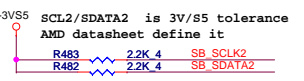


INTRUDER_ALERT# Left not connected (southbridge has 50-kohm internal pull-up to VBAT).

PROJECT : LX89
Quanta Computer Inc.
Size Custom Document Number SB820-PCIE/PCICPU/LPC 1/4 Rev 1A
Date: Monday, September 28, 2009 Sheet 12 of 46



remove pull hi
 (chip internal
 have pull hi)



for EMI



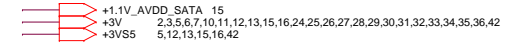
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SB820-ACPI/USB 2/4	Rev 1A
Date: Monday, September 28, 2009	Sheet 13	of 46

SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY



SATA1 HDD



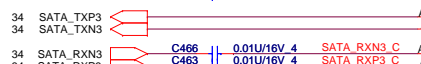
SATA ODD



SATA2 HDD



E-SATA



XTLVDD_SATA-- SATA
crystal power

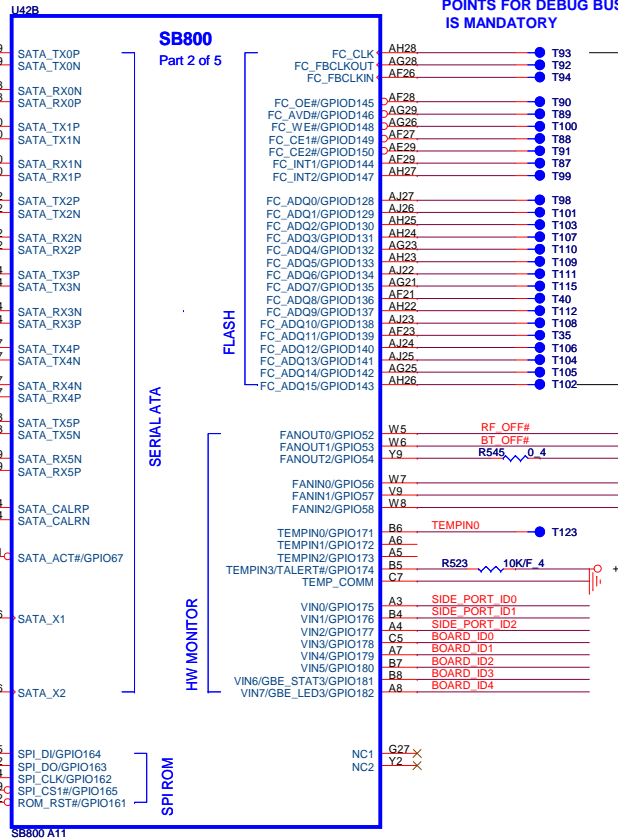
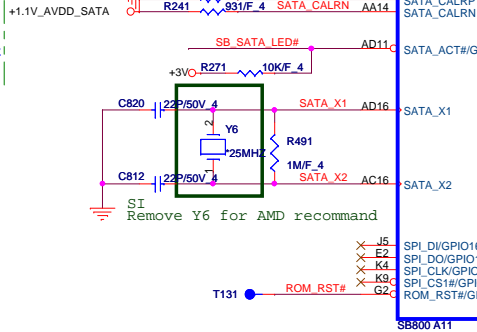
PLVDD_SATA--
SATA PLL
POWER



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

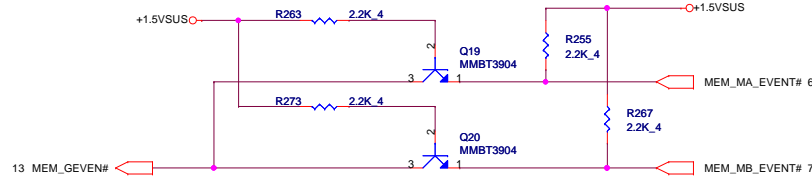
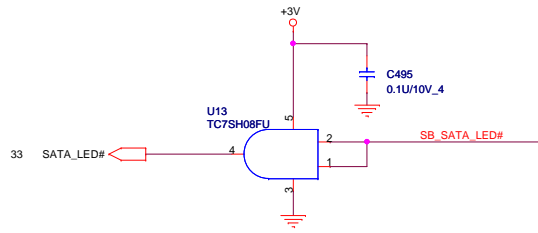
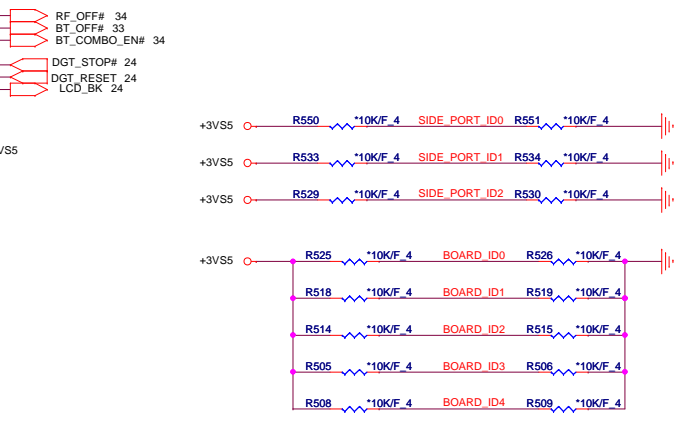
NOTE:

R361 IS 1K 1% FOR 25MHz
XTAL. 4.99K 1% FOR 100MHz
INTERNAL CLOCK



IF USE, power need ready

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port



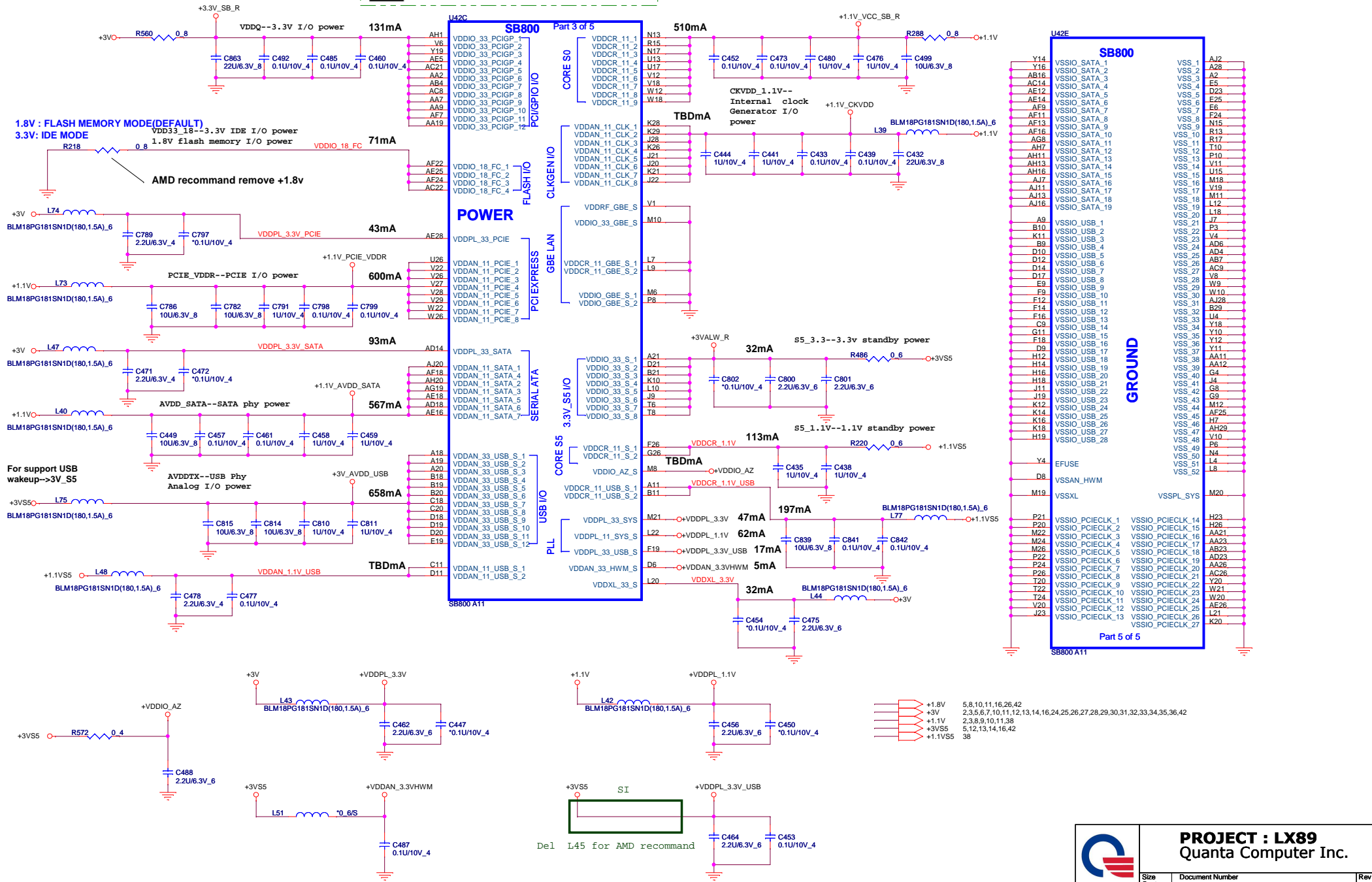
ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	LX8 UMA
0	0	0	0	1	LX9 UMA
0	0	0	1	0	LX8 Madison
0	0	0	1	1	LX8 Park
0	0	1	0	0	LX9 Park
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SB820-ACPI/GPIO/USB 2/J4	Rev 1A
Date: Monday, September 28, 2009 Sheet 14 of 46		

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power



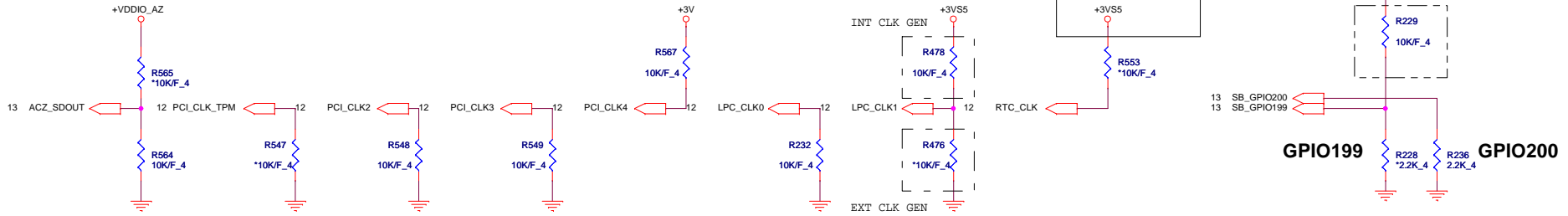
- 1.8V 5,8,10,11,16,26,42
- +3V 2,3,5,6,7,10,11,12,13,14,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
- +1.1V 2,3,8,9,10,11,38
- +3VSS 5,12,13,14,16,42
- +1.1VSS 38

Del L45 for AMD recommend

	PROJECT : LX89	
	Quanta Computer Inc.	
	Size Custom Document Number SB820-PWR/DECOUPLING 4/4 Date: Monday, September 28, 2009	Rev 1A Sheet 15 of 46

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



It must ready before RSMRST#

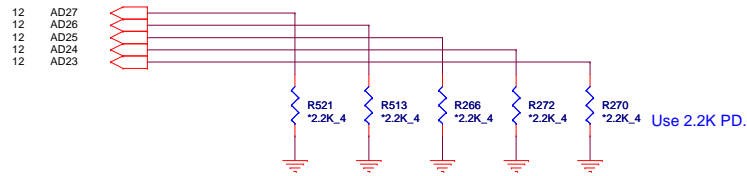
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

TYPE	GPIO199	GPIO200
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

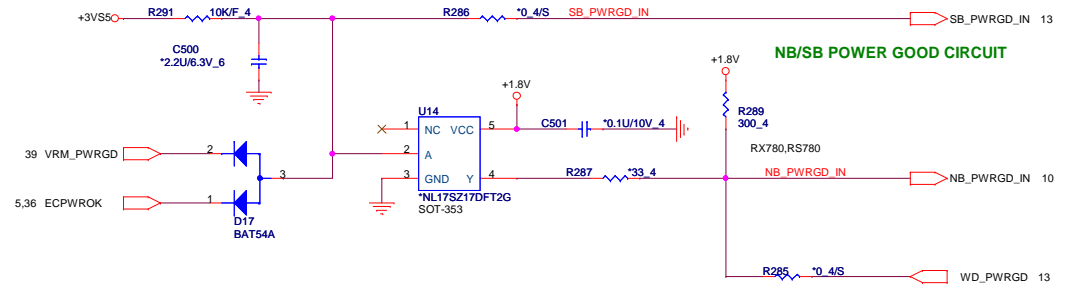
DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



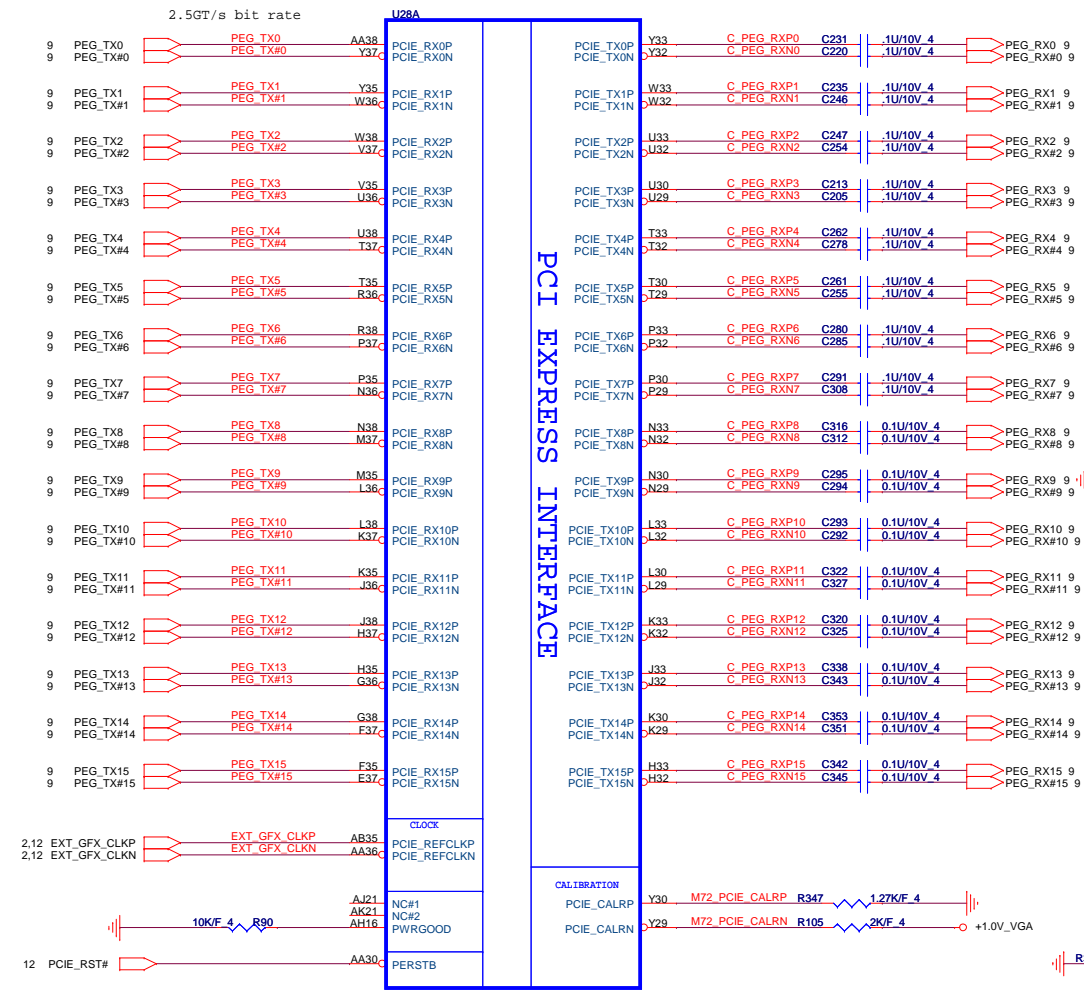
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

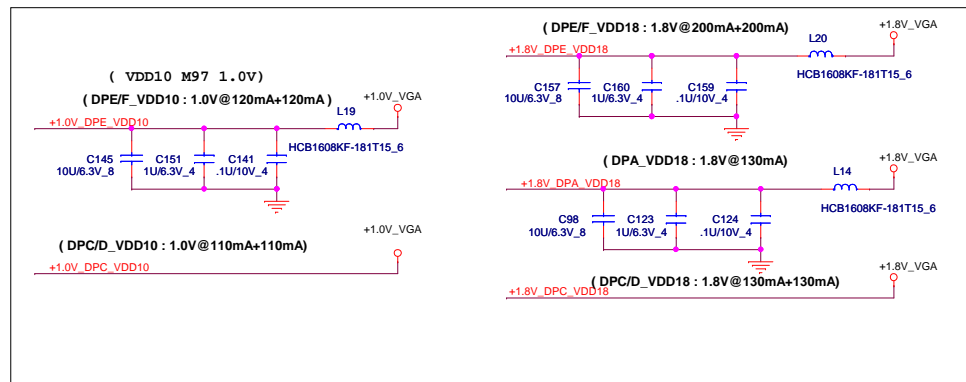
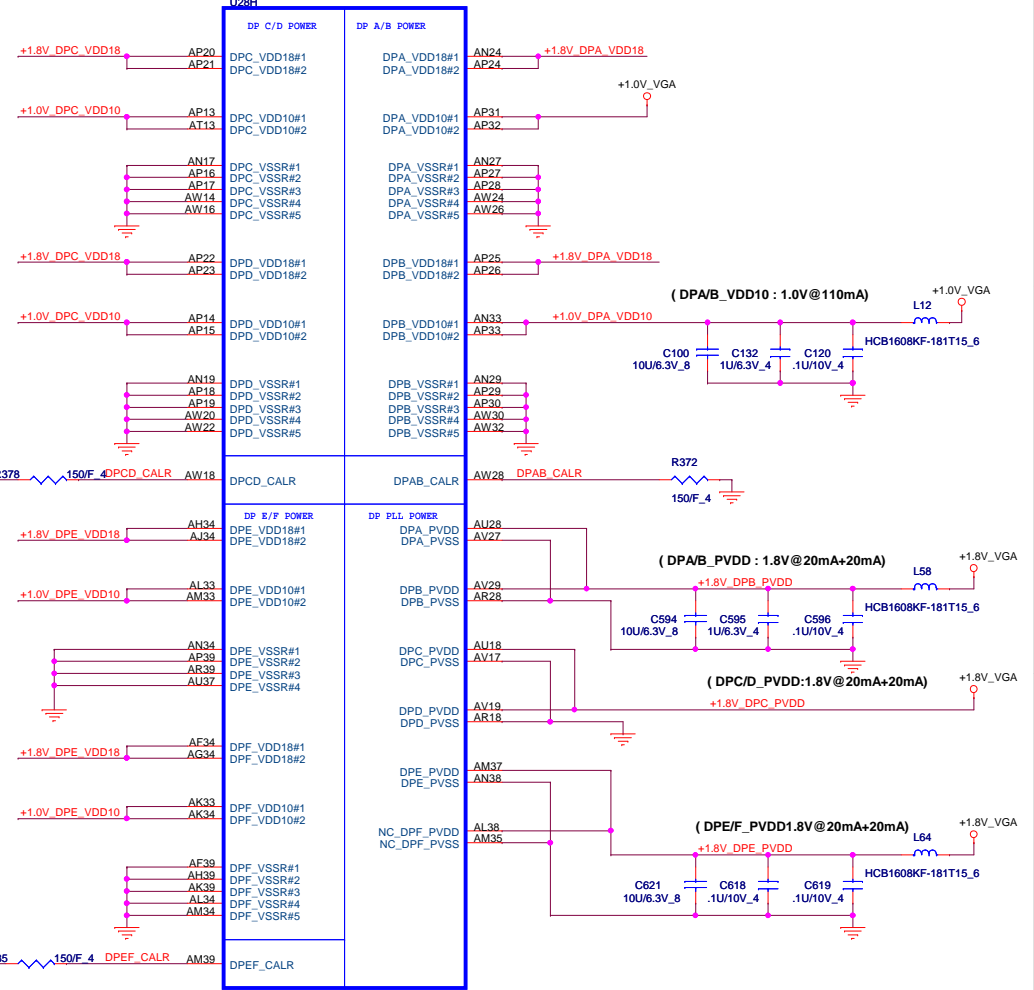


AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	SB820-STRAPS	
NB5/RD2	Date: Monday, September 28, 2009	Sheet 16	of 46



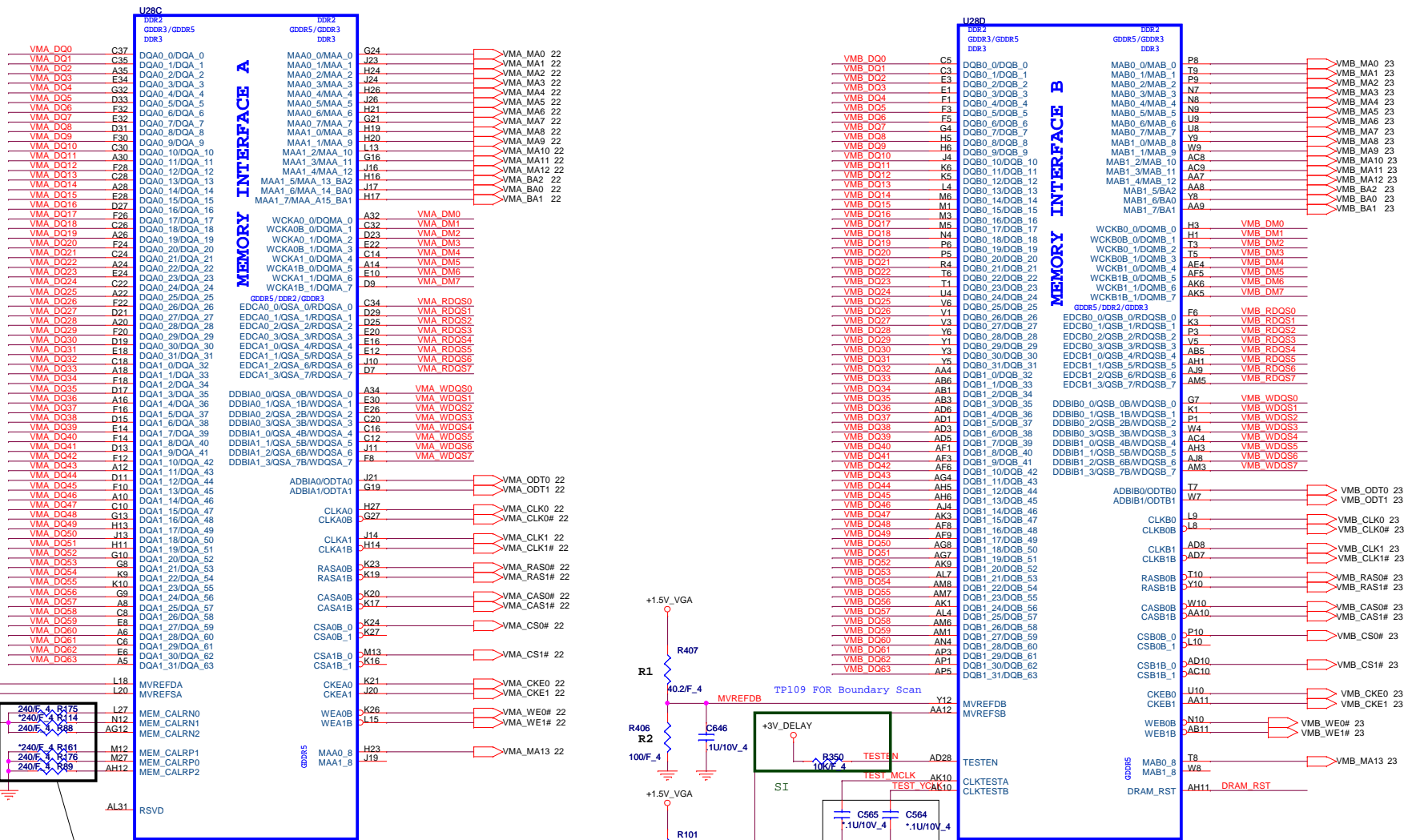
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing



PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number ATI Park/Madison (PCIE I/F) 1/5	Rev 1A
Date: Monday, September 28, 2009	Sheet 17 of 46	

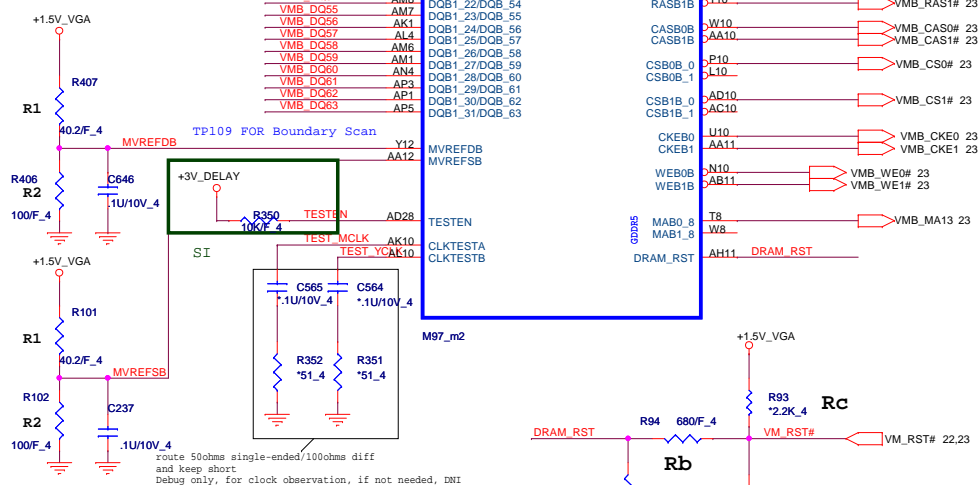
NBS/RDZ



	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
R1	40.2R	40.2R	40.2R
R2	100R	100R	100R

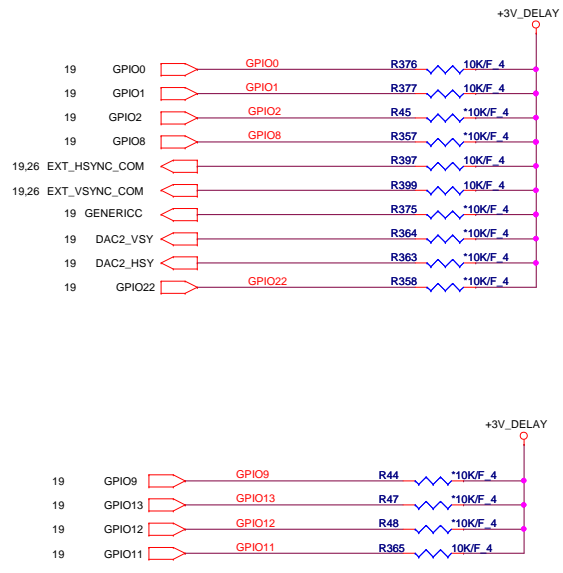
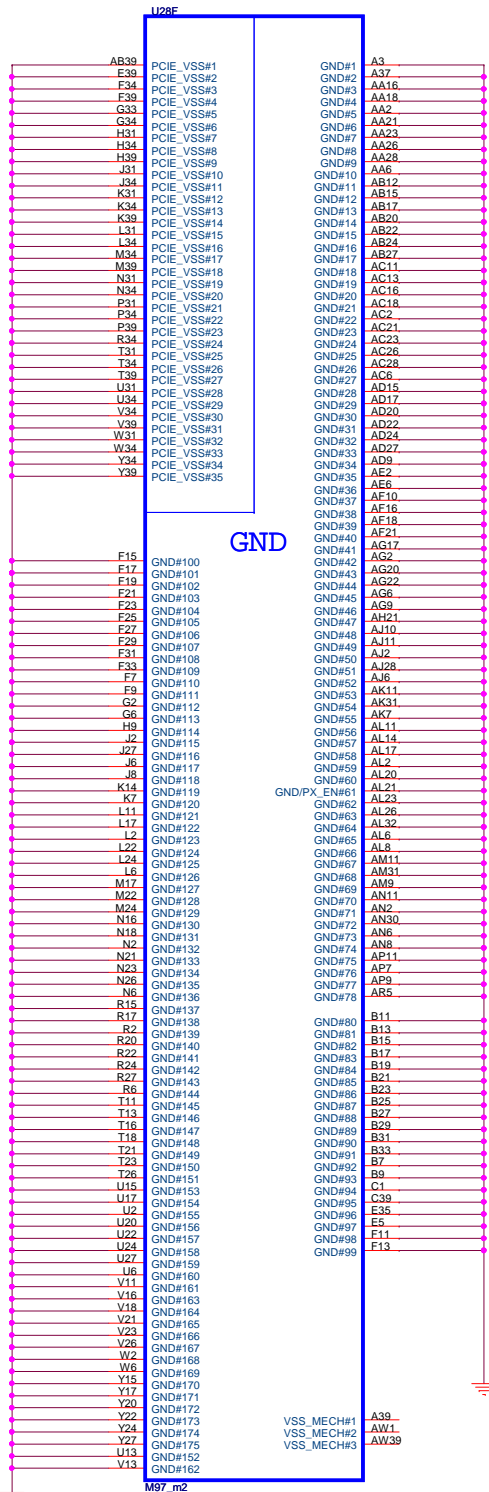
- 22 VMA_DQ[63..0]
- 22 VMA_DM[7..0]
- 22 VMA_DQS[7..0]
- 22 VMA_RDQS[7..0]
- 23 VMB_DQ[63..0]
- 23 VMB_DM[7..0]
- 23 VMB_DQS[7..0]
- 23 VMB_RDQS[7..0]
- 21,22,23,40 +1.5V_VGA



Designator	For M97-M2	For Manhattan
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Date: Monday, September 28, 2009	ATI Park/Madison (MEM VF) 2/5	Sheet 16 of 46



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2,0)	GPIO{13:11}	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

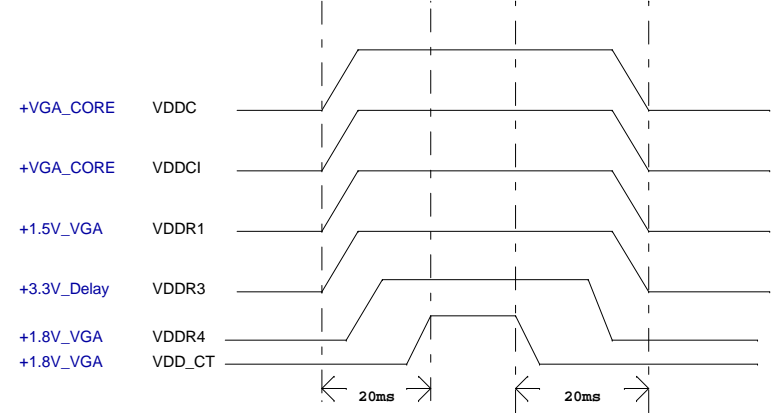
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
H2SYNC	GENERICC		
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
	GPIO21_BB_EN		

Memory Aperture size fix 256M

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

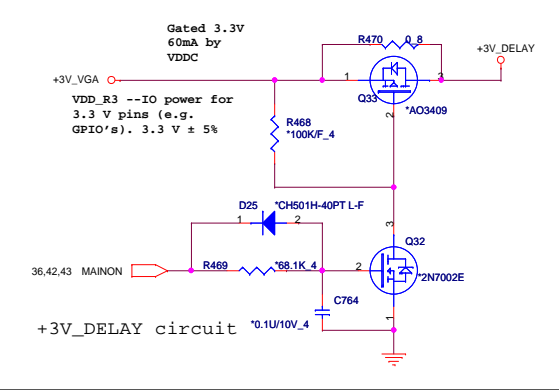
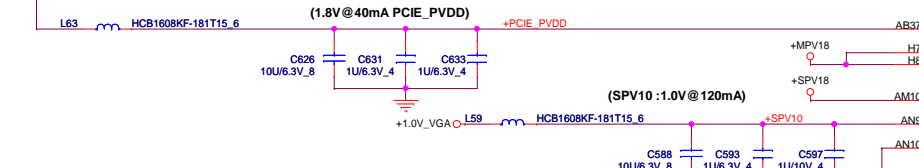
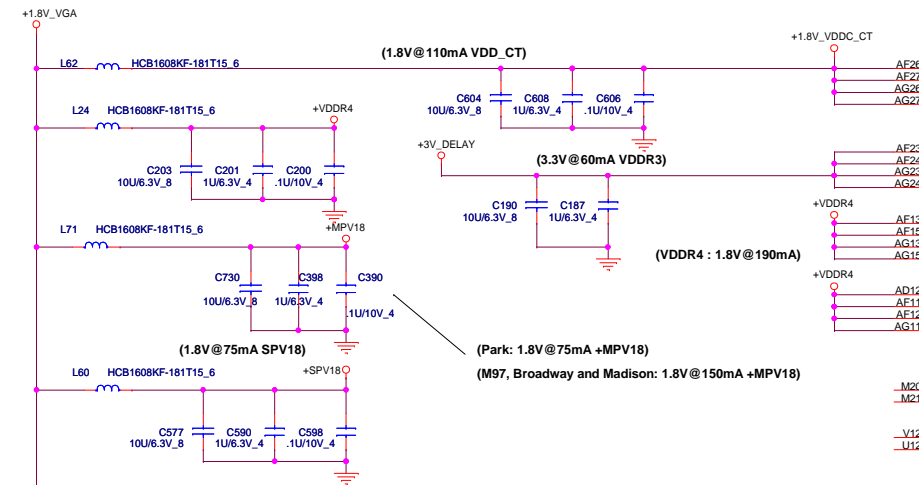
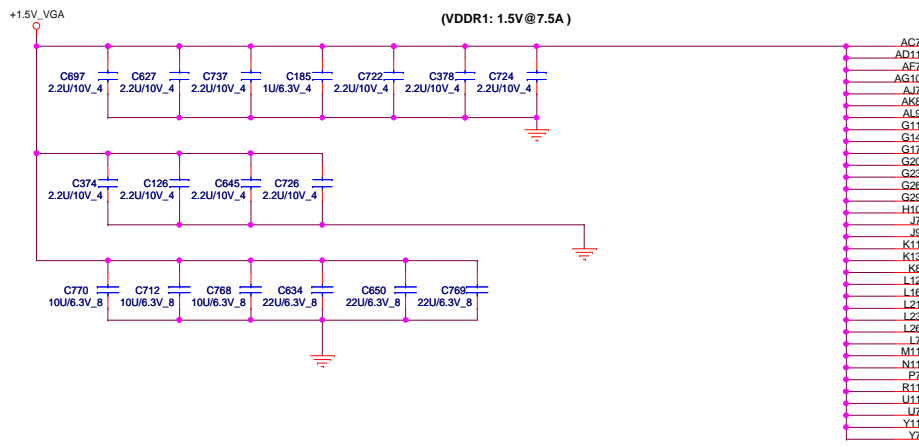
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



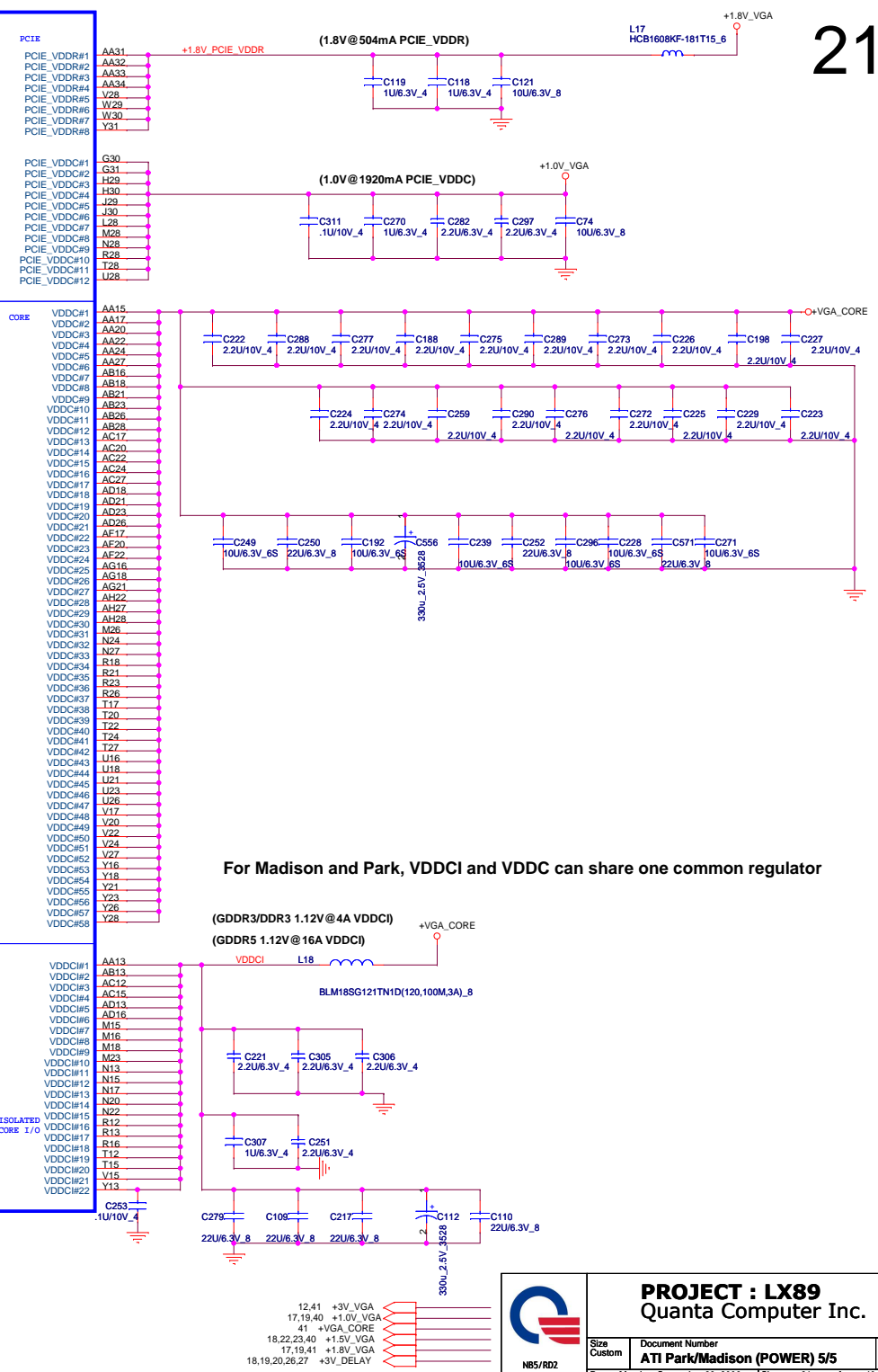
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number ATI Park/Madison(GND&Str&Ther)4/5	Rev 1A
Date: Monday, September 28, 2009	Sheet 20 of 46	



I/O	
AG7	VDDR1#1
AD11	VDDR1#2
AF7	VDDR1#3
AG10	VDDR1#4
AJ7	VDDR1#5
AK8	VDDR1#6
AL9	VDDR1#7
G11	VDDR1#8
G14	VDDR1#9
G17	VDDR1#10
G20	VDDR1#11
G23	VDDR1#12
G26	VDDR1#13
G29	VDDR1#14
H10	VDDR1#15
J7	VDDR1#16
J9	VDDR1#17
K11	VDDR1#18
K13	VDDR1#19
K8	VDDR1#20
L12	VDDR1#21
L16	VDDR1#22
L21	VDDR1#23
L23	VDDR1#24
L26	VDDR1#25
L7	VDDR1#26
M11	VDDR1#27
N11	VDDR1#28
P7	VDDR1#29
R11	VDDR1#30
U11	VDDR1#31
U7	VDDR1#32
Y11	VDDR1#33
Y7	VDDR1#34
LEVEL TRANSLATION	
AF26	VDD_CT#1
AF27	VDD_CT#2
AG26	VDD_CT#3
AG27	VDD_CT#4
I/O	
AF23	VDDR3#1
AF24	VDDR3#2
AG23	VDDR3#3
AG24	VDDR3#4
I/O	
AF13	VDDR4#4
AF15	VDDR4#5
AG13	VDDR4#7
AG15	VDDR4#8
I/O	
AD12	VDDR4#1
AF11	VDDR4#2
AF12	VDDR4#3
AG11	VDDR4#6
-M20	NC_VDDRHA
-M21	NC_VSSRHA
-Y12	NC_VDDRHB
-U12	NC_VSSRHB
PLL	
AB37	PCIE_PVDD
H7	MPV18#1
H8	MPV18#2
AM10	SPV18
AN9	SPV10
AN10	SPVSS
VOLTAGE SENSE	
AF28	FB_VDDC
AG28	FB_VDDCI
AH29	FB_GND
M87_m2	

POWER

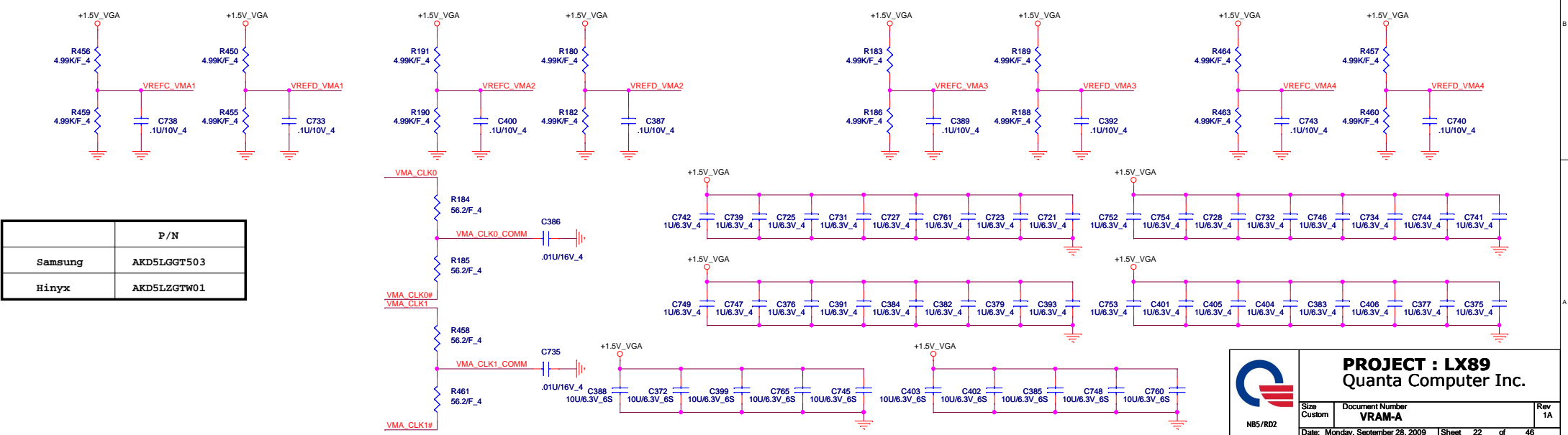
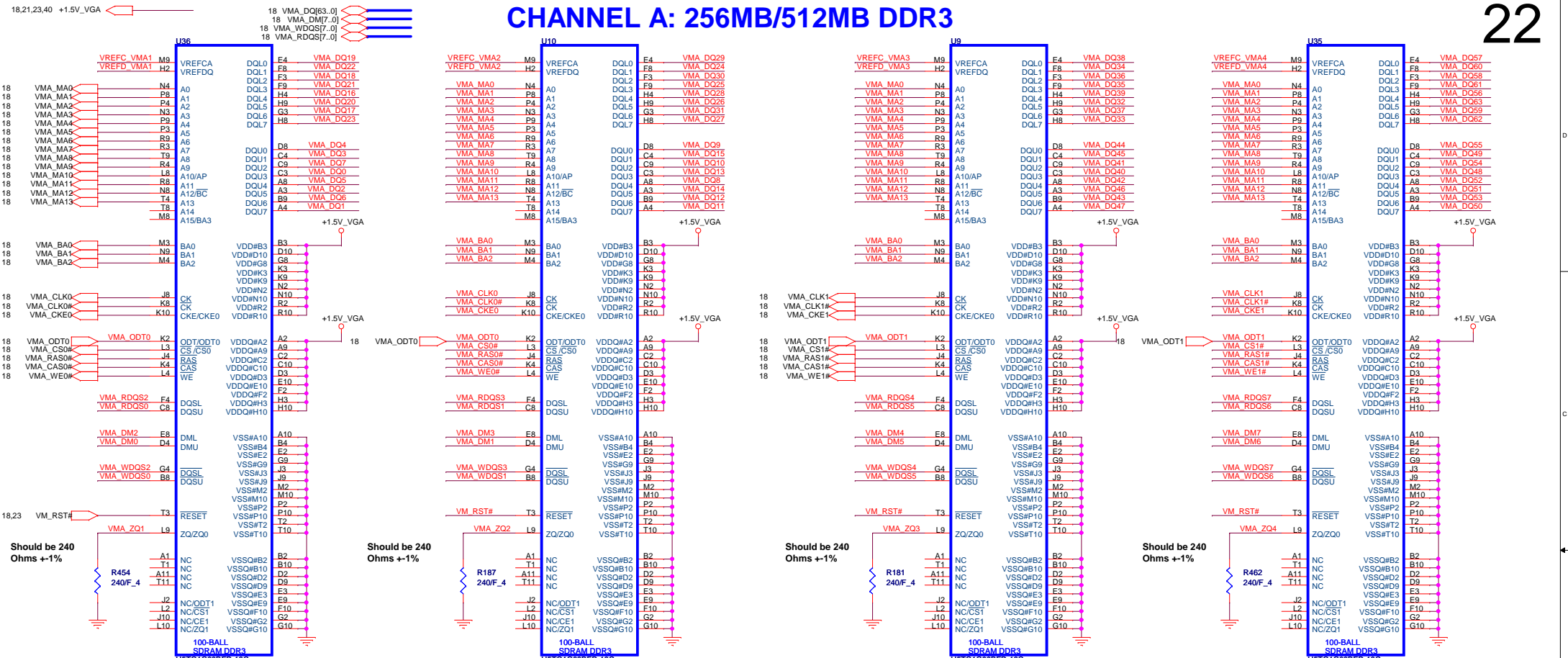


PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number **ATI Park/Madison (POWER) 5/5** Rev 1A

Date: Monday, September 28, 2009 Sheet 21 of 46

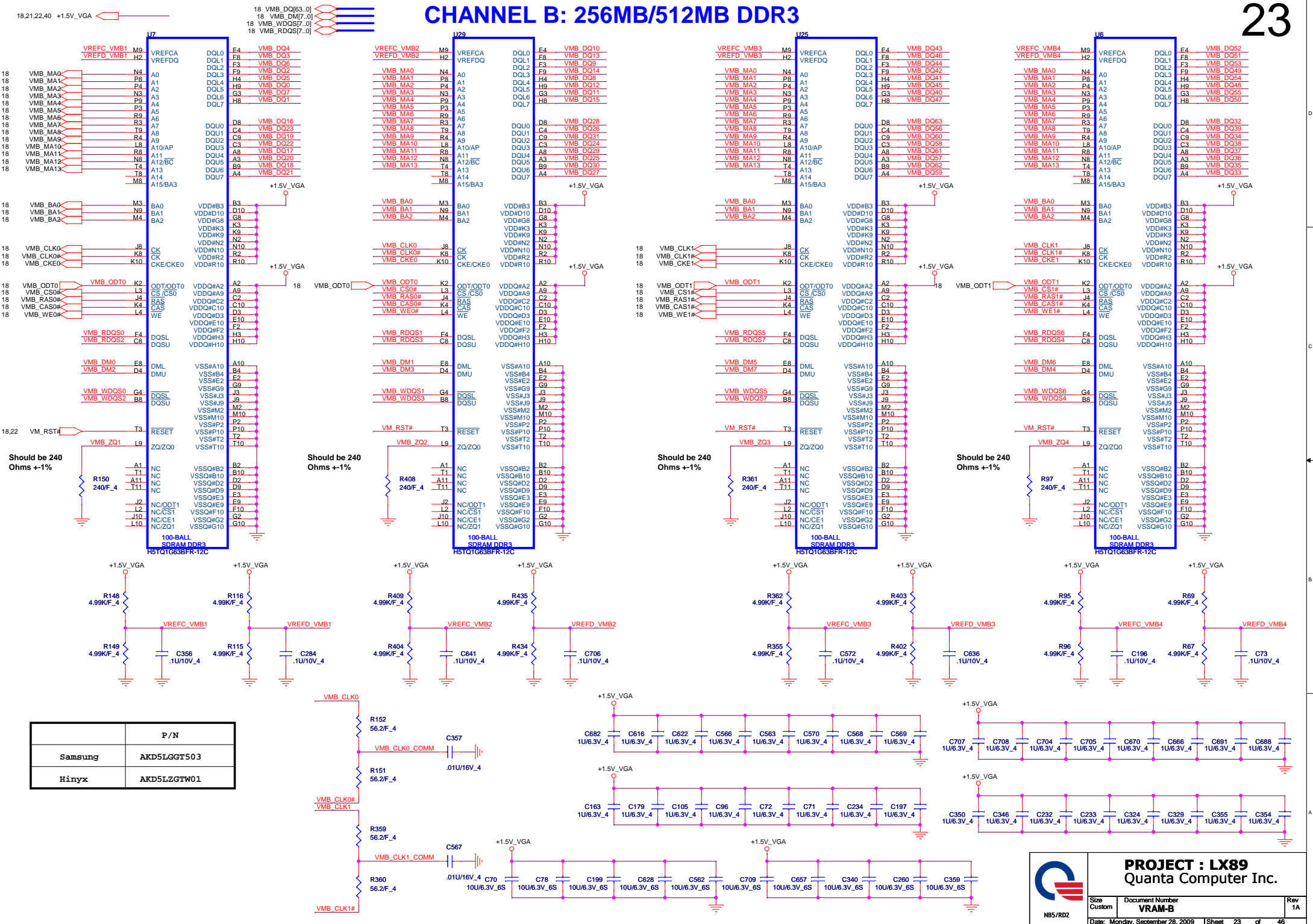
CHANNEL A: 256MB/512MB DDR3



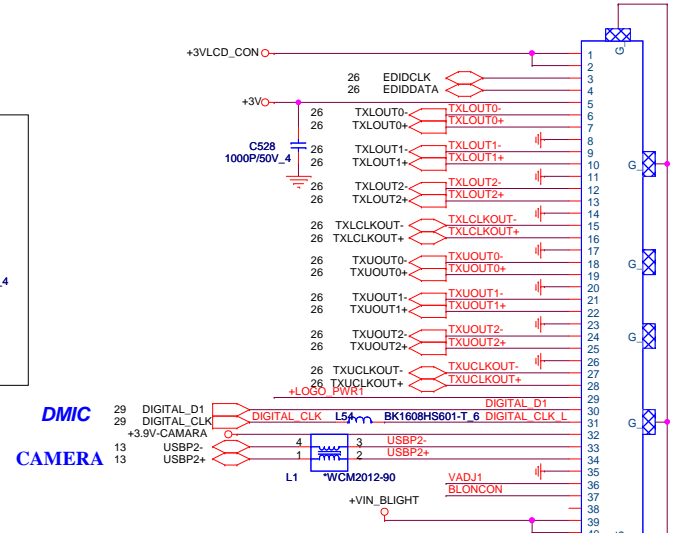
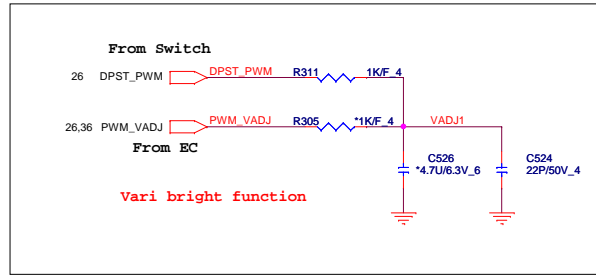
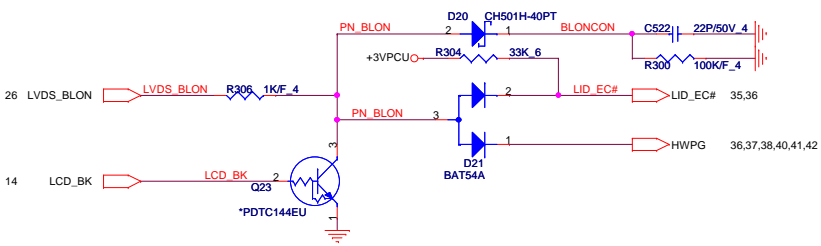
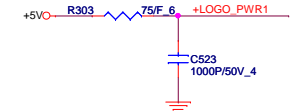
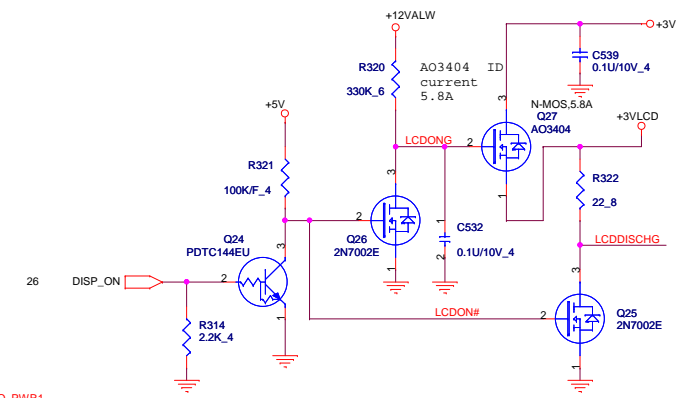
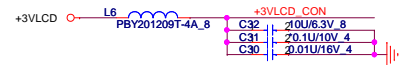
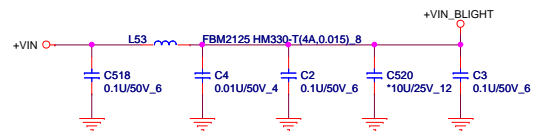
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number VRAM-A	Rev 1A
Date: Monday, September 28, 2009	Sheet 22 of 46	

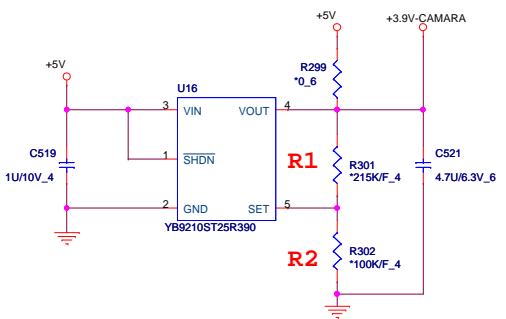
CHANNEL B: 256MB/512MB DDR3



+VIN	31,37,38,39,40,41,42,43
+12VALW	33,35,40,41,42
+3V	2,3,5,6,7,10,11,12,13,14,15,16,25,26,27,28,29,30,31,32,33,34,35,36,42
+3V_DELAY	18,19,20,21,26,27
+5V	25,26,27,28,29,33,34,35,42

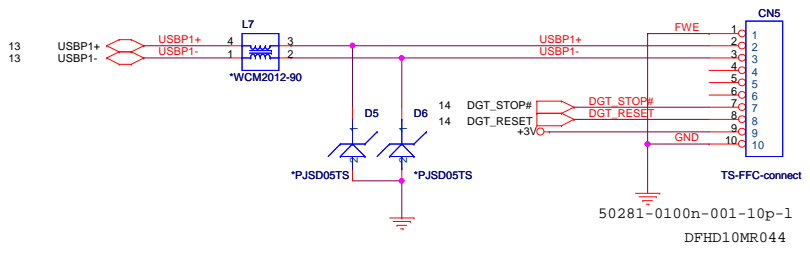


CAMERA POWER



$$V_{out} = 1.25(1 + R1/R2)$$

Digitizer Connector



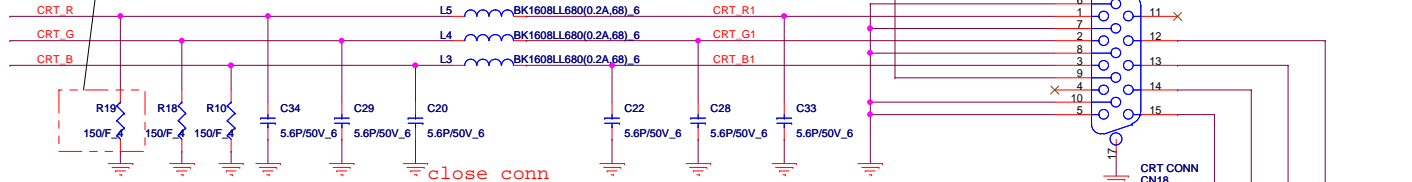
$$V_{out} = 1.25(1 + R1/R2)$$

	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	LCD CONN	
Date: Monday, September 26, 2009		Sheet 24	of 46

CRT PORT

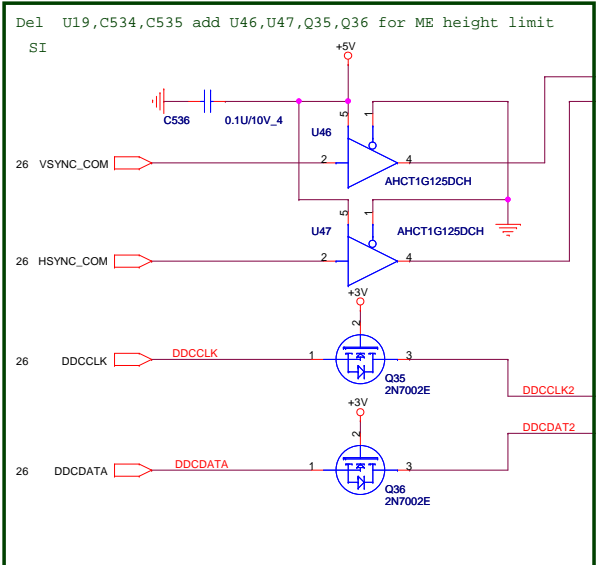
+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,26,27,28,29,30,31,32,33,34,35,36,42
 +5V 24,26,27,28,29,33,34,35,42
 +3V_DELAY 18,19,20,21,26,27

R19 for UMA use 140 ohm
 for DIS+PowerExpress use 150 ohm (AMD)

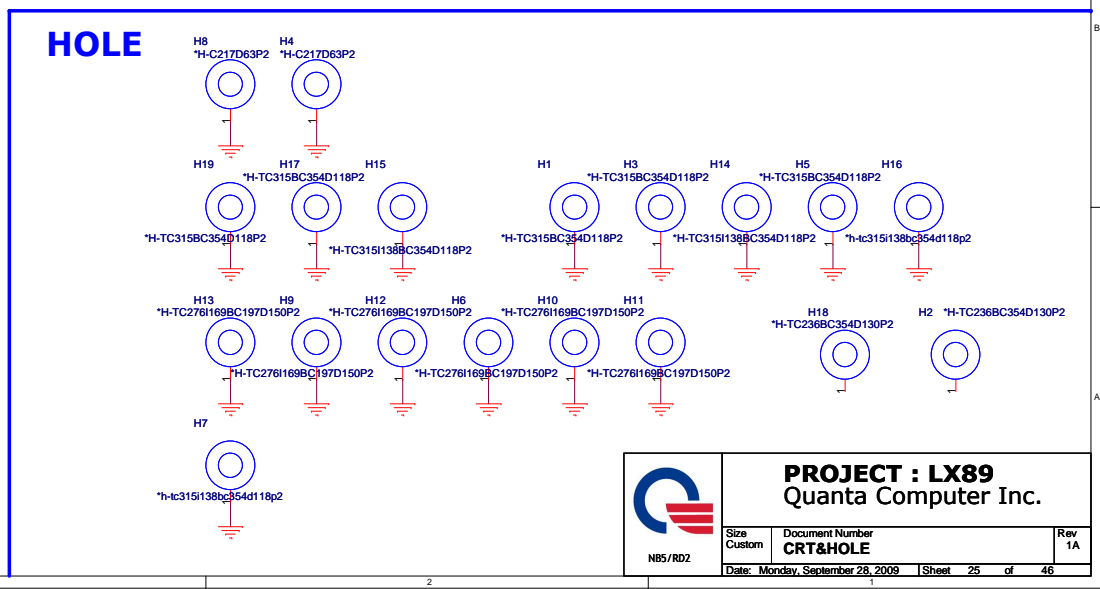
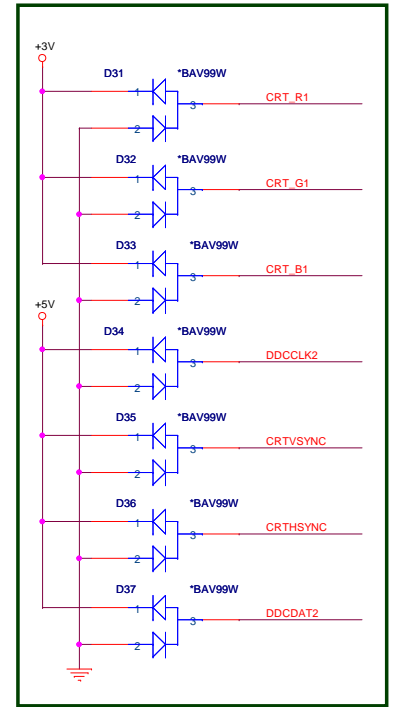


close conn
 within 600mils

26 CRT_R
 26 CRT_G
 26 CRT_B



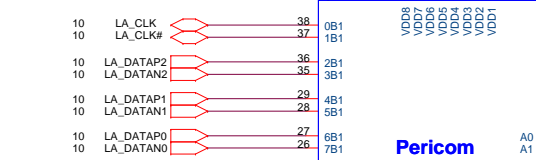
SI Add D31-D37 for ME height limit



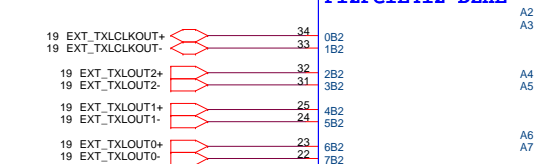
PROJECT : LX89 Quanta Computer Inc.		
Size Custom	Document Number CRT&HOLE	Rev 1A
Date: Monday, September 28, 2009	Sheet 25	of 46

For Single-link panel

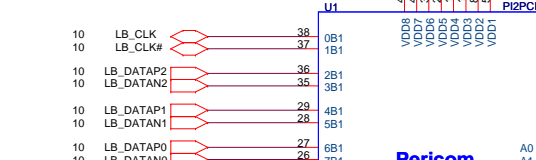
IGPU_Channel-A



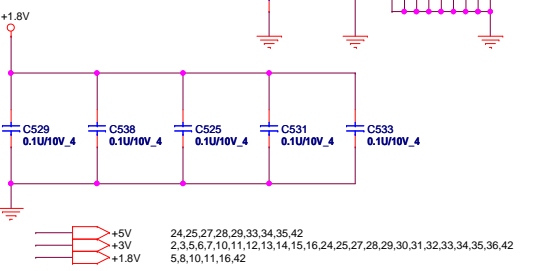
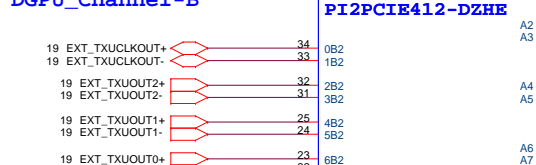
DGPU_Channel-A



IGPU_Channel-B

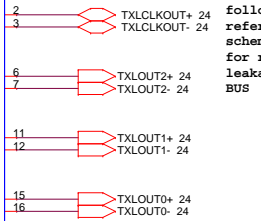


DGPU_Channel-B



LVDS Channel Switch

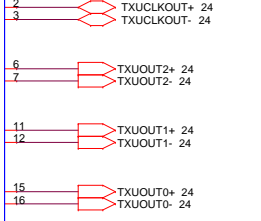
SELx	Ay
HIGH	B2
LOW	B1



SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

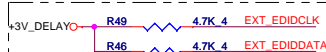
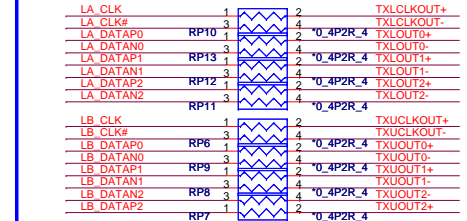
LVDS Channel Switch

SELx	Ay
HIGH	B2
LOW	B1

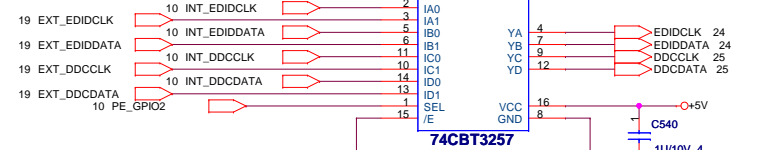


SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

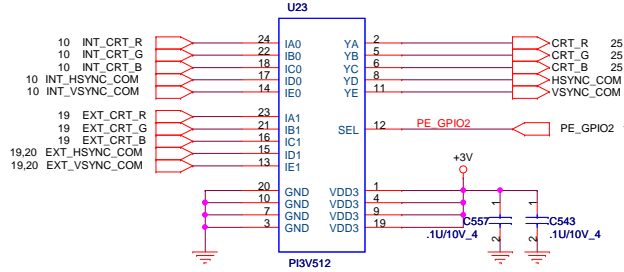
OPTION SIGNAL FROM NB to LVDS for UMA



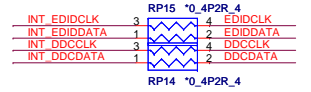
LVDS/CRT DDC Switch



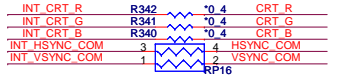
VGA Switch



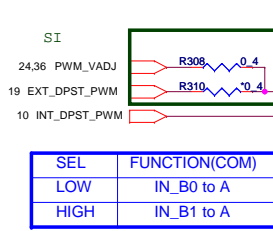
OPTION SIGNAL FROM NB to LVDS/CRT for UMA



OPTION SIGNAL FROM NB to CRT for UMA



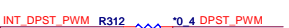
DIS Change Vari bright function from EC control



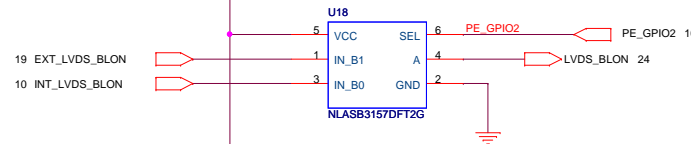
DPST Control

SEL	FUNCTION(COM)
LOW	IN_B0 to A
HIGH	IN_B1 to A

OPTION DPST SIGNAL FROM NB to LVDS for UMA



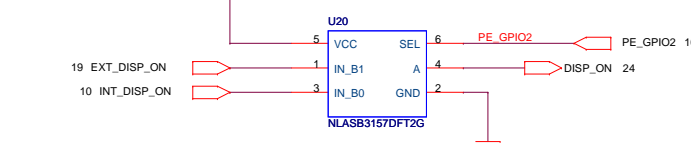
Back Light On control



OPTION Back Light SIGNAL FROM NB to LVDS for UMA



LCDVcc control



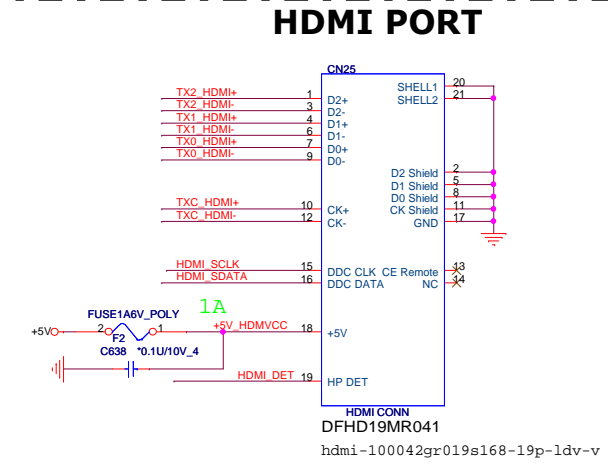
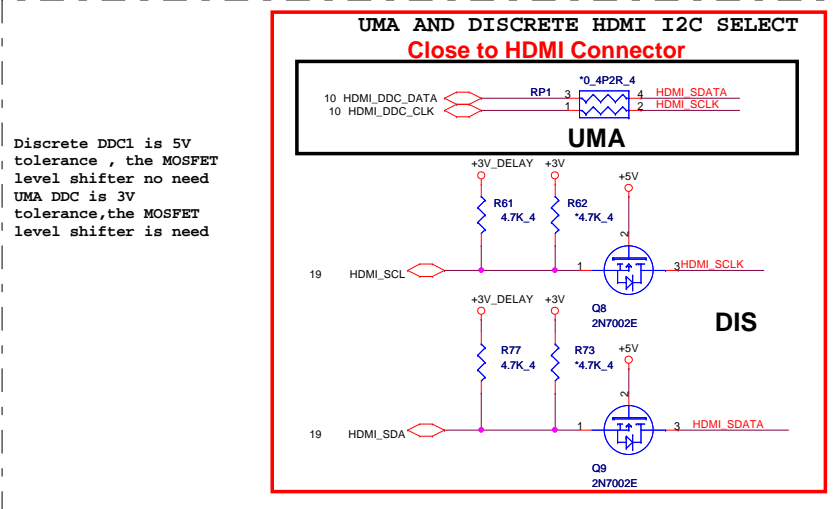
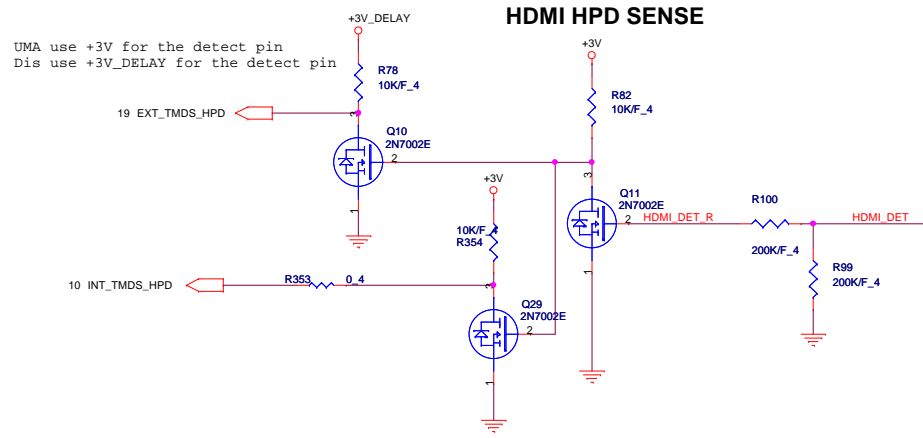
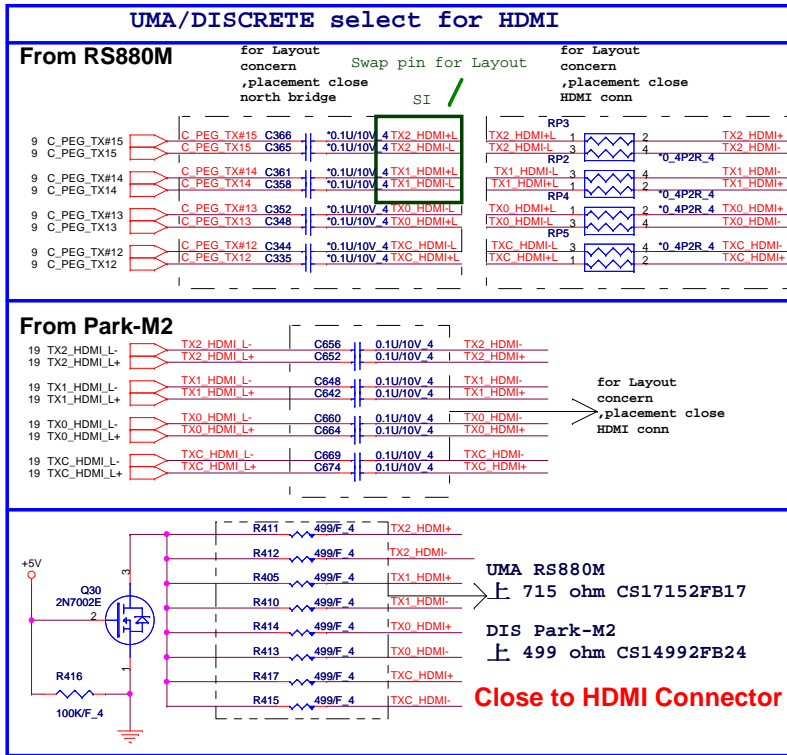
OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA



PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
LVDS/CRT Hyper_switch		
Date: Monday, September 28, 2009	Sheet 26	of 46

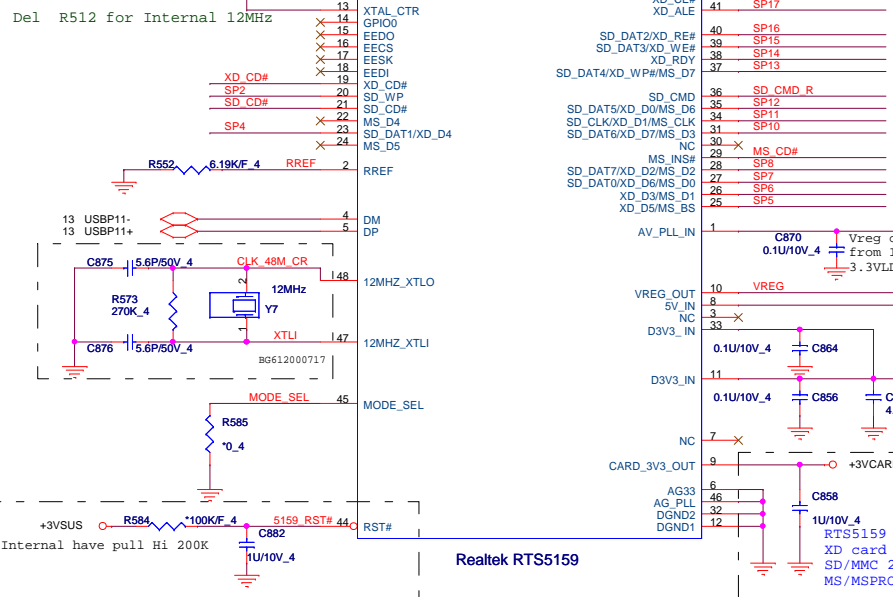
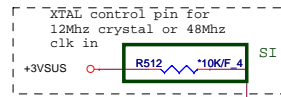
+5V 24,25,27,28,29,33,34,35,42
+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,27,28,29,30,31,32,33,34,35,36,42
+1.8V 5,8,10,11,16,42



- ⌈ +5V 24,25,26,28,29,33,34,35,42
- ⌈ +3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,28,29,30,31,32,33,34,35,36,42
- ⌈ +3V_DELAY 18,19,20,21,26

PROJECT : LX89
Quanta Computer Inc.

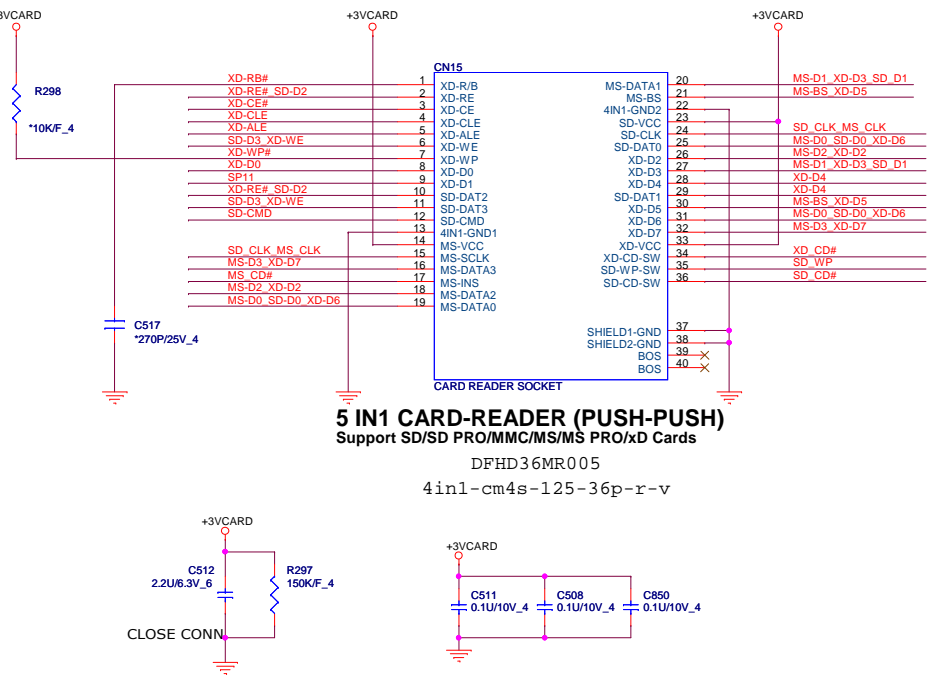
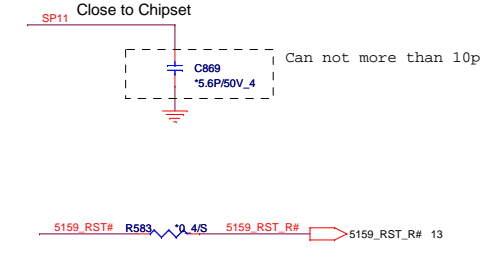
Size Custom	Document Number HDMI	Rev 1A
Date: Monday, September 28, 2009 Sheet 27 of 46		



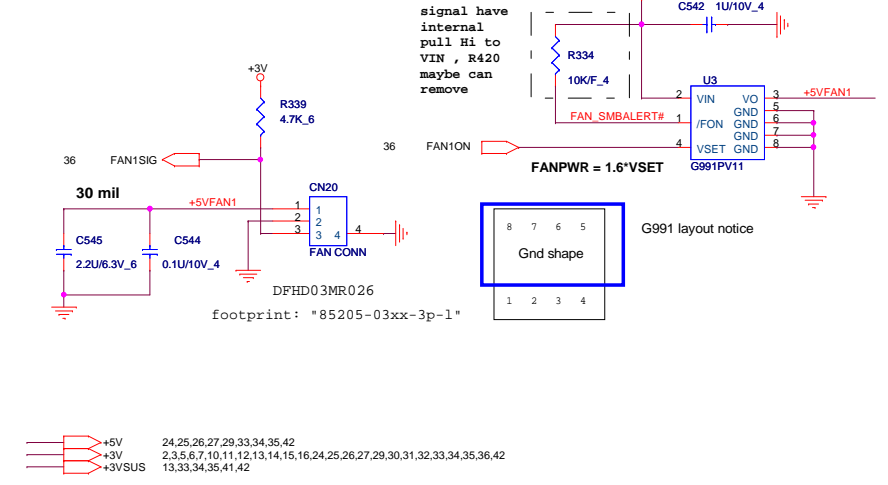
Note:

SD/MMC	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DATA1	XD D4
SP5	MS_BS	XD D5
SP6	MS_D1	XD D3
SP7	SD_DATA0	MS_D0
SP8	SD_DATA7	MS_D2
SP9	MS_IN#	XD D2
SP10	SD_DATA6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DATA5	XD D0
SP13	SD_DATA4	XD_WP#
SP14	SD_DATA3	XD_RE#
SP15	SD_DATA2	XD_WE#
SP16	SD_DATA1	XD_LE
SP17	SD_DATA0	XD_ALE
SP18	SD_CMD_R	XD_CE#
SP19		XD_CLE

SP7	R528	0.4	MS-D0	SD-D0	XD-D6
SP6	R524	0.4	MS-D1	SD-D3	SD-D1
SP8	R531	0.4	MS-D2	XD-D2	
SP16	R579	0.4	XD-RE#	SD-D2	
SP5	R522	0.4	MS-BS	XD-D5	
SP15	R578	0.4	SD-D3	XD-WE	
SP11	R569	0.4	SD-CLK	MS-CLK	
SP2	R511	0.4	SD_WP		
SP13	R576	0.4	XD_WP#		
SP19	R582	0.4	XD-CLE		
SP4	R510	0.4	XD-D4		
SP10	R537	0.4	MS-D3	XD-D7	
SP14	R577	0.4	XD-RB#		
SP12	R570	0.4	XD-D0		
SP17	R580	0.4	XD-ALE		
SP18	R581	0.4	XD-CE#		
SD_CMD_R	R571	0.4	SD-CMD		



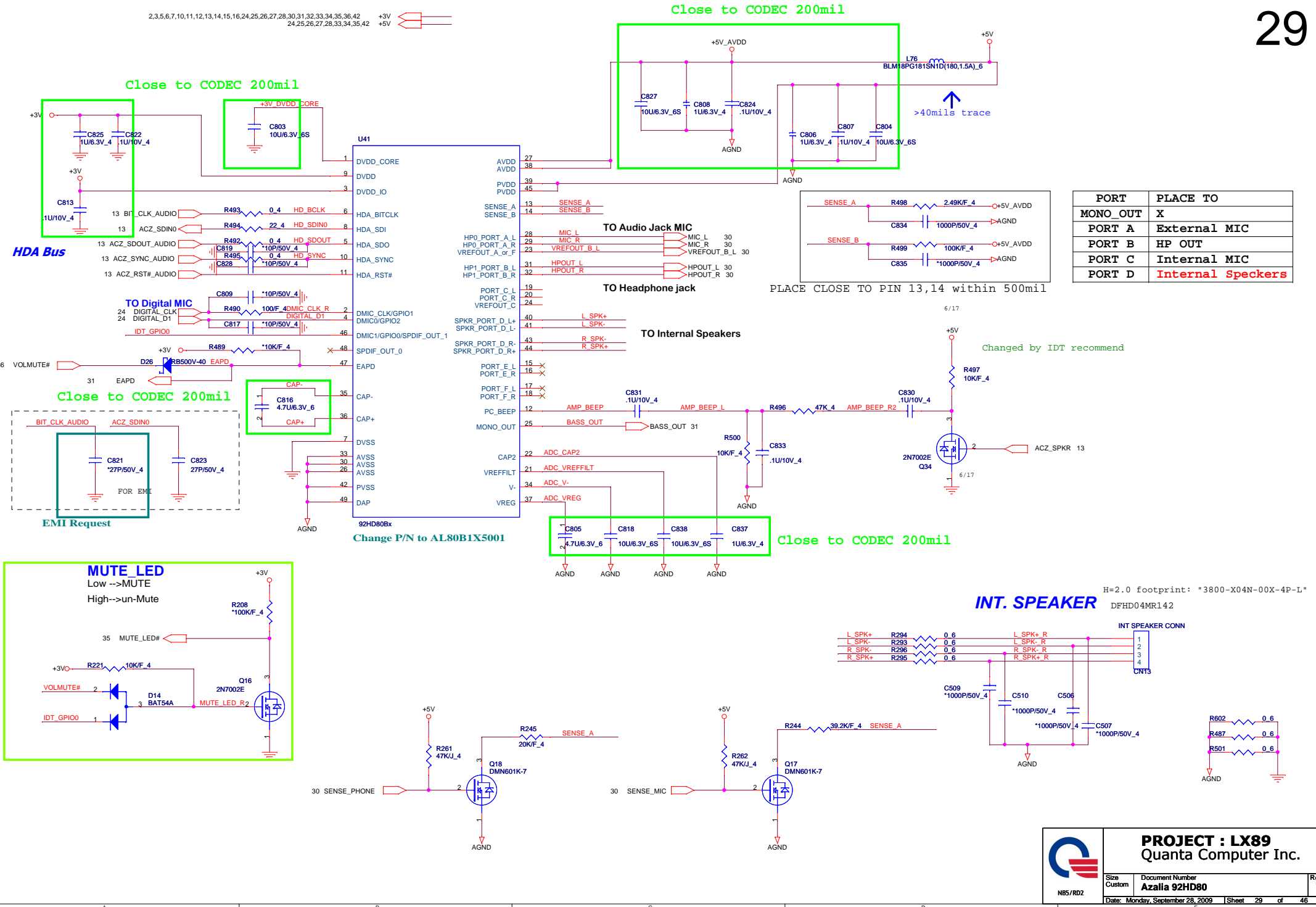
CPU FAN



PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	RTS5159&CPU FAN	
Date: Monday, September 28, 2009 Sheet 28 of 46		

2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,30,31,32,33,34,35,36,42
24,25,26,27,28,33,34,35,42



PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers

PLACE CLOSE TO PIN 13,14 within 500mil

Changed by IDT recommend

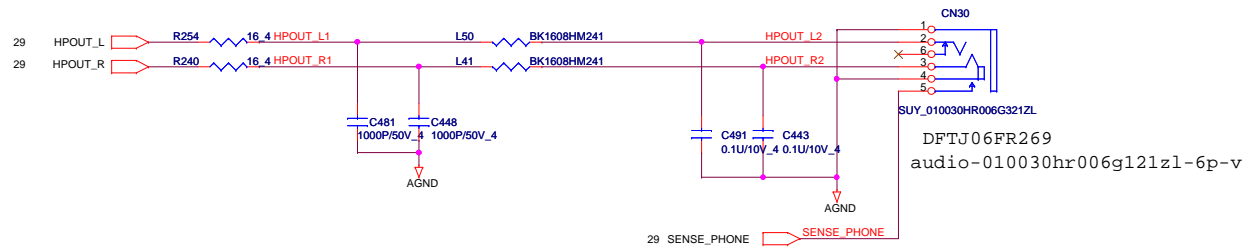
H=2.0 footprint: "3800-X04N-00X-4P-L"
DFHD04MR142

	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Document Number Azalia 92HD80	Rev 1A
Date: Monday, September 28, 2009		Sheet 29 of 46

Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

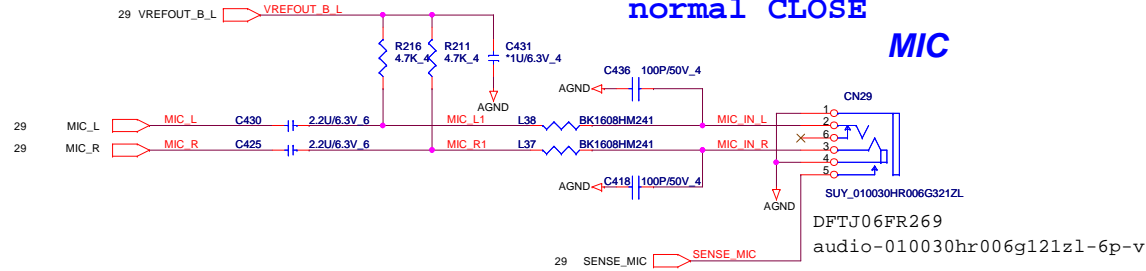
33,34,36,37,38,39,40,41,42,43 +5VPCU
2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,31,32,33,34,35,36,42 +3V

normal CLOSE Line out



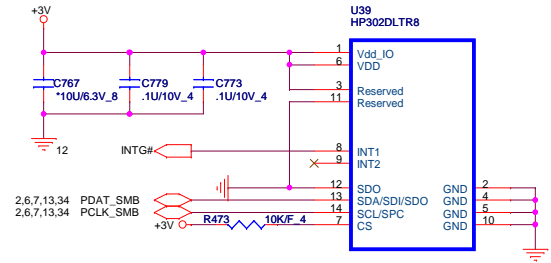
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.


normal CLOSE MIC



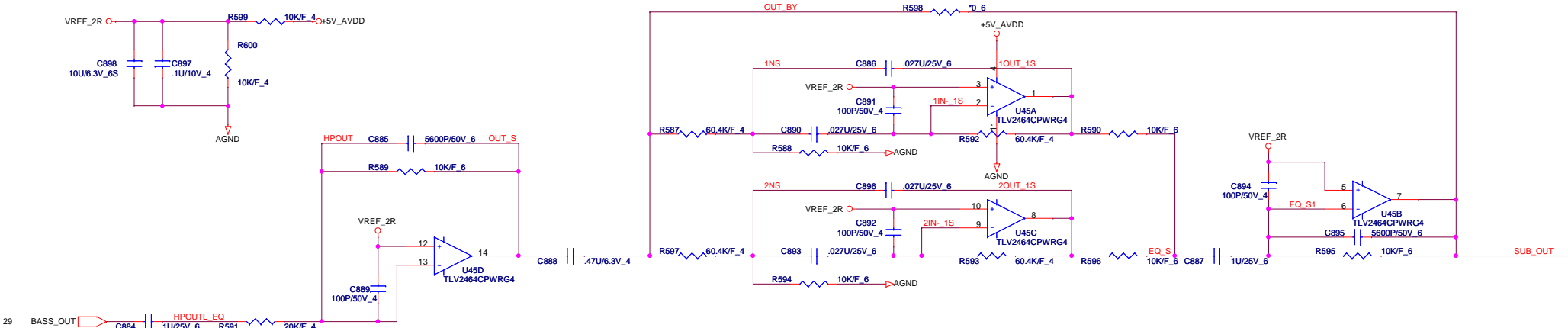
Accelerometer Sensor

SGT-LI9302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



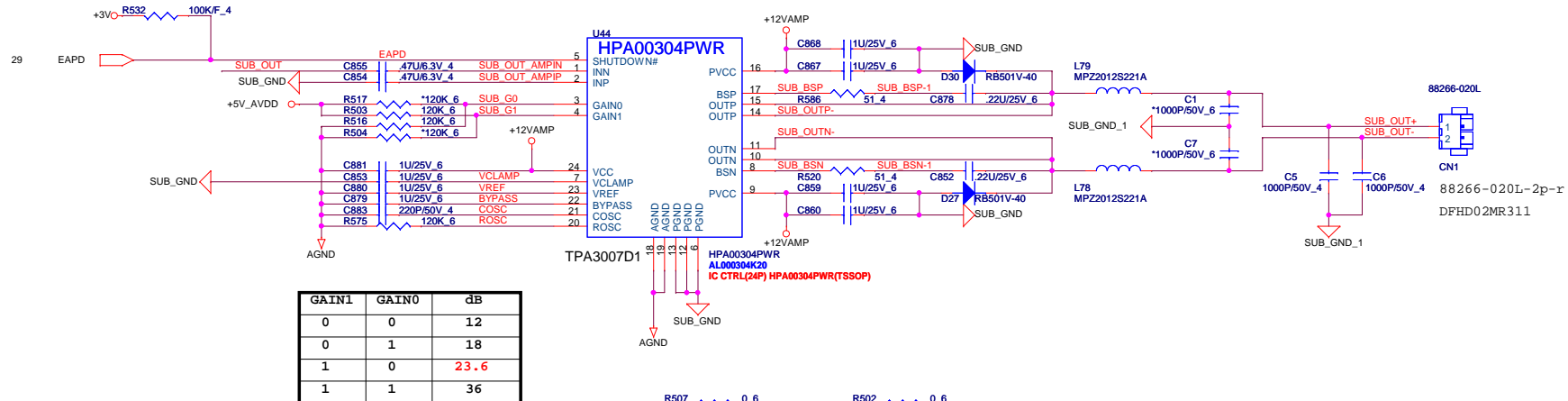
 <p>NBS/RD2</p>	<p>PROJECT : LX89 Quanta Computer Inc.</p>		<p>Rev 1A</p>	
	<p>Size Custom</p>	<p>Document Number Audio Jack/Accelerometer</p>		<p>Date: Monday, September 28, 2009 Sheet 30 of 46</p>

EQ FOR SUBWOOFER



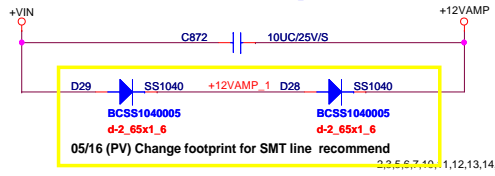
MODEL	UP7
R9402	60.4K/F_6
R9403	60.4K/F_6
R9407	60.4K/F_6
R9408	60.4K/F_6
C5144	0.027U/25V_6
C5146	0.027U/25V_6
C5148	0.027U/25V_6
C5153	0.027U/25V_6

5/27: NA for subwofer function



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

Sub-Woofer power

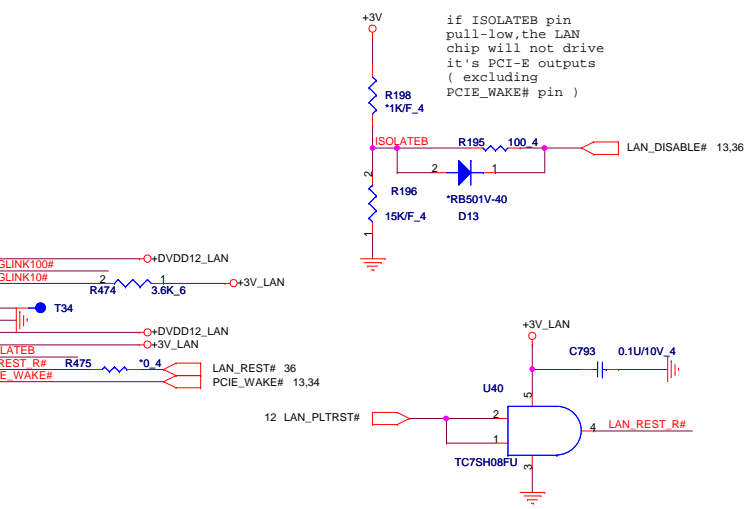
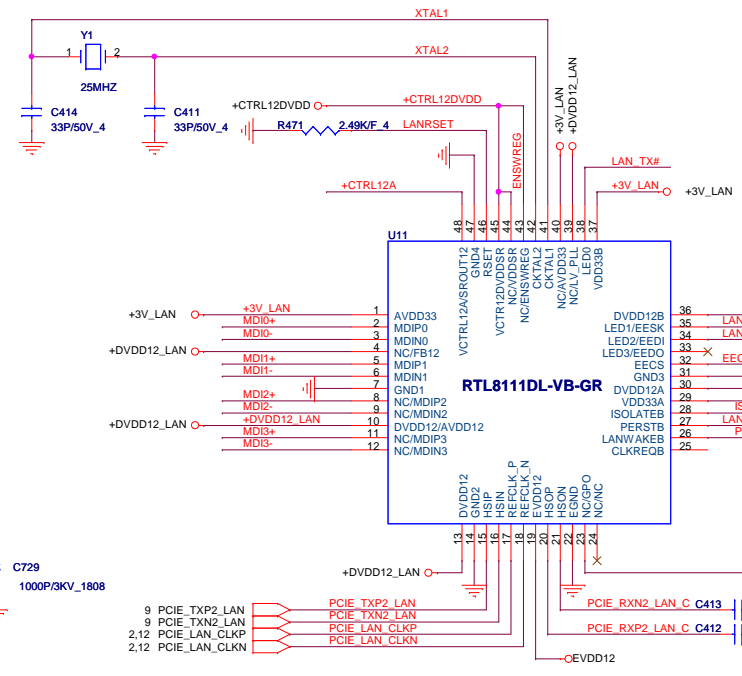
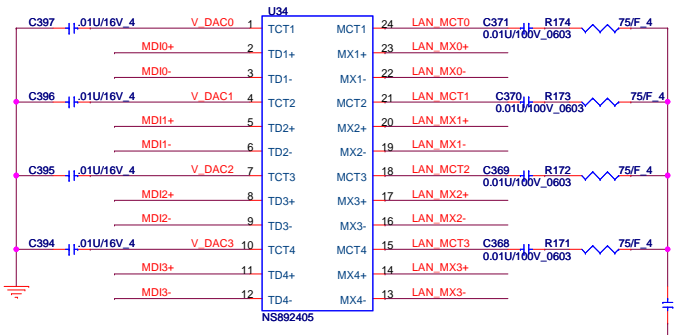
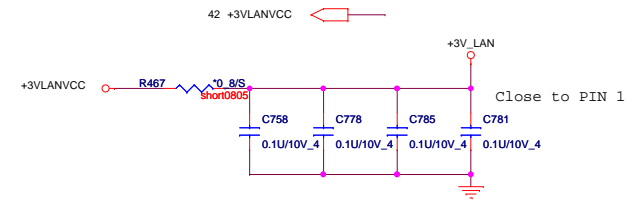
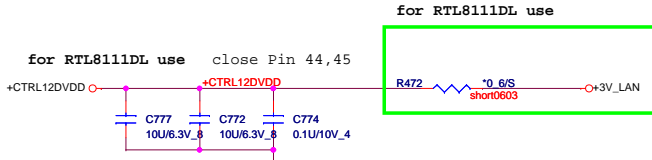


+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,32,33,34,35,36,42
 +5V_AVDD 29
 +VIN 24,37,38,39,40,41,42,43

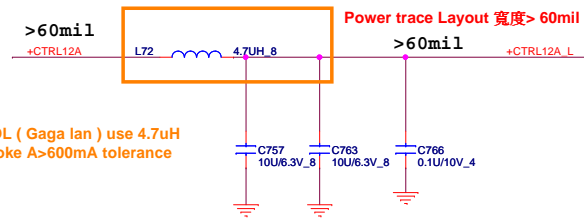
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
SUBWOOFER (EQ & AMP.)		
Date: Monday, September 28, 2009	Sheet 31	of 46

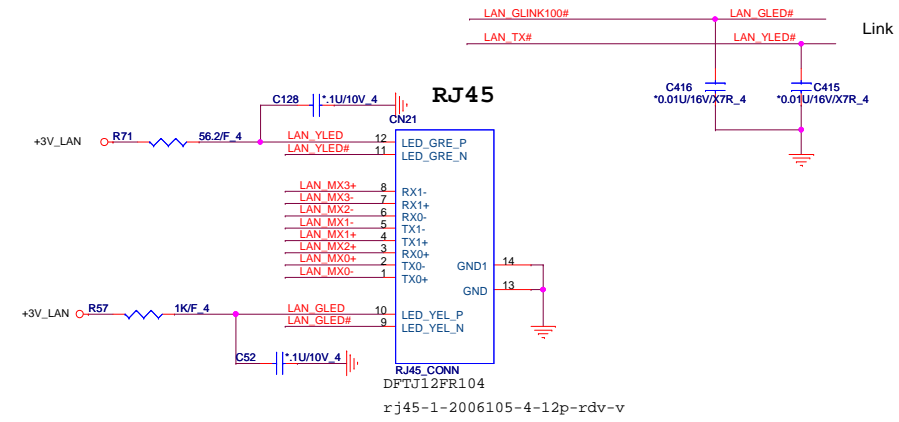
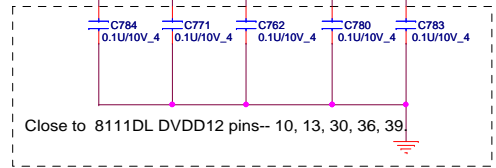
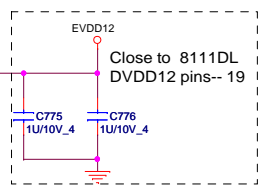
T : Stuffed for RTL8111DL(10/100/1000)



NS892402:GIGABIT DB0AT9LAN05

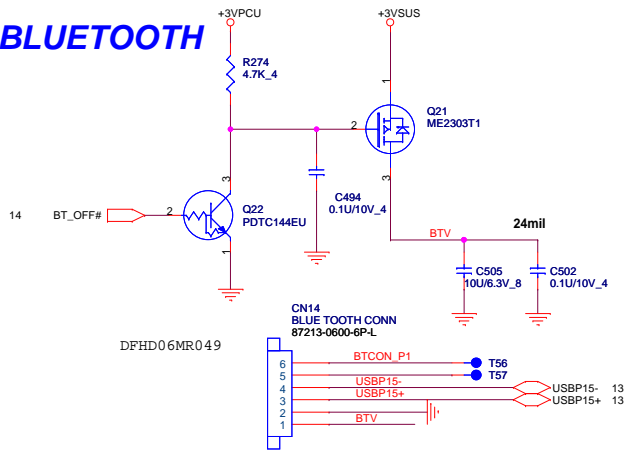


L149
RTL8111DL (Giga lan) use 4.7uH
power choke A>600mA tolerance
±15%

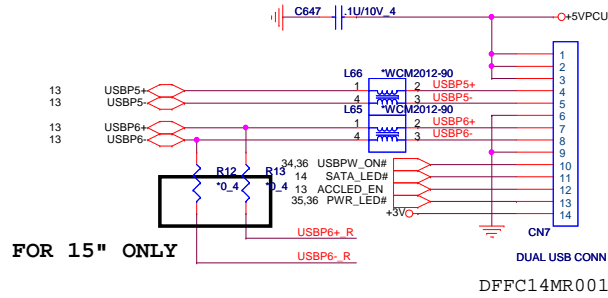


	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	RTL8111DL/RJ45	
Date: Monday, September 28, 2009	Sheet	32	of 46

BLUETOOTH

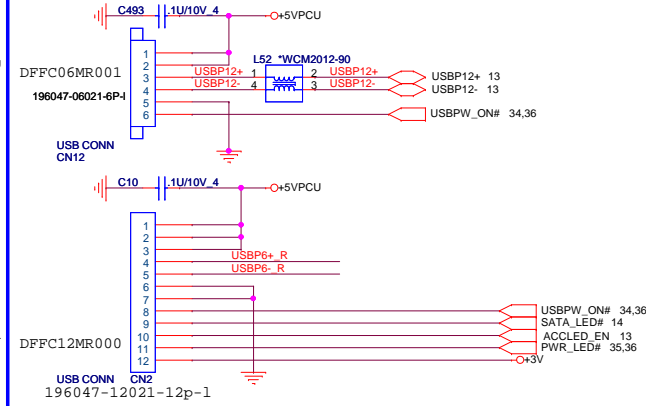


RIGHT SIDE USB2 for 17"



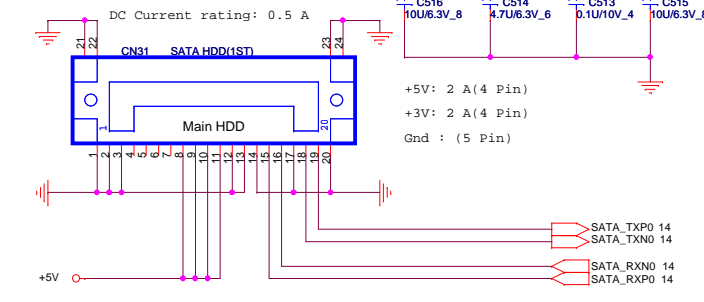
FOR 15" ONLY

RIGHT SIDE USB2 for 15"



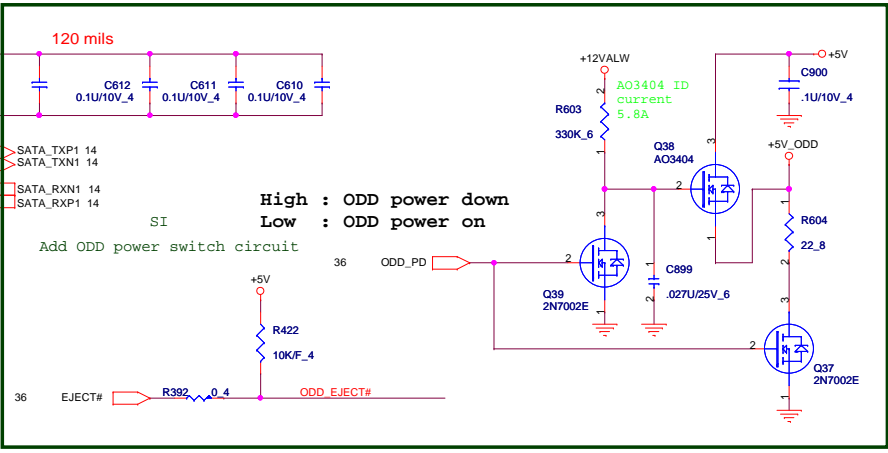
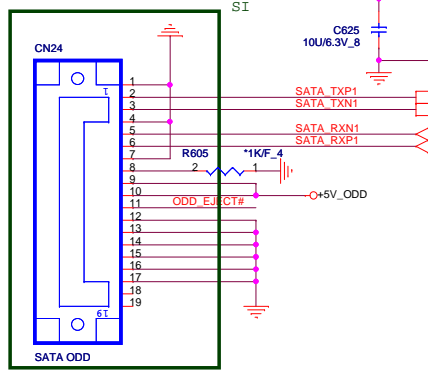
SATA HDD CONNECTOR

H=2.6 Footprint: "GS12201-1011-9F-20P-L"
DFHD20MR023



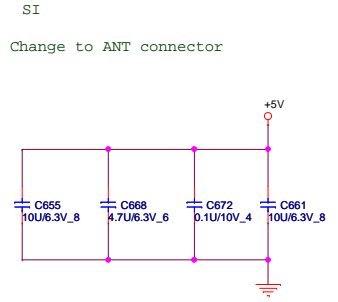
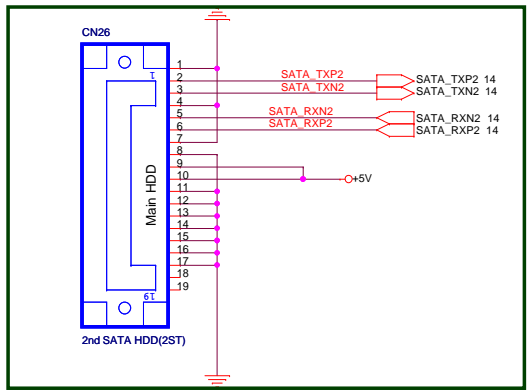
SATA CD-ROM

Change to ANT connector



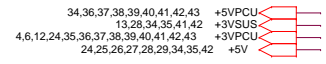
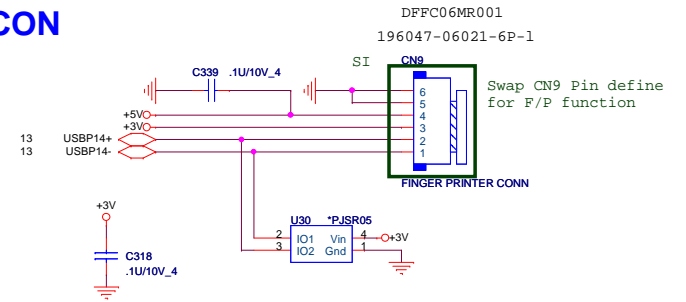
SATA_2 HDD CONNECTOR FOR 17.3"

+5V: 2 A(4 Pin)
Gnd : (5 Pin)



USB Fingerprint CON

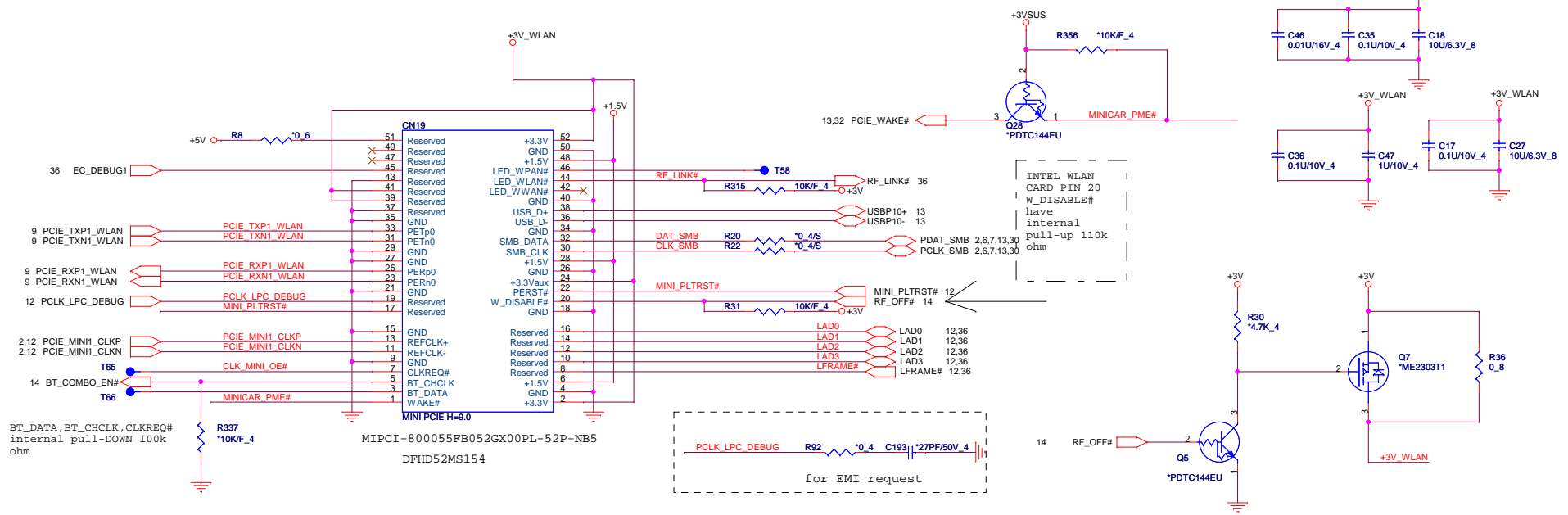
1. SYSTEM GND
2. SYSTEM GND
- 3.LED PWR(+5V)
- 4.USB PWR(+3V)
5. USB1.1+
6. USB1.1-



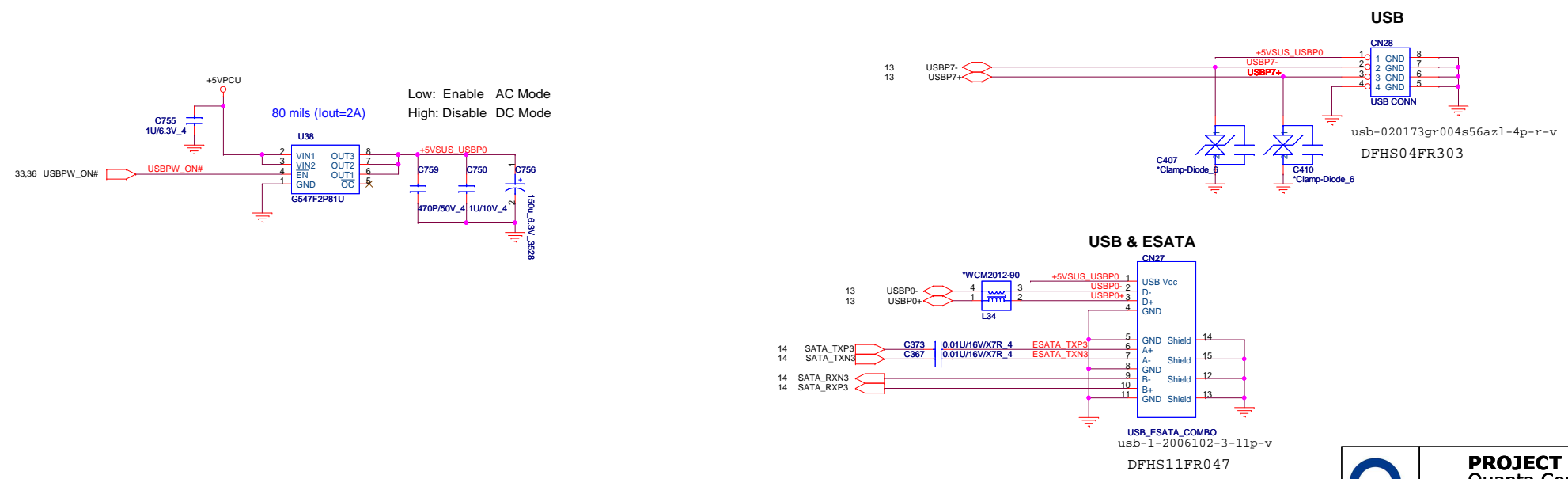
PROJECT : LX89
Quanta Computer Inc.


Size Custom	Document Number BT/FP/USBX2/SATA HDDX2/ODD	Rev 1A
Date: Monday, September 28, 2009	Sheet 33	of 46

Mini PCI-E Card WLAN

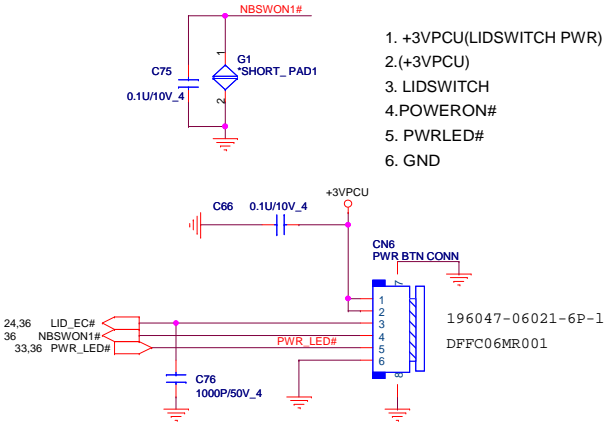


USB2.0 X 1 and E-SATA/USB2.0 COMBO

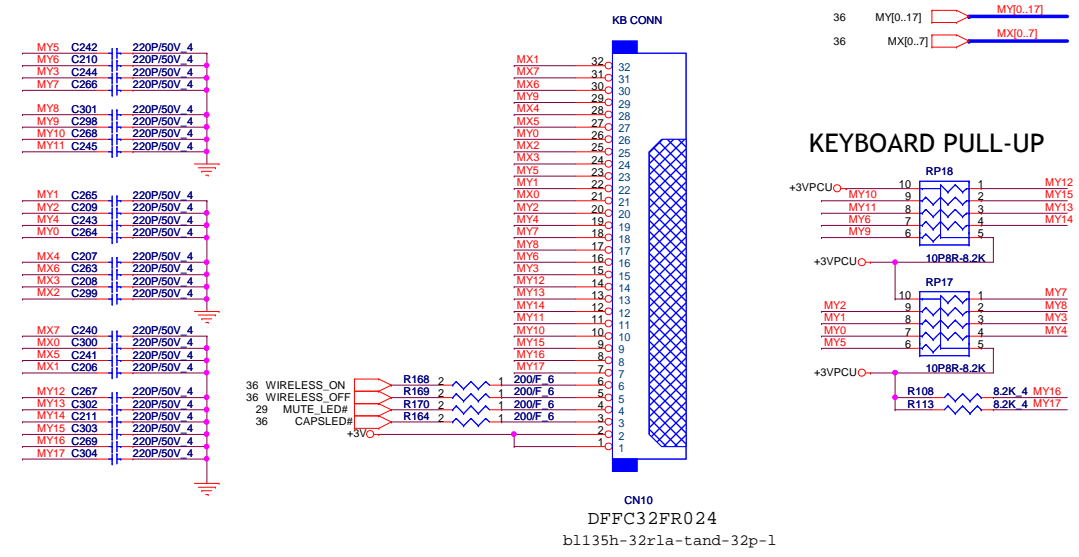


			PROJECT : LX89 Quanta Computer Inc.	

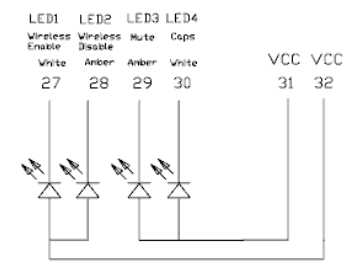
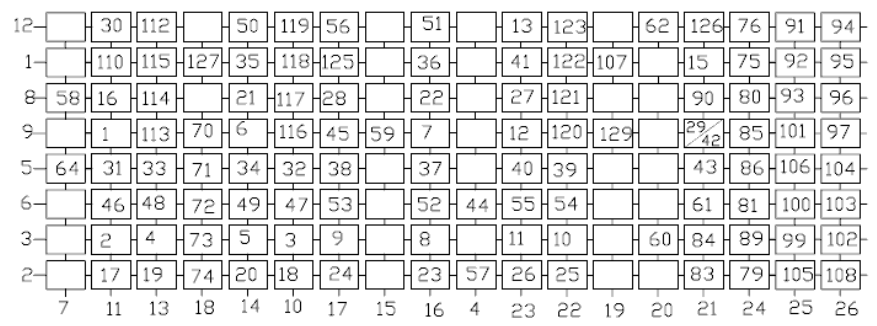
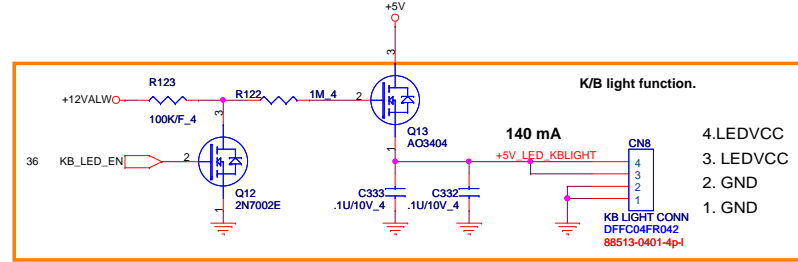
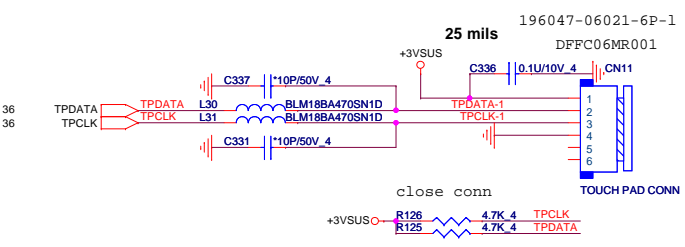
POWER BUTTON CONNECT



KEYBOARD Con.

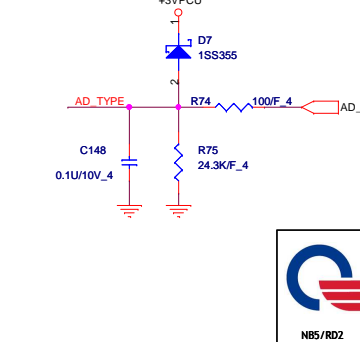
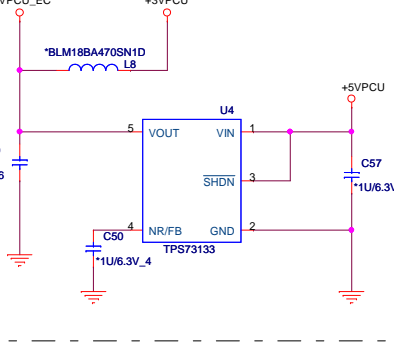
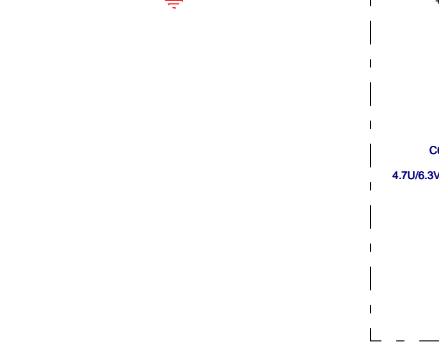
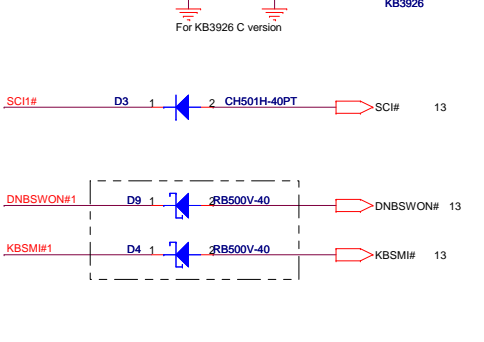
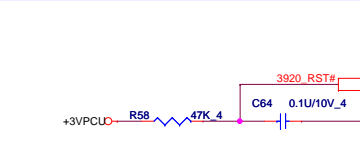
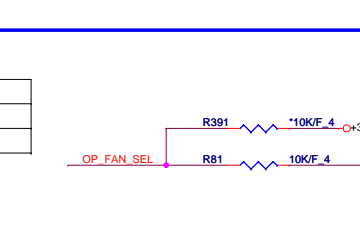
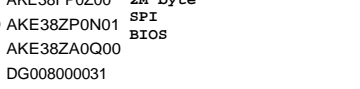
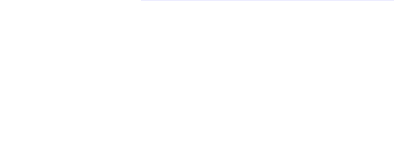
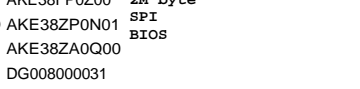
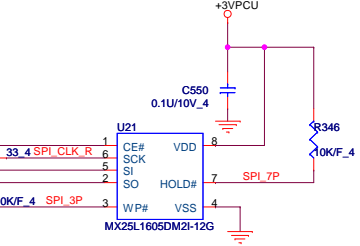
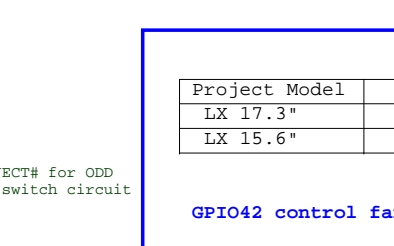
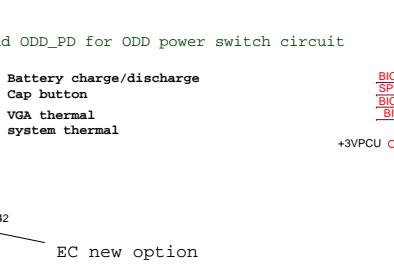
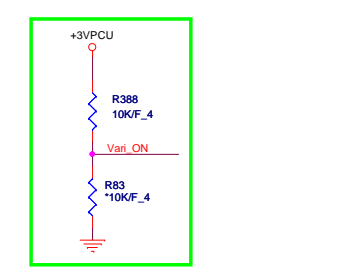
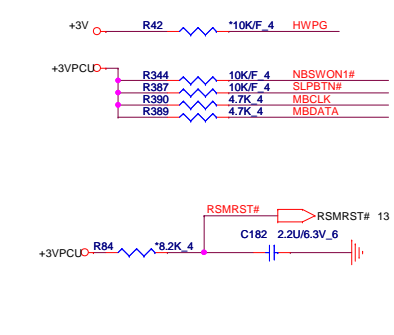
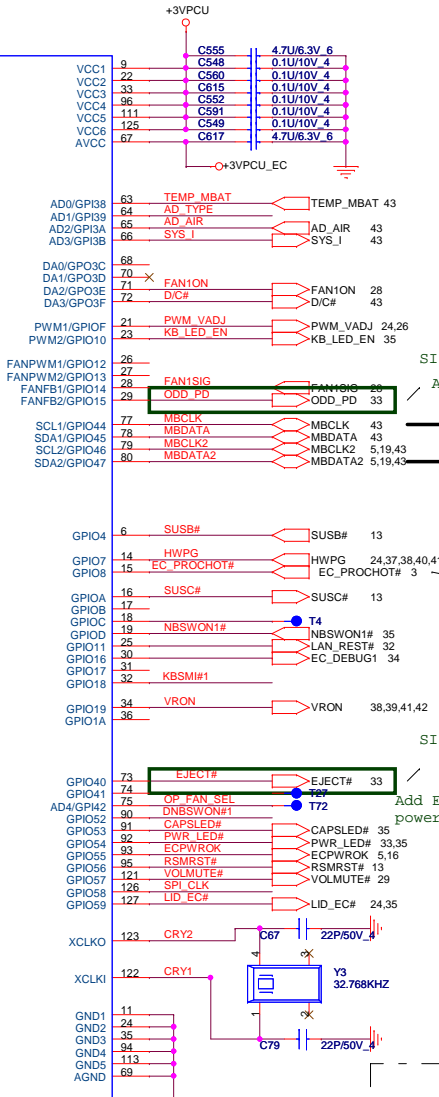
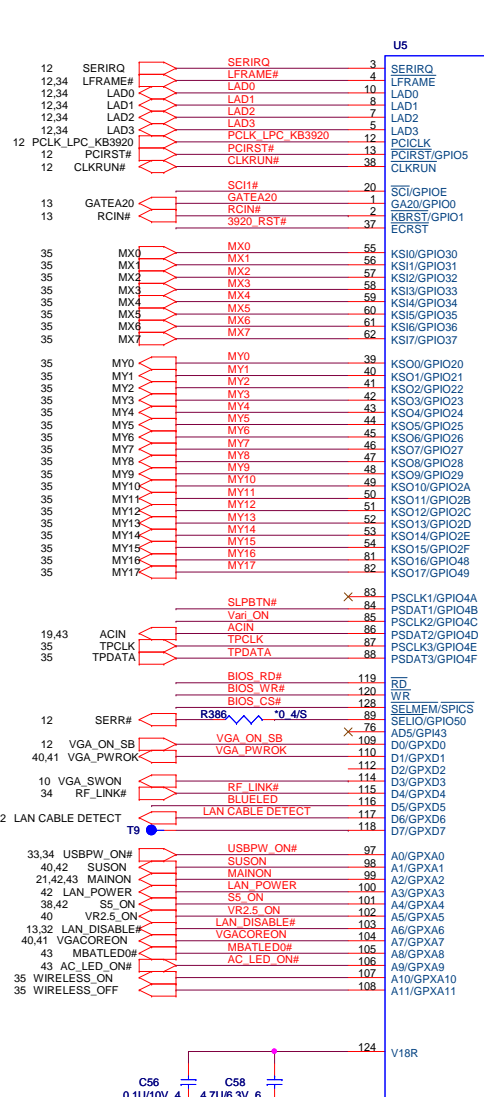


TOUCH PAD CONN



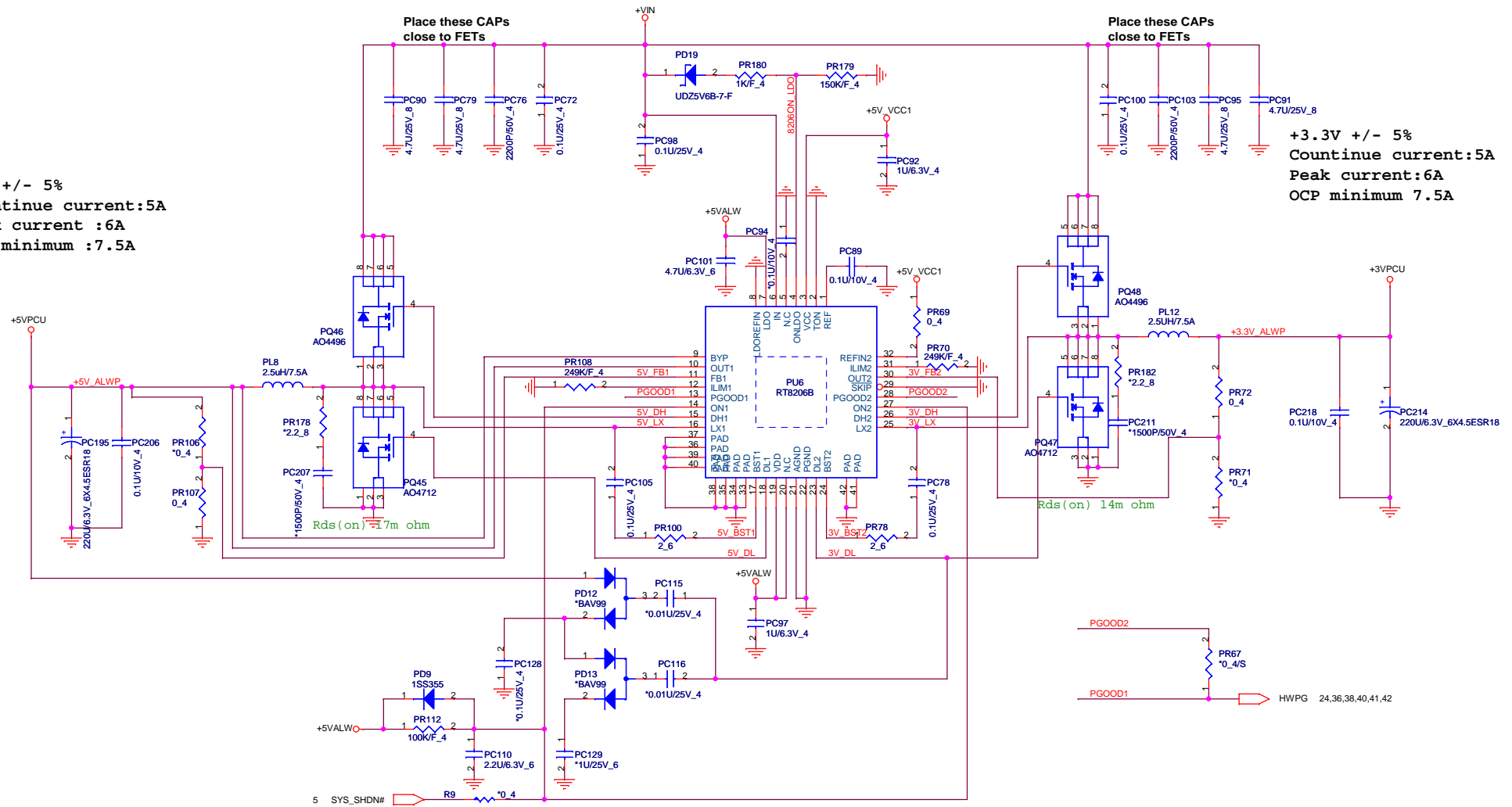
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number LED/KEYBOARD/SW_BOARD	Rev 1A
Date: Monday, September 28, 2009 Sheet 35 of 46		



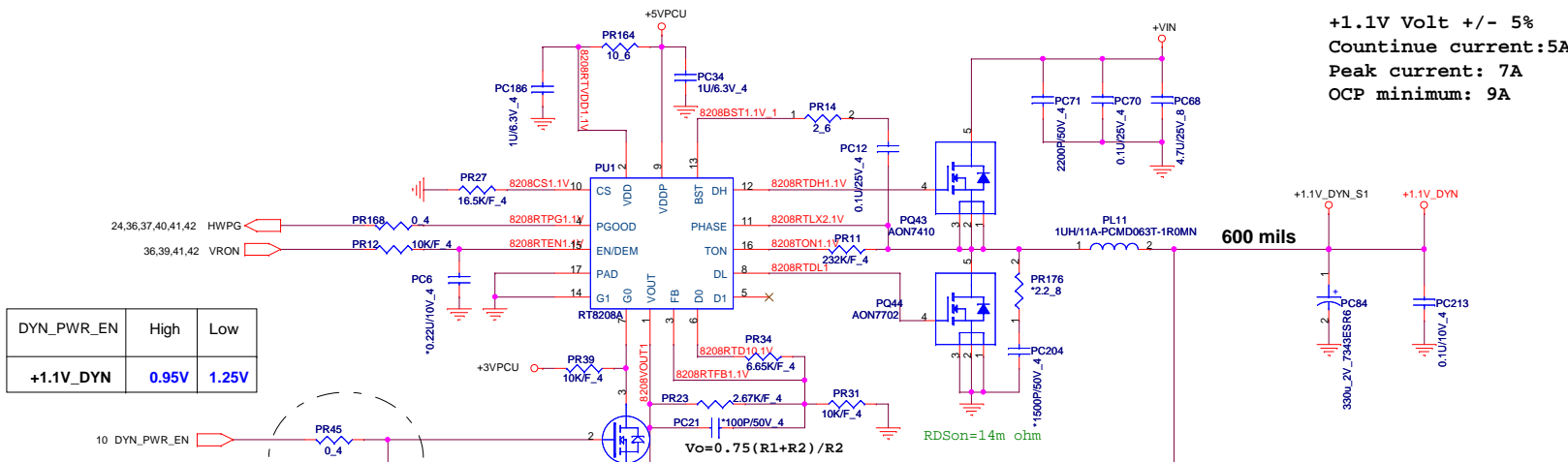
+5V +/- 5%
 Countinue current:5A
 Peak current :6A
 OCP minimum :7.5A

+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum 7.5A



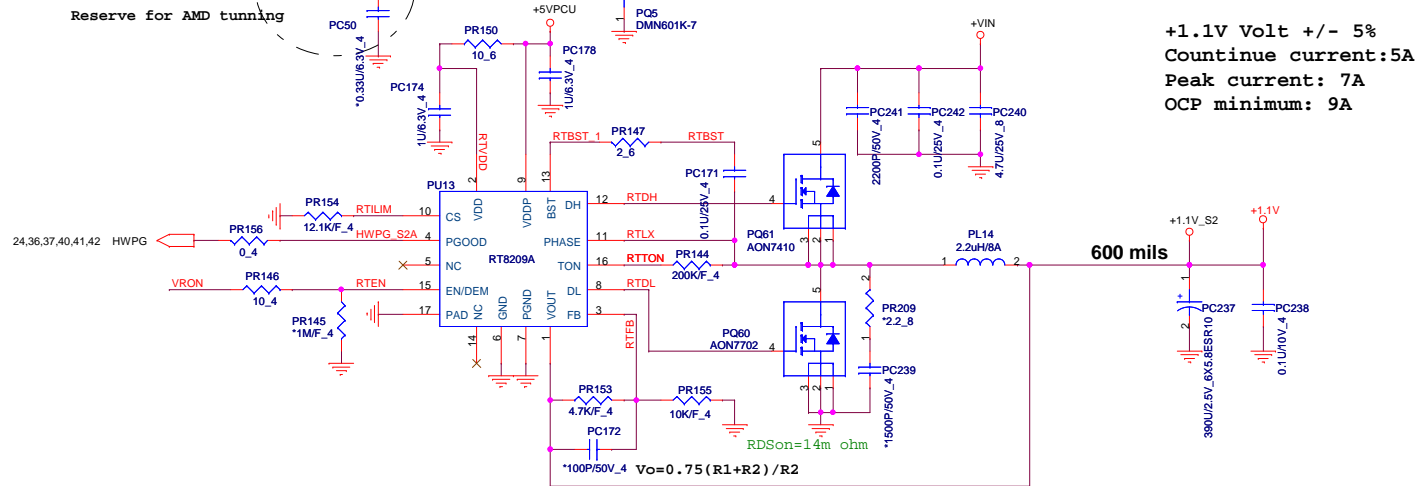
- +VIN 24,31,38,39,40,41,42,43
- +3VPCU 4,6,12,24,33,35,36,38,39,40,41,42,43
- +5VPCU 33,34,36,38,39,40,41,42,43

	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Size Custom	Document Number +5V/+3V (RT8206B)
Date: Monday, September 28, 2009 Sheet 37 of 46		

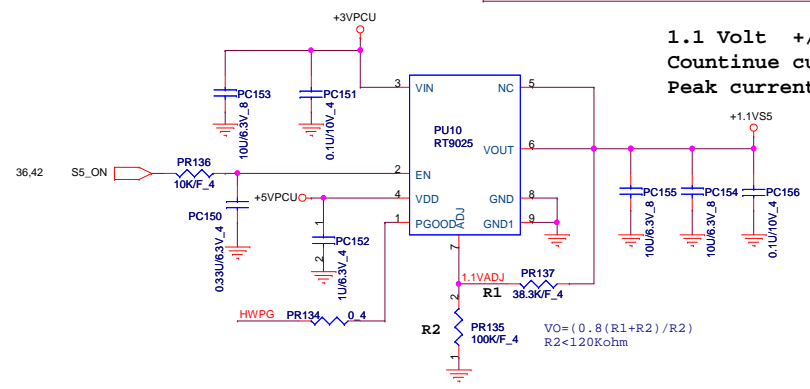


DYN_PWR_EN	High	Low
+1.1V_DYN	0.95V	1.25V

Reserve for AMD tuning



1.1 Volt +/- 5%
 Countinue current:0.2A
 Peak current:0.5A



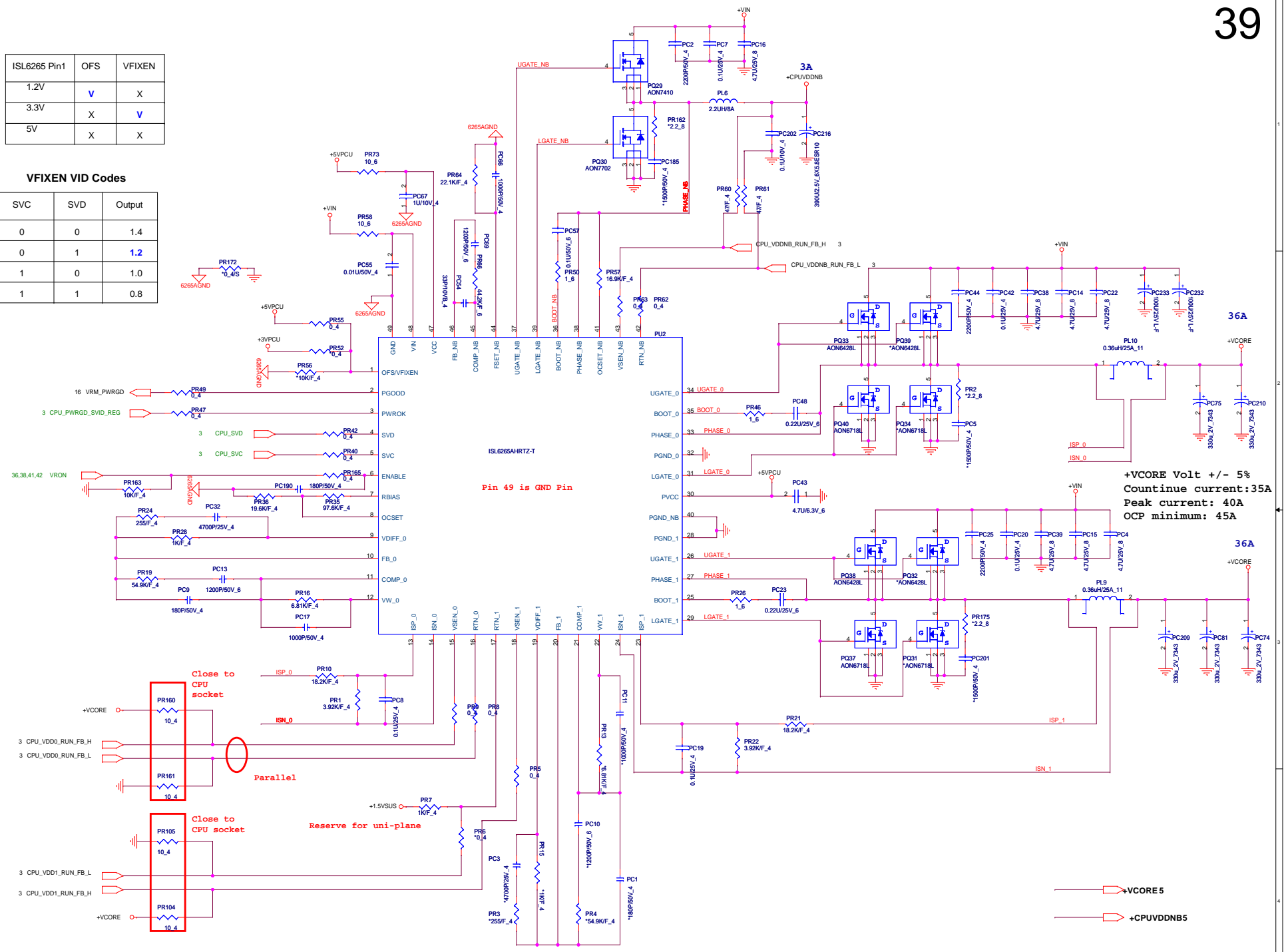
PROJECT : LX89
 Quanta Computer Inc.

Size Custom	Document Number VGA Core/+1.8VGF1.0VGF	Rev 1A
Date: Monday, September 28, 2009	Sheet 38	of 46

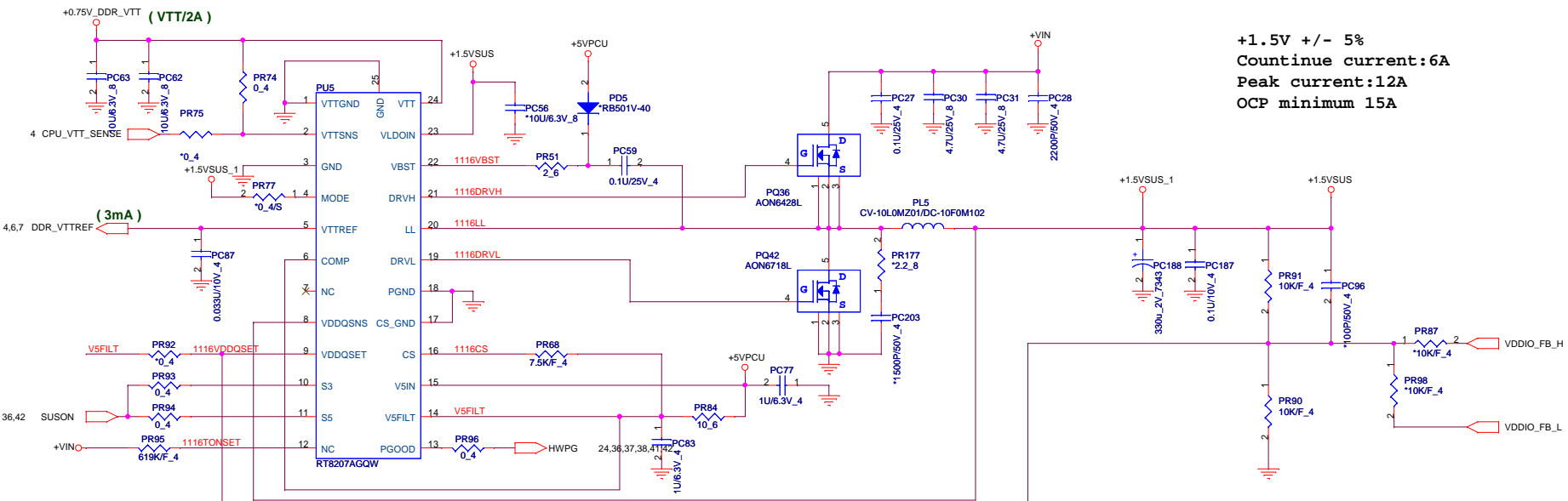
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

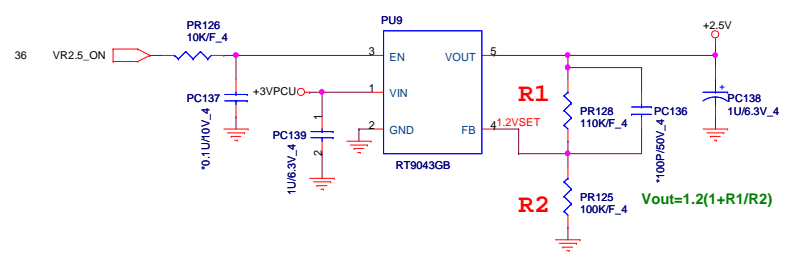
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



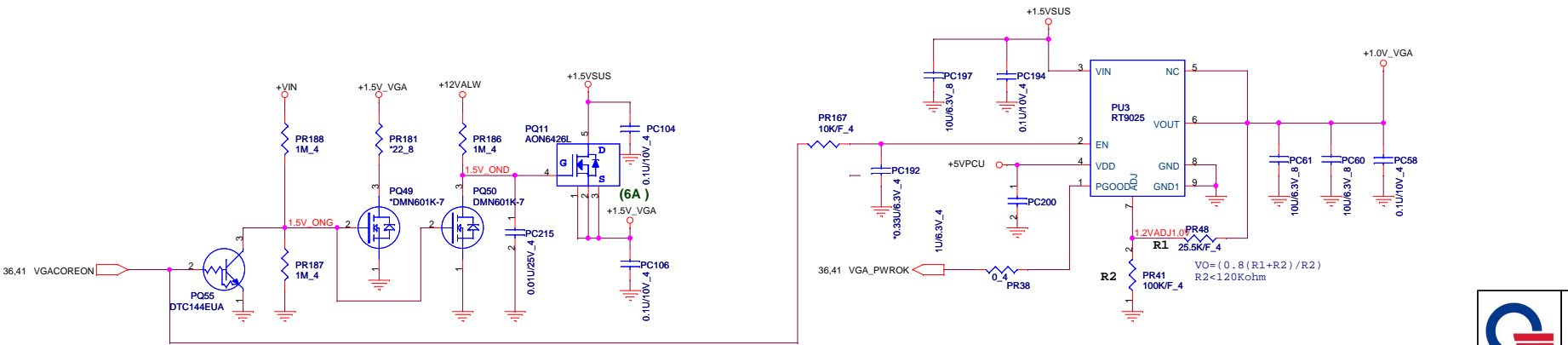
+VCORE Volt +/- 5%
 Countinue current:35A
 Peak current: 40A
 OCP minimum: 45A




+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA



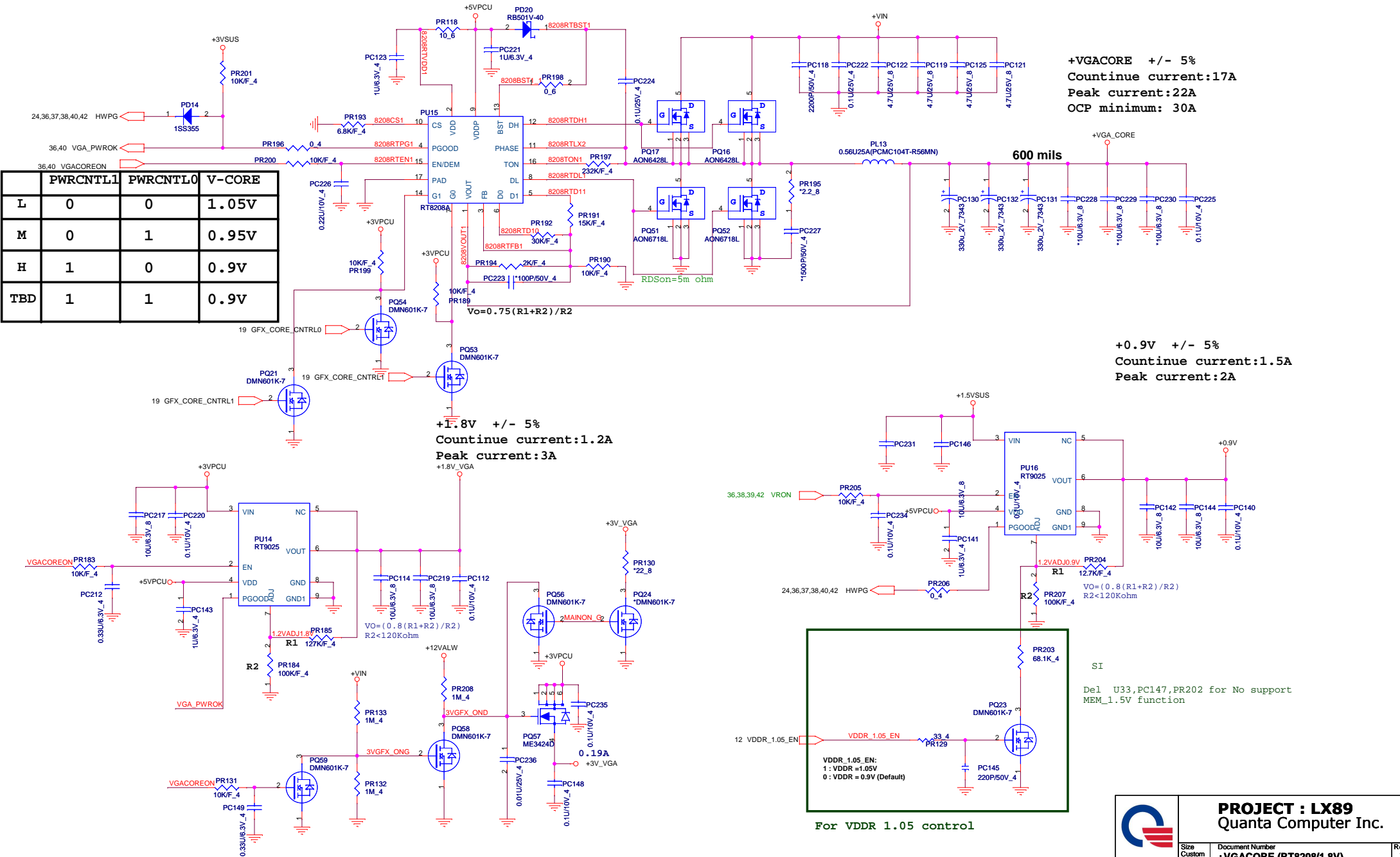
+1.0V +/- 5%
Countinue current:1.5A
Peak current:3A



 PROJECT : LX89 Quanta Computer Inc.			Size	Document Number	Rev
			Custom	DDR3 (RT8207)	1A
NBS/RD2			Date: Monday, September 28, 2009	Sheet 40 of 46	

VGA Core

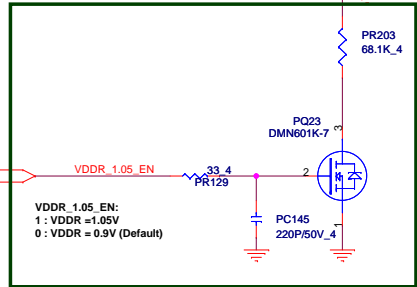
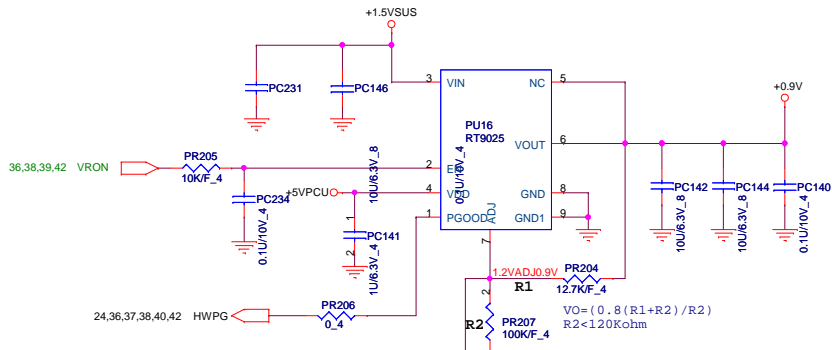
	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	1.05V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.9V



+VGACORE +/- 5%
 Continue current:1.7A
 Peak current:2.2A
 OCP minimum: 30A


+0.9V +/- 5%
 Continue current:1.5A
 Peak current:2A

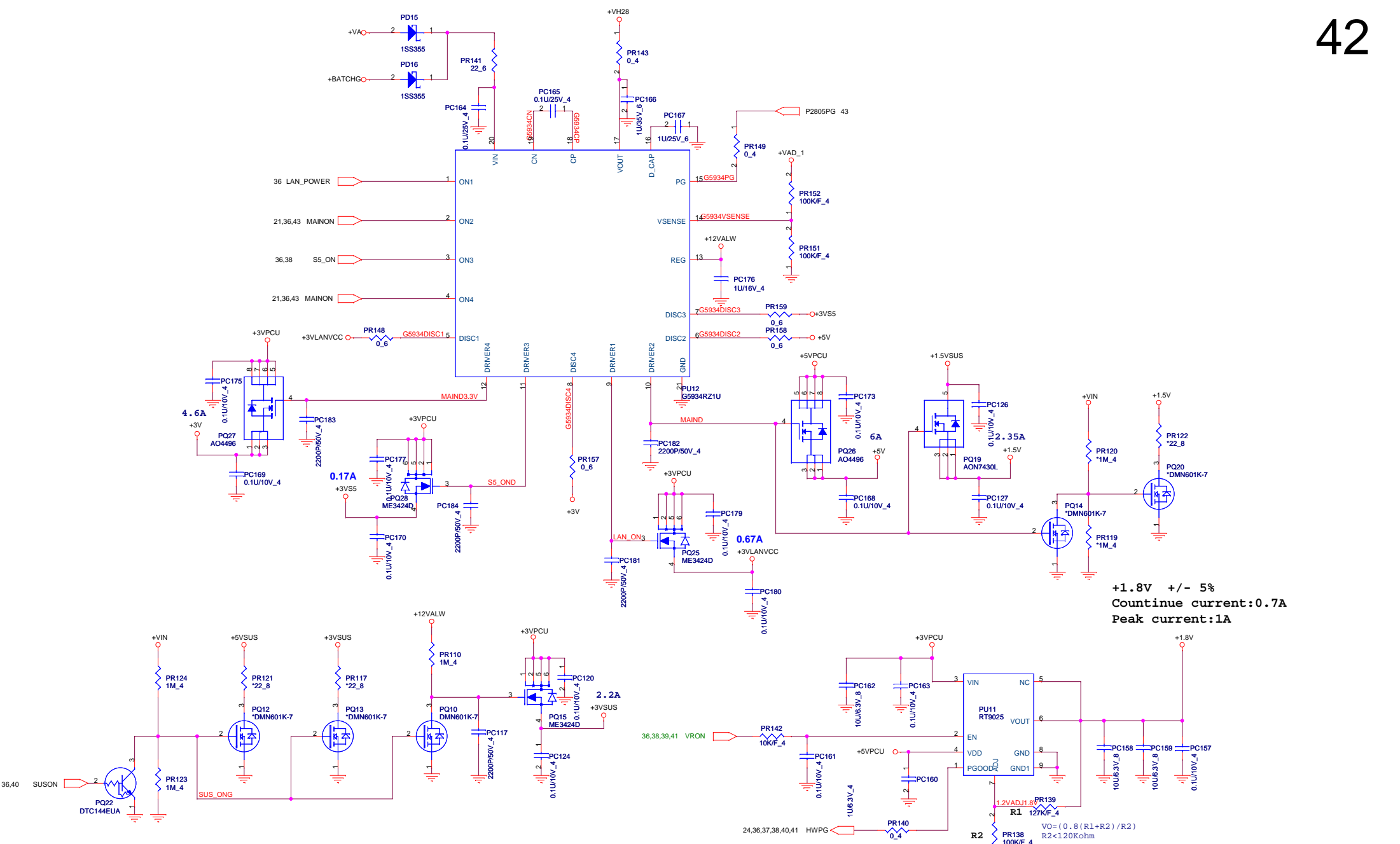
+1.8V +/- 5%
 Continue current:1.2A
 Peak current:3A




For VDDR 1.05 control

SI
 Del U33,PC147,PR202 for No support
 MEM_1.5V function

 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Document Number +VGACORE (RT8208/1.8V)	Rev 1A
Date: Monday, September 28, 2009 Sheet 41 of 46		

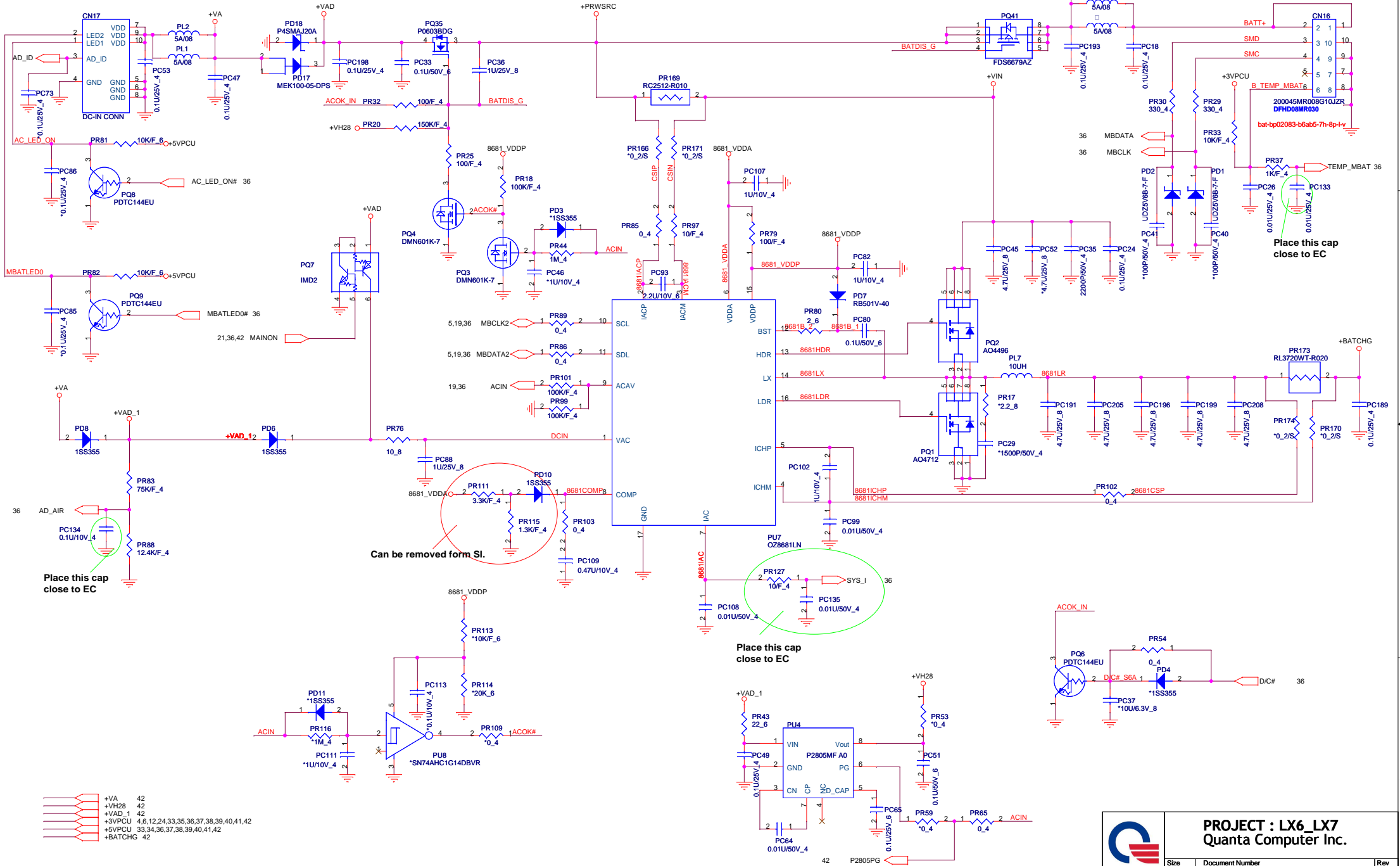


+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

	PROJECT : LX89	
	Quanta Computer Inc.	
Size Custom	Document Number Dis-charge IC (P2806)	Rev 1A
Date: Monday, September 28, 2009 Sheet 42 of 46		

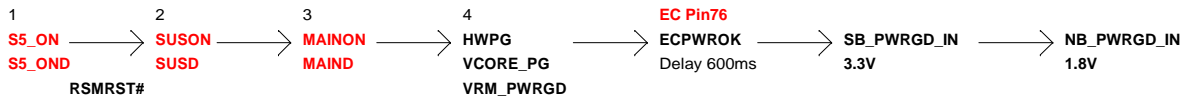
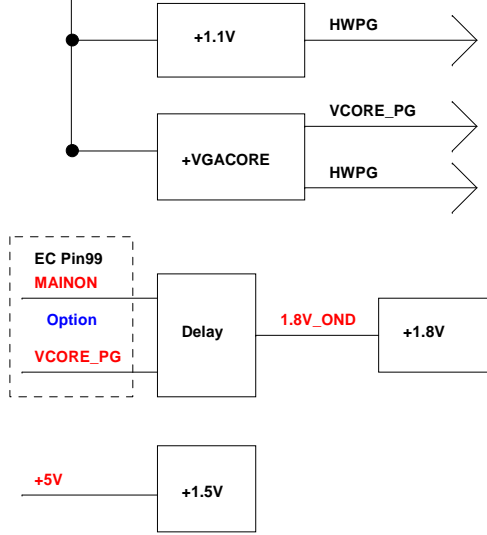
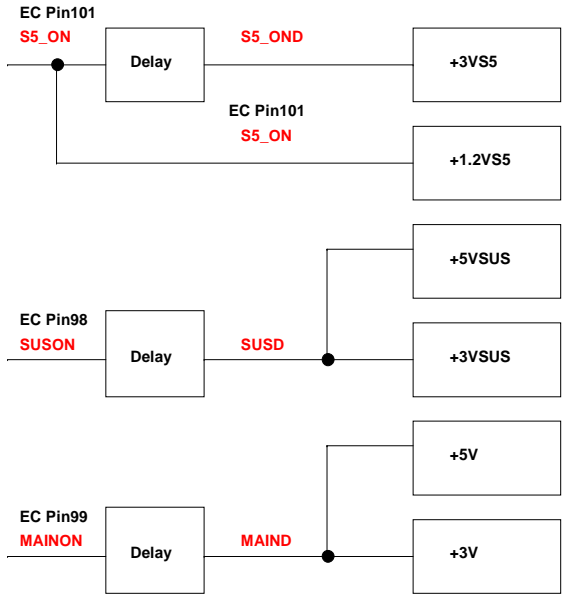
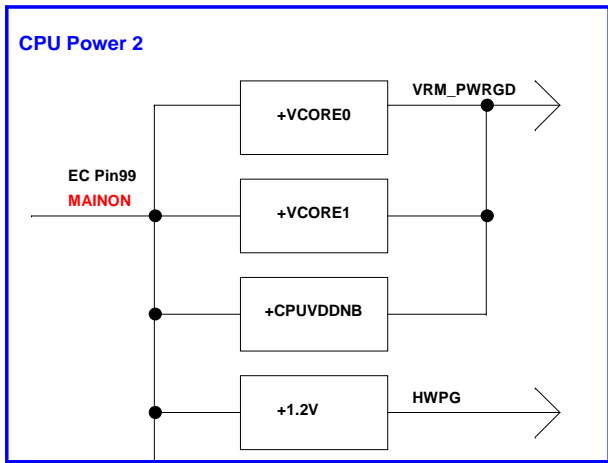
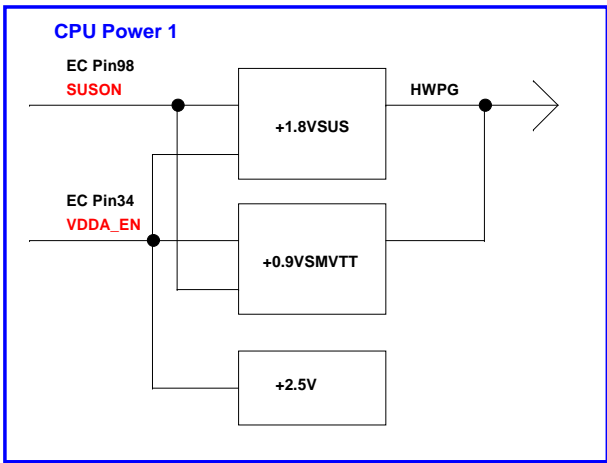
TOP DC JACK
65W/90W

20346-100n-1-10p-1dv



- +VA 42
- +VH28 42
- +VAD_1 42
- +3VPCU 4.6,12,24,33,35,36,37,38,39,40,41,42
- +5VPCU 33,34,36,37,38,39,40,41,42
- +BATCHG 42

	PROJECT : LX6_LX7	
	Quanta Computer Inc.	
	Size Custom	Document Number Charger (BQ24704)
Date: Monday, September 28, 2009 Sheet 43 of 46		



Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLAVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS


DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

 Custom-Doc NBS/RD2	PROJECT : LX89 Quanta Computer Inc.	
	Size	Document Number
	Date: Monday, September 28, 2009	Sheet 45 of 46